Design and Test of a Signal Packet Router Prototype for the ATLAS NSW sTGC Detector

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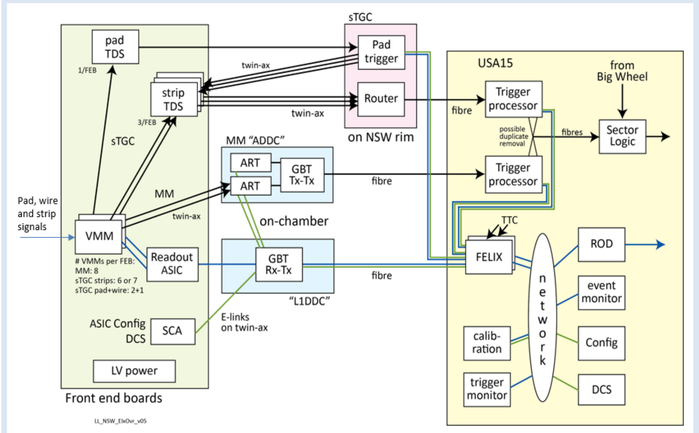
on behalf of the ATLAS Muon Collaboration

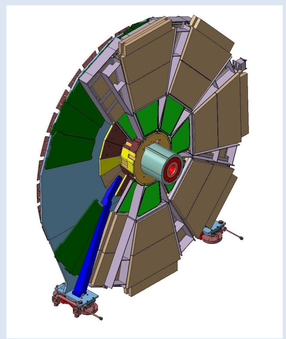
NSW sTGC Detector Electronics System



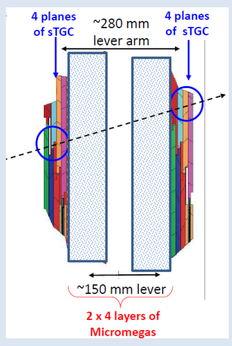
sTGC electronic system for one layer of a 1/16th sector

- The New Small Wheel (NSW) detector consists of two detector technologies: small-strip thin-gap chambers (sTGC) and Micromegas (MM).
- On detecting a signal peak, FE electronics digitizes time & amplitude and then sends to TDS (Trigger Data Serializer).
- Signal Packet Router serves as a fast switching-yard @ 4.8Gbps between incoming active TDS signals and a limited number of optoelectronic outputs.

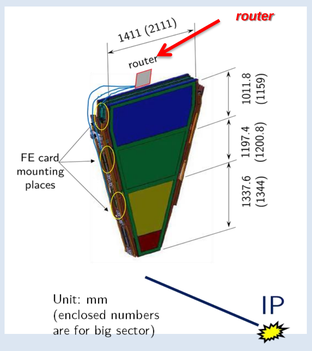
The sTGC Router Design R&D



NSW Mechanical Structure



NSW Detector Layout



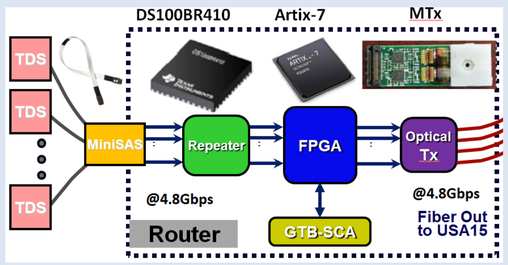
Router on the rim (shown one sector)

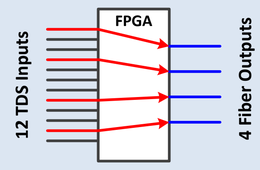
- One router board /sector layer: failure isolated to a single layer
- Recover degraded electronic signal
- Process all TDS data packets and drop NULL packets
- Input channels ~16 & Output channels ~4
- Fix & low latency (~90ns)
- Radiation tolerant: TID ~78kRad & SEU Mitigable

Strips@Inner	~406	#128-TDS	4
Strips@Middle	~365	#128-TDS	3
Strips@Outer	~307	#128-TDS	3
#128-TDS/1 Layer		10	
# TxRx/FPGA		16	
# FPGA's/1 Layer		1	
# FPGA's/4 Layer		4	
FPGA's/Sector		8	
Sectors/Wheel		16	
Wheels		2	
Total # FPGA's		8*16*2 = 256	
Total # Router's		**256**	

- Front End serial electrical link: TDS → Router, 4.8 Gbps
- Back End serial optical link: Router →USA15, 4.8 Gbps

The sTGC Router Prototype

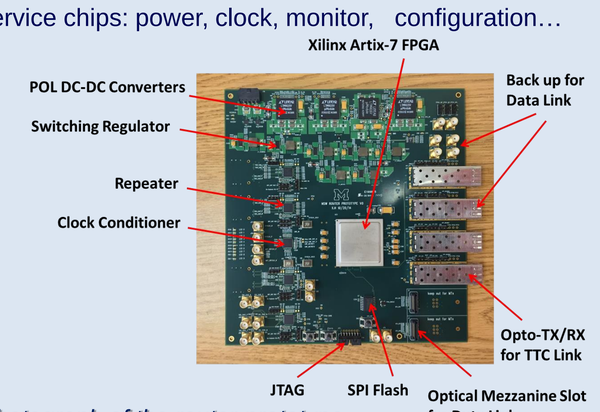




Router Func. Diagram

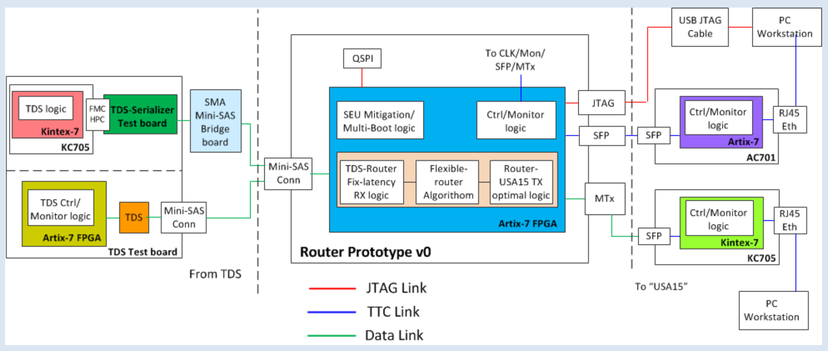
Block Diagram of Router

- Input connector: 3M 36pos MiniSAS
- Repeater: compensate for signal loss in 3m~4m transmission
- ***Data processing***: Artix-7 FPGA (**XC7A200T-FBG1156)**
- Optical transmitter: MTx (SMU)
- Service chips: power, clock, monitor, configuration…



Photograph of the router prototype

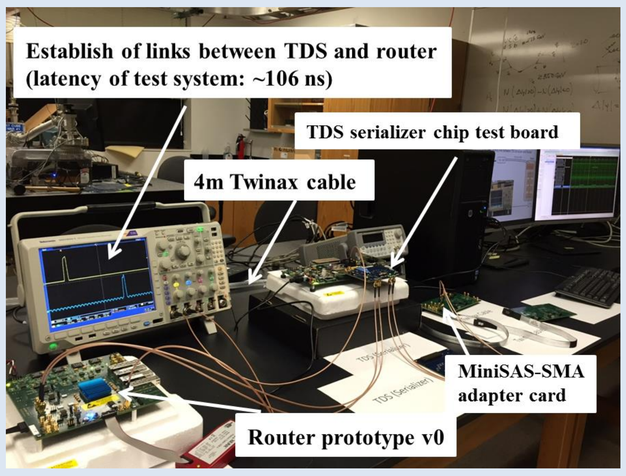
sTGC Router Prototype Function Testing

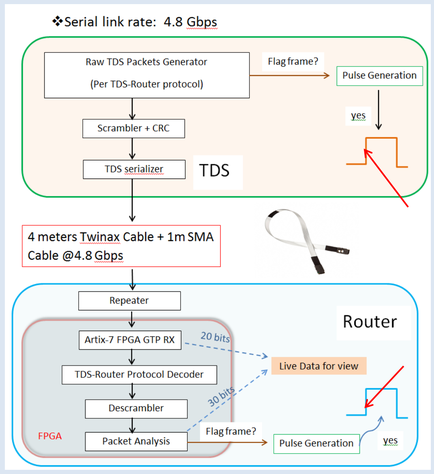


Router Prototype Test Setup

- All service blocks : power supply scheme, repeaters, clock distribution… ✓
- Artix-7 FPGA basic function: power-on sequence, JTAG, GTP IBERT ✓
- TDS-Router Link Test ✓

Router Prototype Lab Test picture





Latency showed on scope: rising edge to rising edge

- Optimal GTP RX logic + Sync. Buffer + Cutting-through switching algorithm: tested with TDS current data format
- **Latency of TDS-Router link is tested (Total ~106ns)**
  - TDS end ~22ns
  - Cable total length 5m (4m Twinax + 1m SMA)~25ns
  - Reading time ~6.25ns
  - Router optimal RX + Sync. Buffer + Cutting-through ~ 53ns (matched with latency estimation)

sTGC Router Prototype – Repeater TID Radiation Test

Repeater TID Co-60 γ radiation test setup

Repeater @ BNL Co-60 source location

TID for electronics on the rim of NSW : 78 kRad (safety factor: 30)

- **Repeater Total Ionizing Dose test system**
  - Firmware
    - MicroBlaze (MB) soft processor + Ethernet
    - "Bridge" logic: communicate between fabric logic & MB embedded system
    - Fabric logic: PRBS-31 Generator + PRBS-31 Checker + GTX (4 channels)
  - Software GUI: show/save all the key info during the test

Repeater DS100BR410	#1	#2
Test Time/hour	~25	~47 + ~24
Test Dose Rate/hour	5 *kRad(Si)*	5 *kRad(Si)* + 40 *kRad(Si)*
Total Dose/*kRad(Si)*	**~125**	**~1100**
Chip states	functional	functional
4.8Gbps data link	No error	No error

Repeater TID test summary

Power consumption of DS100BR410 sample #2 extended ~1.1*MRad(Si)* TID irradiation test

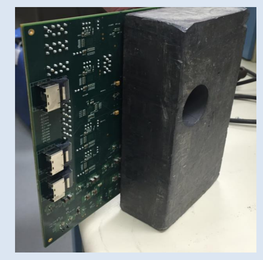
Power consumption of both DS100BR410 samples during the first period of ~125*kRad(Si)* TID irradiation test

Sample #1 and sample #2 track each other well

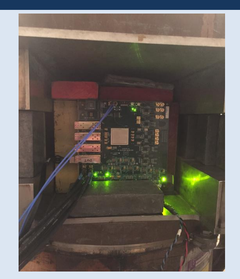
sTGC Router Prototype – Artix-7 FPGA Radiation Test

- **Artix-7 FPGA TID Test**
  - Monitor PRBS-31 data link @ 4.8Gbps
  - Get voltage/current info from LTC2991 and send out via SFP
  - DAQ Firmware
    - MicroBlaze (MB) soft processor + Ethernet
    - Fabric logic: PRBS-31 Generator + PRBS-31 Checker + GTP (3 channels)
    - Control & error information: 8b/10b encoder

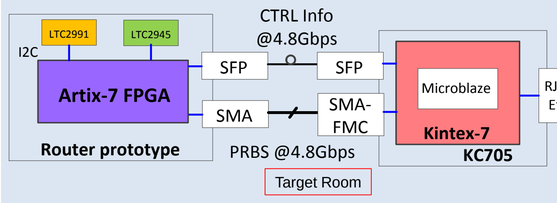
TID for electronics on the rim of NSW : 78 kRad (safety factor: 30)



Router board shielded with lead block except FPGA



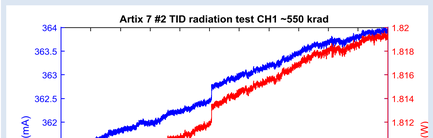
Artix-7 FPGA @ BNL Co-60 source location



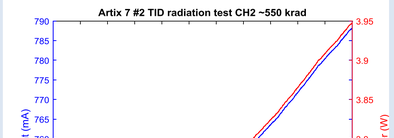
Artix-7 FPGA	#1	#2
Test Time/hour	~20	~55
Test Dose Rate/hour	~10 *kRad(Si)*	~10 *kRad(Si)*
Total Dose/*kRad(Si)*	**~200**	**~550**
Chip states	functional	functional
Current&power	normal	normal
4.8Gbps data link	No error	No error

Artix-7 FPGA TID Co-60 γ radiation test setup

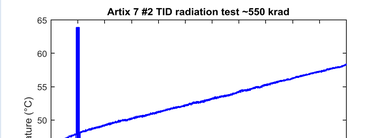
Artix-7 FPGA TID test summary



Current & Power consumption of router #2 Input CH 1~550k*Rad(Si)* TID irradiation test



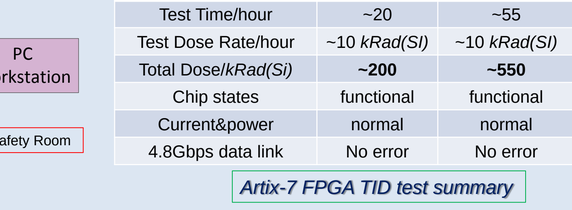
Current & Power consumption of router #2 Input CH 2~550k*Rad(Si)* TID irradiation test



Temperature of router #2 Artix-7 FPGA ~550k*Rad(Si)* TID irradiation test

- **Artix-7 FPGA Single Event Effects test**
  - Test at the Los Alamos Neutron Science Center (LANSCE): Oct. 27th ~ Oct. 31th
  - Neutron Beam: max 800MeV, 2" collimator
  - Flux:1.25 x 10^{11} neutrons/cm^2/day

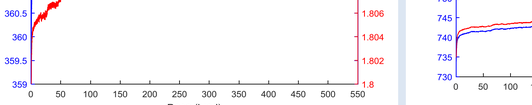
Artix-7 FPGA SEE test setup I



Artix-7 FPGA SEE test setup II

❑ Test Setup I

- Router & TDS-SER board & KC705
- 2 channels optimal GTP "RX" logic
- Cutting-through switching algorithm (TMR)
- Scrubbing logic: SEM repair
- Multi-boot: dynamic fully reconfiguration
- SFP: send out control information



❑ Test Setup II

- Router & KC705
- PRBS-31 data generator @4.8Gpbs
- 3 channels optimal GTP "RX" logic
- 3 channels optimal GTP "TX" logic
- PRBS-31 data checker @4.8Gpbs
- Scrubbing logic: SEM repair
- Multi-boot: dynamic fully reconfiguration

❑ DAQ for Test Setup I & II

- MicroBlaze soft processor + Ethernet
- MATLAB GUI

Summary:

The signal packet router board serves as a very fast switching-yard between incoming active TDS signals and a limited number of optoelectronic outputs. The design and different tests of fist router prototype version are presented. More radiation tests will be performed to measure SEU cross section.