The FTK to Level-2 Interface Card (FLIC)

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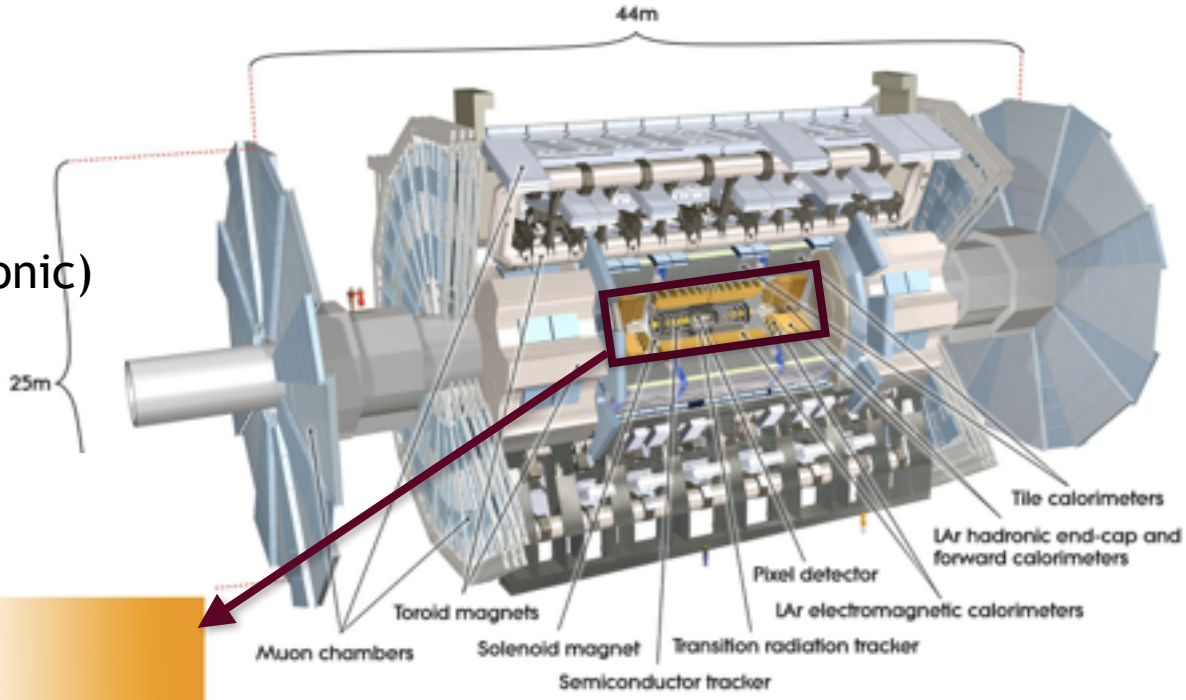
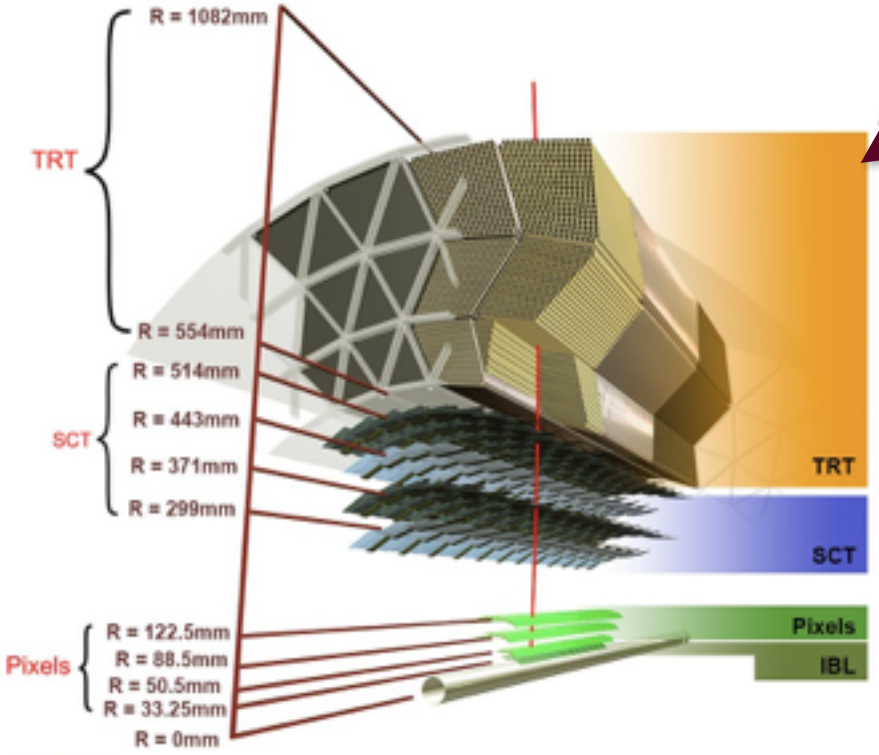
Outline

- Introduction to ATLAS, TDAQ and Fast Tracker(FTK)
- Level-2 Interface Crate (FLIC)
  - Functionality and design
  - Data processing, control and monitoring
  - Performance
- Summary

ATLAS detector

- Inner detector
- Calorimeter
  (Electromagnetic + Hadronic)
- Muon detector

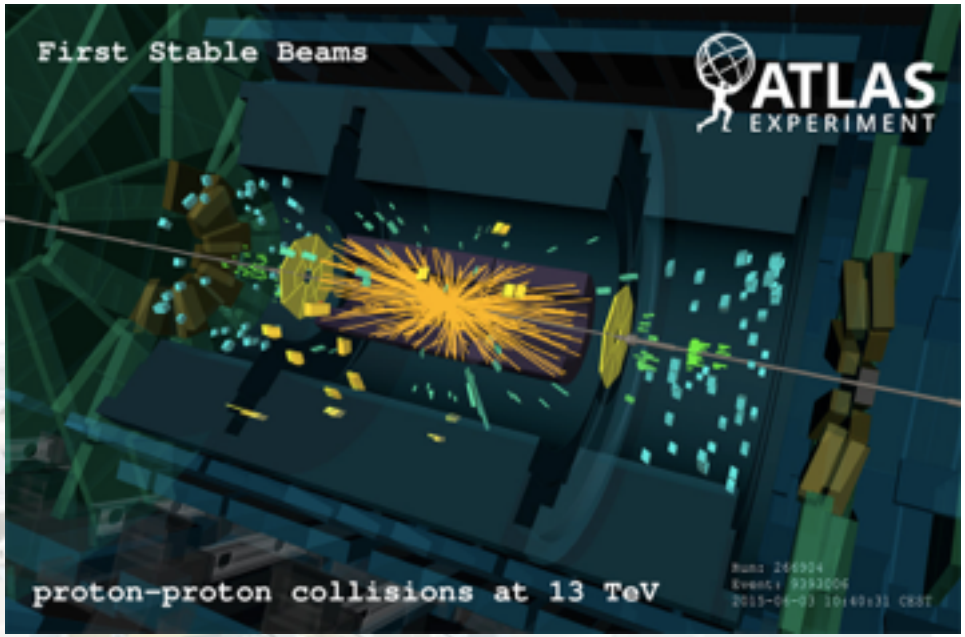


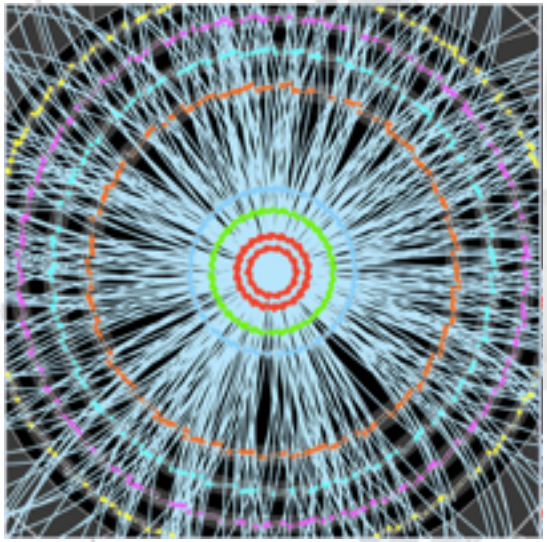


- Inner detector
  - Insertable B-Layer (IBL)
  - Pixel detector (Pixel)
  - Semiconductor tracker (SCT)
  - Transition radiation tracker (TRT)

Silicon detectors

ATLAS TDAQ





Tracks

40 MHz

All hits in IBL, Pixel and SCT

Level 1

100 kHz

p_T > 1 GeV

FTK

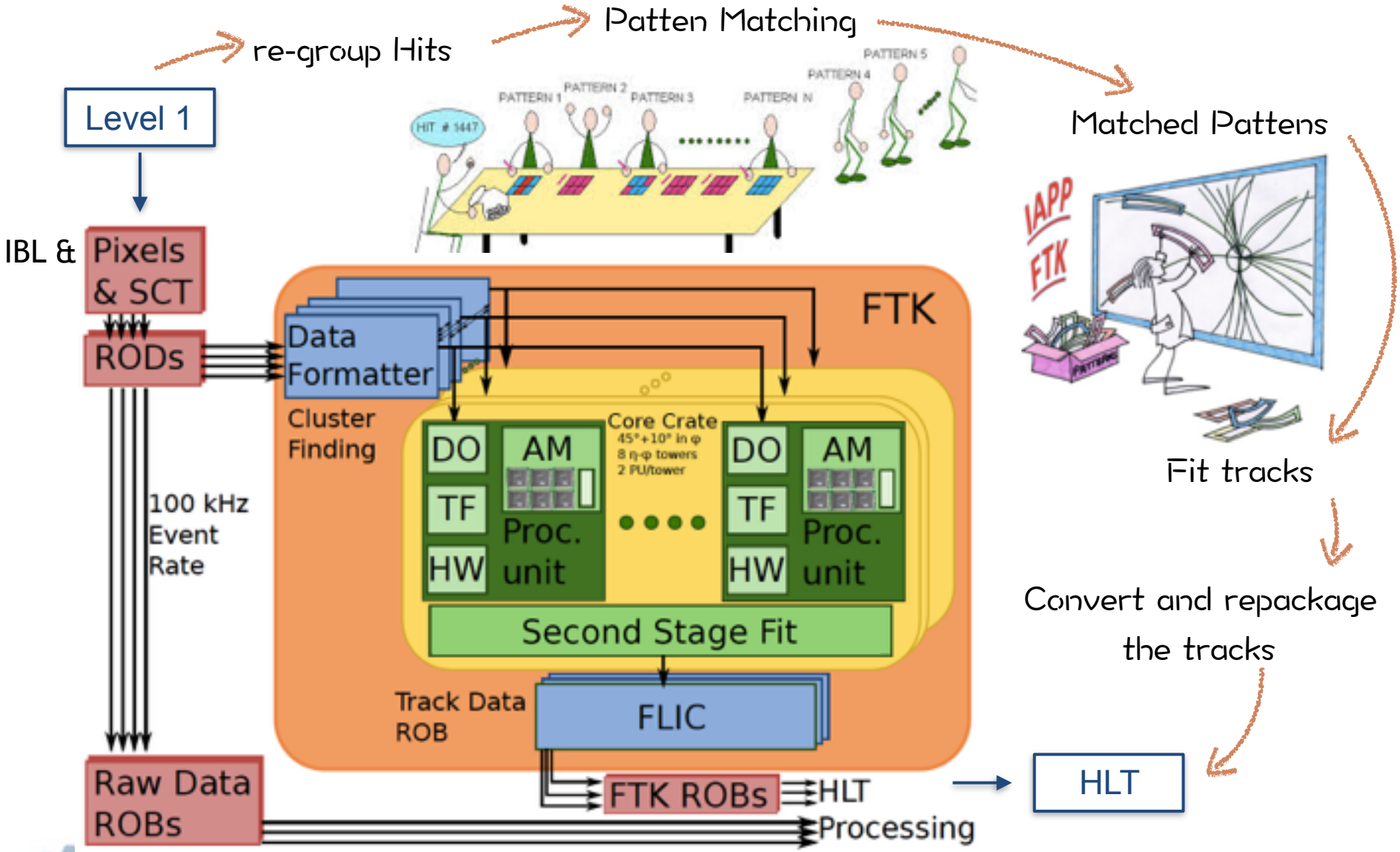
HLT

100 kHz

~1000 Hz

Level 1 – Level 1 Trigger, HLT – High Level Trigger

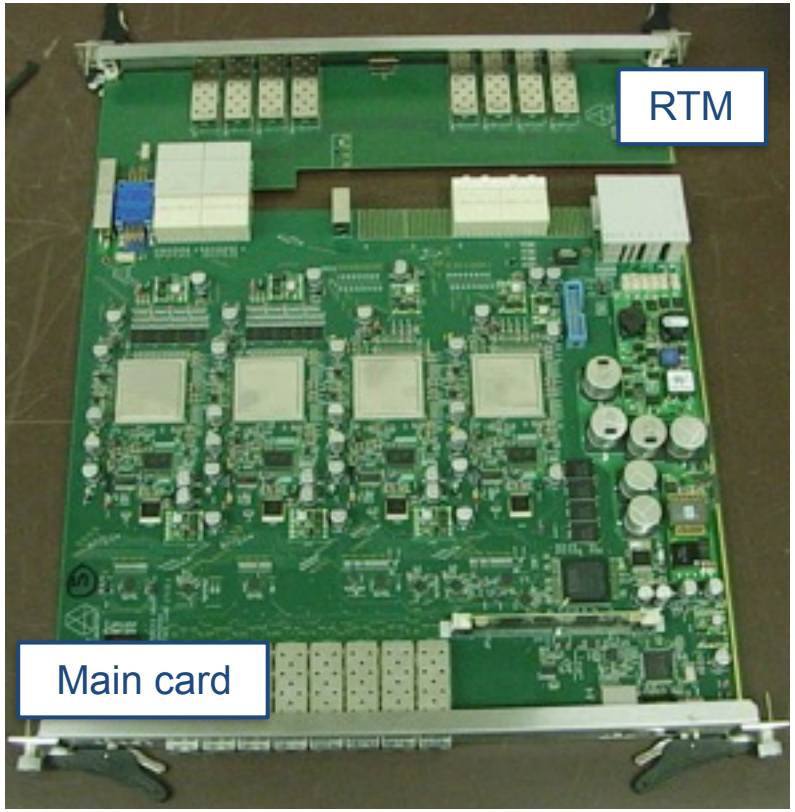
Fast TracKer (FTK)



FTK Level-2 Interface Crate (FLIC)

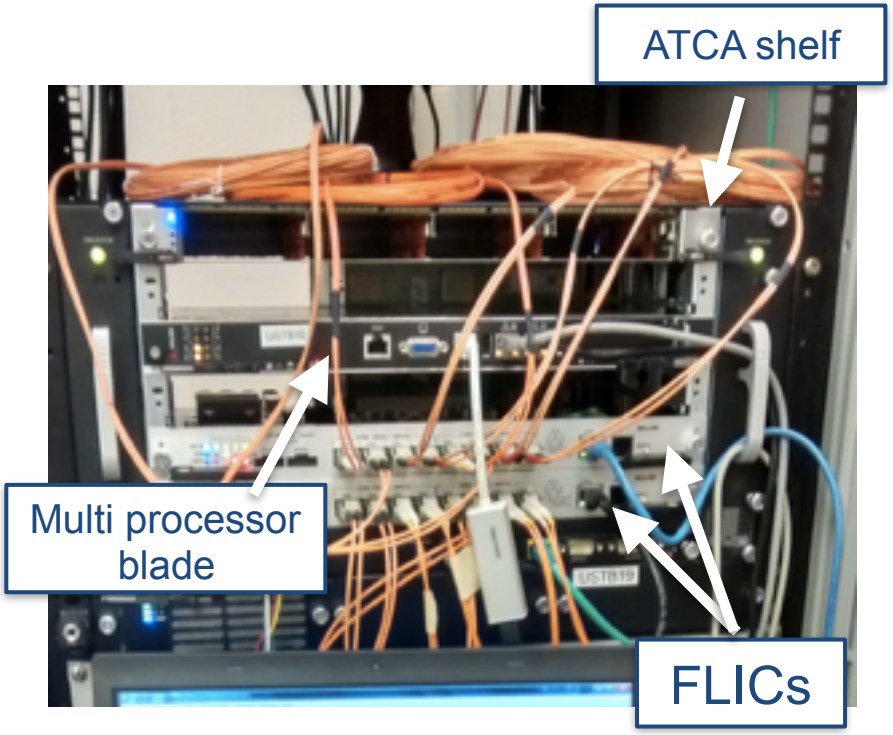
- FLIC is the final component of the FTK
- Receive event records from upstream FTK system, 1/16th of the detector per channel
  - Full bandwidth output from the FLIC to HLT
    - Baseline: 300 tracks per event @ 100 kHz
- Convert FTK identifiers to ATLAS global identifiers using SRAM lookup
- Repackage event record into standard ATLAS format
- Communicate with HLT
  - Sends records
  - receives xoff signal and propagates it upstream to FTK
- Monitoring and Processing on ATCA Blades via backplane

RTM — Rear Transition Module



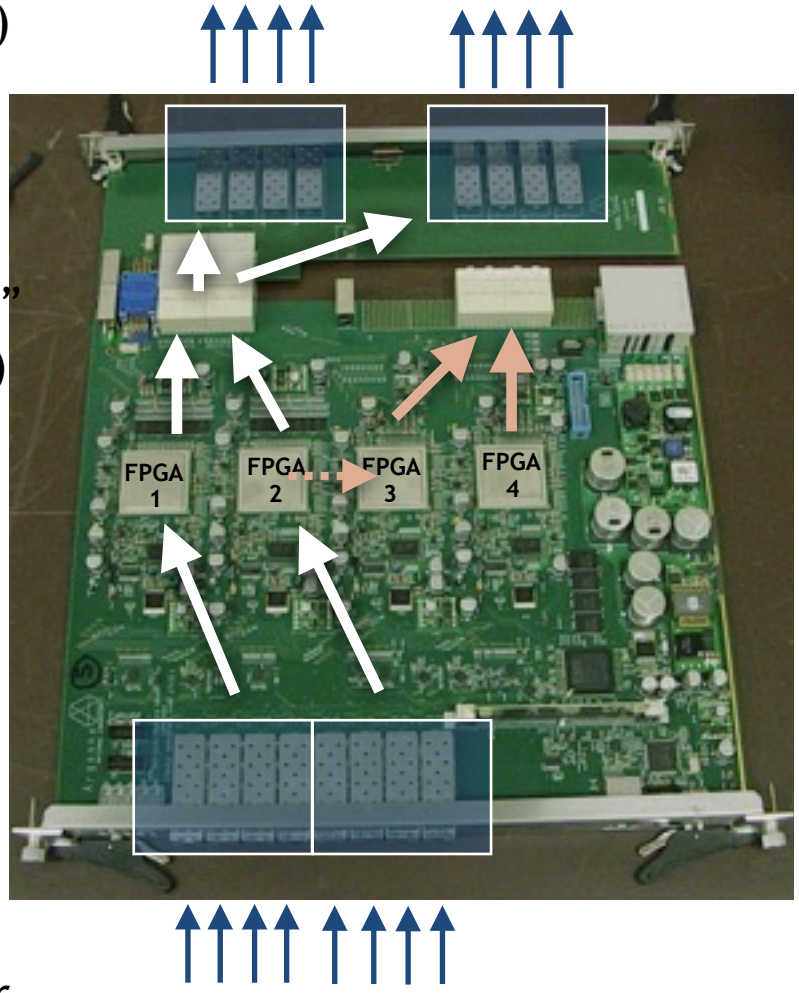
ATCA

- Advanced Telecommunication Computing Architecture (ATCA) for data acquisition
  - Each FLIC implements four 10 Gb Ethernet channels
  - Allows for data distribution to up to four commercial processor blades
  - For trigger processing and complex data quality monitoring
    - ATCA shelf allows data from either FLIC to any blade
  - Data transfer to blades occurs in parallel with flow-through data processing



Hardware design

- 18-layer circuit board, standard FR-4
- 2 Virtex-6 FPGAs as the data processor (1&2)
  - Each has 128 Mbit of fast SRAM (32 Mbit per SFP input) to implement data-driven lookup tables
  - Track geometry data from the lookup table are inserted into the data stream “on the fly”
- 2 Virtex-6 FPGAs as the ATCA interface (3&4)
  - Each implements two 10Gb Ethernet interfaces to ATCA backplane (total 40Gb output bandwidth)
  - Each has 8 SERDES links of input from I/O processor FPGAs, matched to total ATCA output bandwidth
  - Distribute data, from the FLIC to the multiple processor blades
- Full, matched-bandwidth internal mesh of SERDES links between all FPGAs
- General-purpose DDR3 memory per FPGA for buffering or event record building



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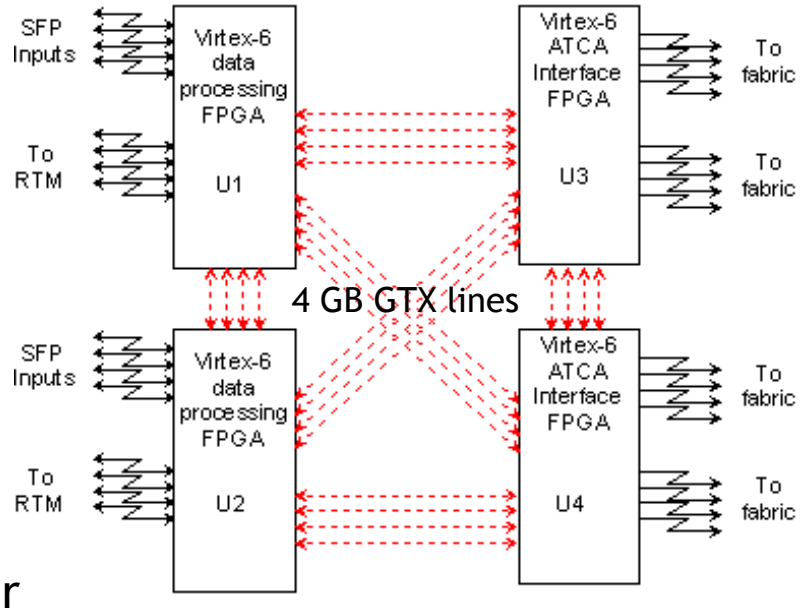
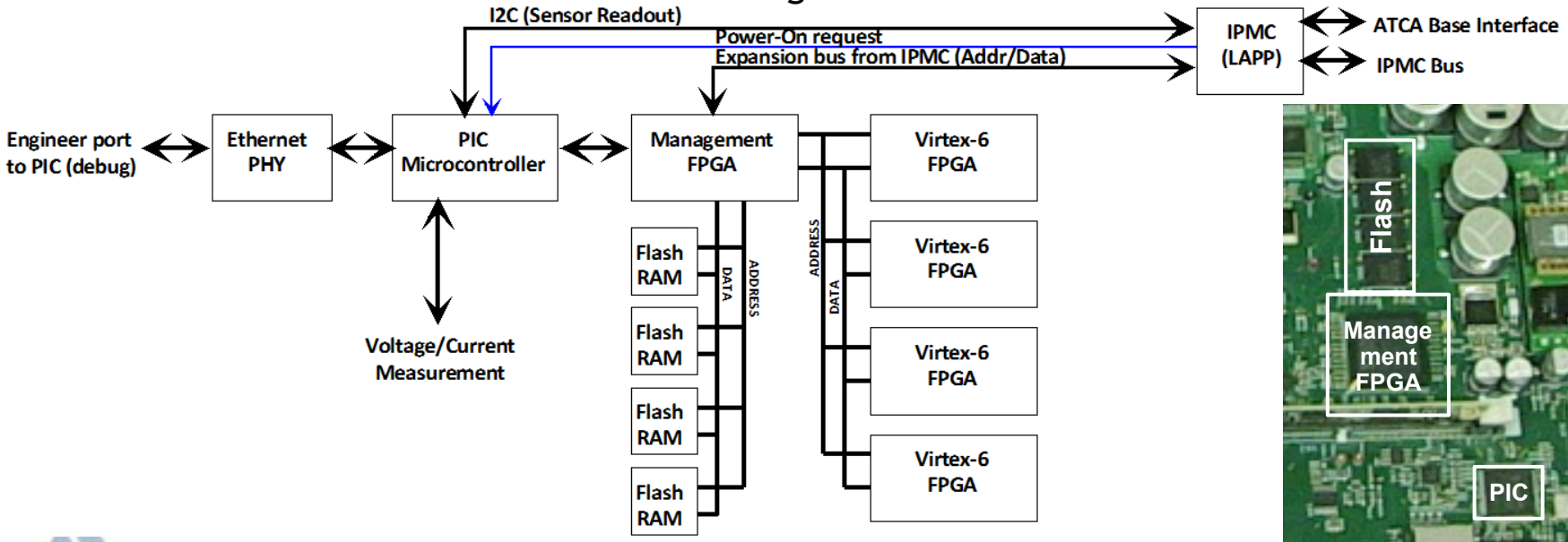


Slow control

All communication is done through the management area

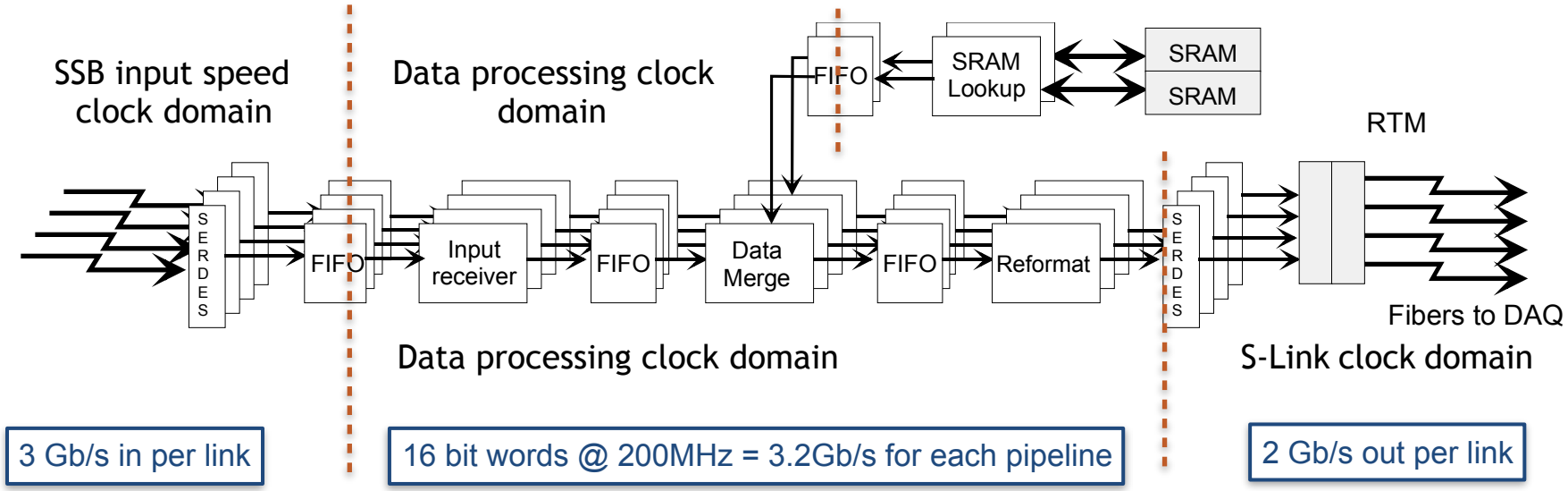
- Microcontroller (PIC)
  - Ethernet port in the front panel
  - FPGA voltage, current and temperature monitoring
- LAPP IPMC
  - Power control and sensor monitoring though PIC
  - Communicate to the Shelf Manager
- Management FPGA (Spartan-3 FGPA)
  - Main FPGA configuration and monitoring
  - Flash RAMs (4*128 MB) -> non-volatile FPGA image storage for 4 main FPGAs + non-volatile storage of SRAM lookup table values



Data processing

Multiple state machines at different speeds, decoupled by FIFOs

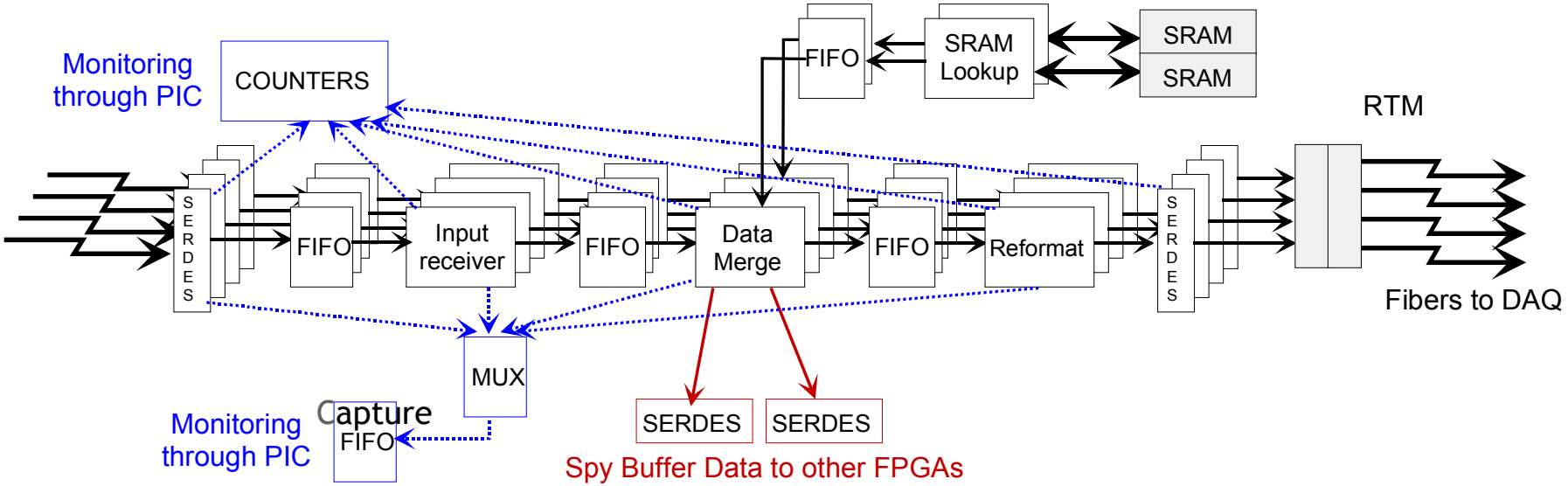
- Data received from front panel SFP's is immediately buffered
- Internal processing clock is faster than front SFP word clock, no potential for overflow
- On-the-fly lookup of detector global ID for each track from external SRAM, based upon indices in input data
- Merged with input data to create base output format



- Merged data is reformatted following ATLAS TDAQ specification and sent out via RTM

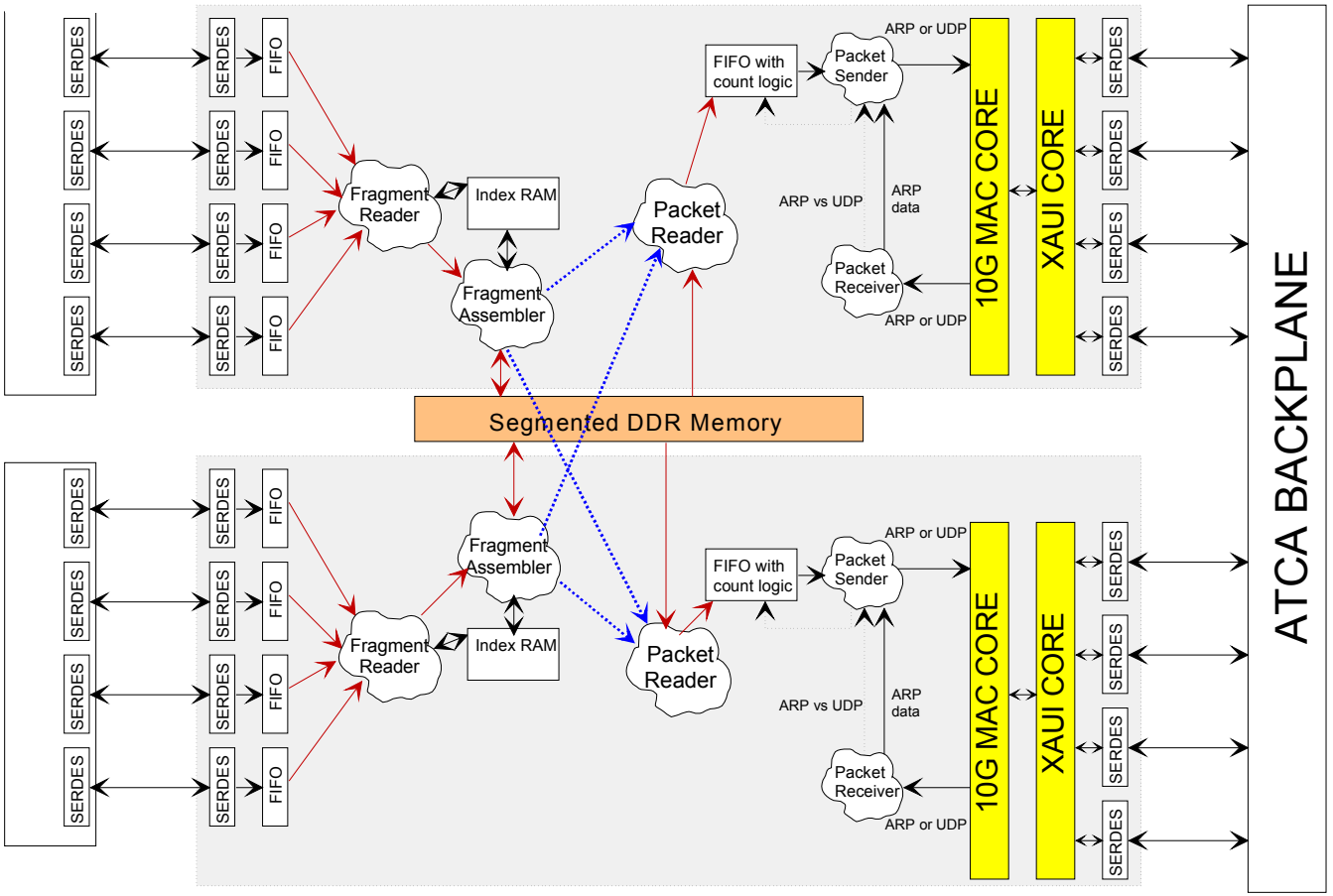
Control and monitoring

- Flow Control
  - XON/XOFF messages sent back to upstream
  - Based upon internal states or XON/XOFF from HLT
- Monitoring of the data processing
  - Counters for number of events and event size at each stage of the data processing
  - Copy the event record in each state machines to the capture FIFO
    - Detailed check on the format change of the record
  - Separated for the four pipelines



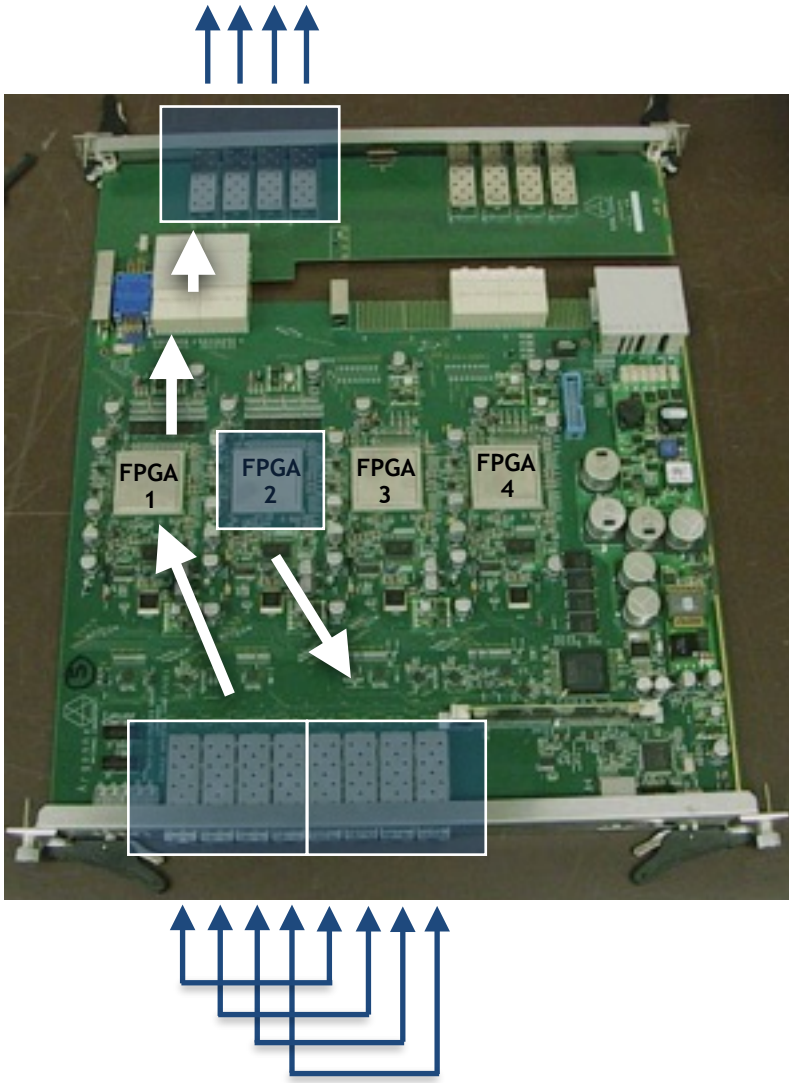
Firmware for control and monitoring

- Spy buffer
  - Select event, copy to the ATCA interface FPGAs though the internal mesh
  - Assemble the received fragments, form Ethernet packets, then send to processing blade through the ATCA backplane



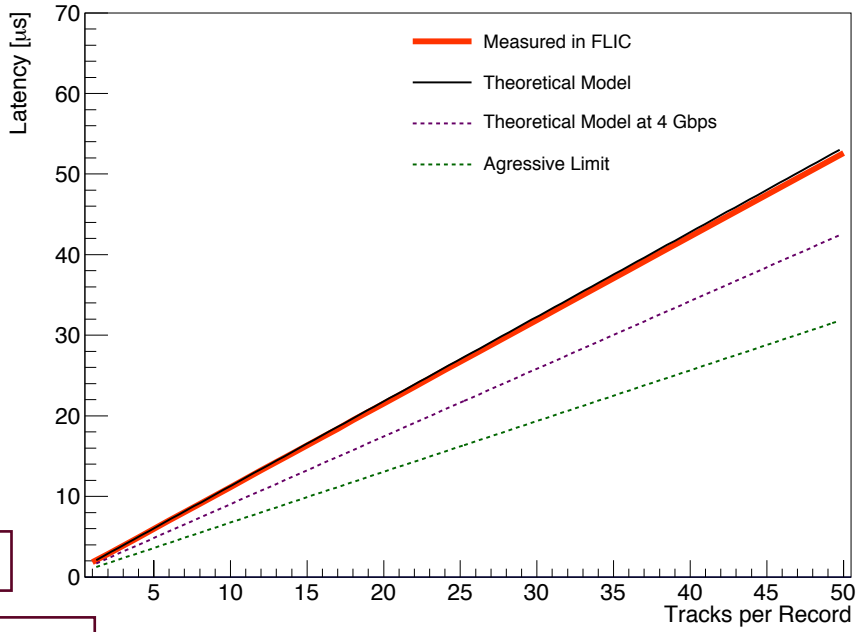
Data stream testing

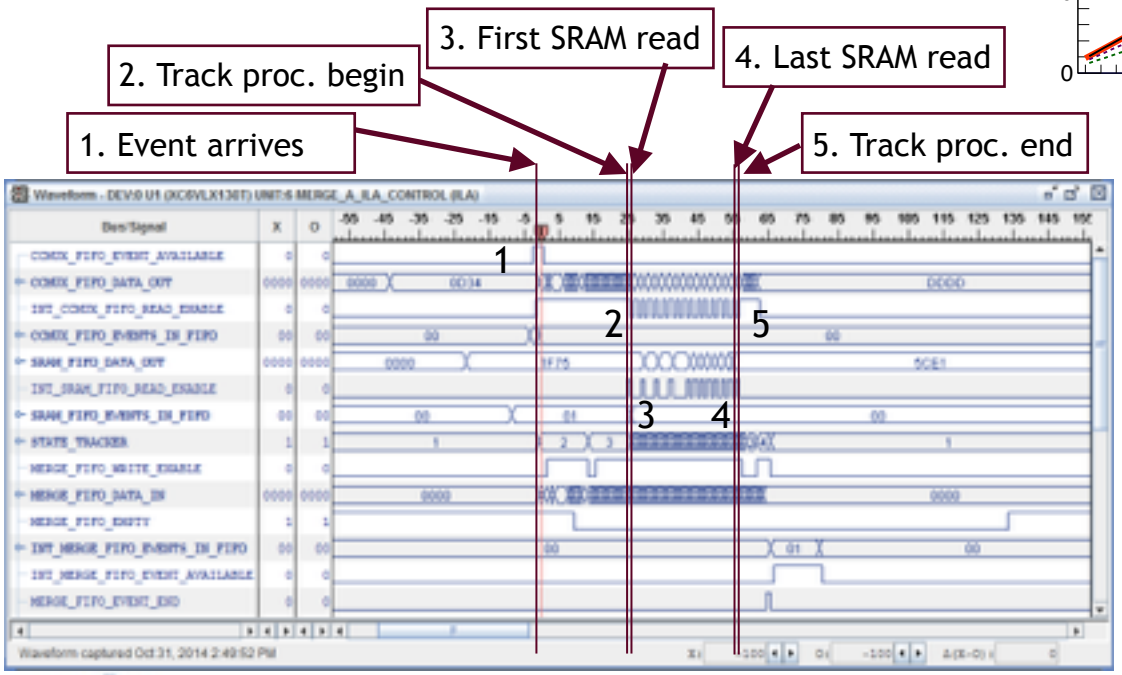
- Upstream FTK Data Emulator
  - Eg. use FPGA 2 as emulator
  - Special firmware for emulation
  - Pseudo random data generated and out from front panel SFPs
- Data processing
  - In this case, FPGA 1 is used as normal data processor
  - Received generated data from front SFPs, process them, send out from RTM S-Links
- Output to HLT



Performance - Data processing in board

- Event processing inside the FLIC is monitored using Chipscope
  - Time used for processing of each track takes 160 ns
  - The SRAM look-up takes a maximum of 139 ns for all 12 silicon layers



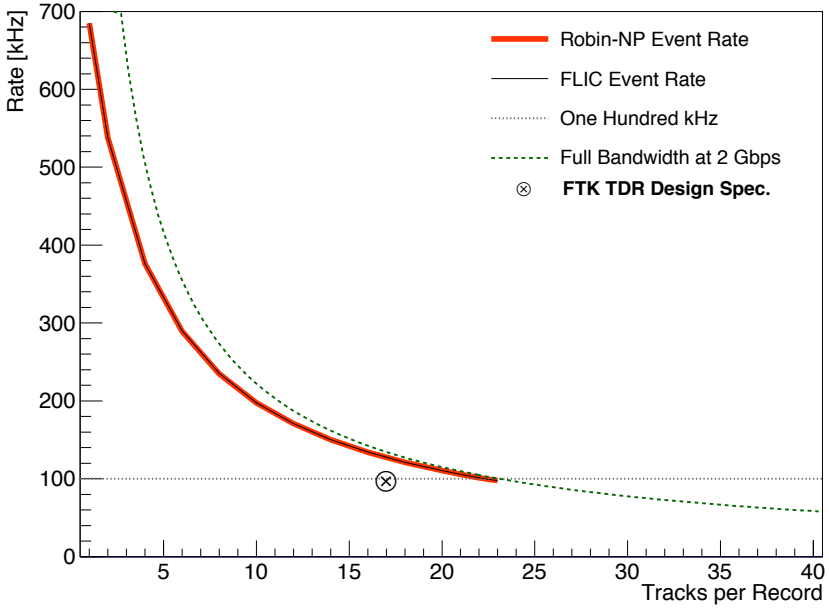


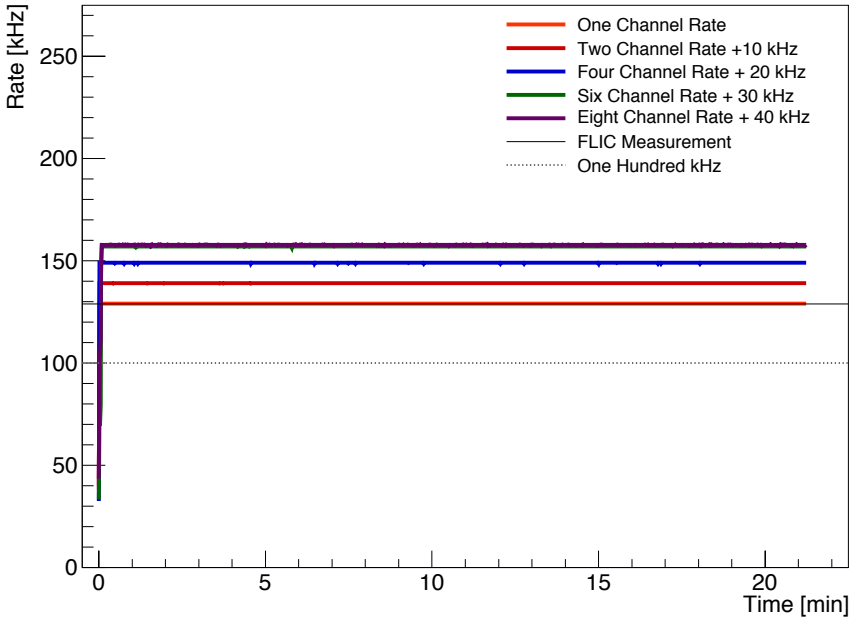
- Measure the delay between first word written to last word read out for a single record
  - Function of number of tracks
- Latency under control and well understood
  - Driven by data expansion
- SRAM Look up not a bottleneck

Performance - Event sending to HLT

- FLIC sending constant bandwidth to HLT
  - Size of event record varies with number of tracks
- Sending 200 MB/s of data to HLT using one channel
- Running above design spec, no limitation on the total data rate of the FTK system

- Full system test running at design specification
  - Running above 100 kHz
  - Testing with constant event record size to the HLT
  - No effect from parallel channels





Summary

- The FLIC, an interface to High Level Trigger of the experiment built with desired functionality
  - Data dispatching to HLT with geometry description conversion
  - Data monitoring and processing on ACTA blades
- The FLIC has been extensively tested and meets all the specifications
  - Event processing in the board
  - Event sending to the HLT
- Next step -> production board implementation at ATLAS

Looking forward to the first event sent from the FTK though FLIC to HLT!