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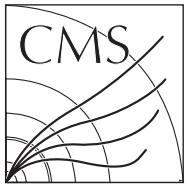

The Compact Muon Solenoid Experiment

Conference Report

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Commissioning of the Upgraded CSC Endcap Muon Port Cards at CMS

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Abstract

We report on the status of commissioning of the upgraded Muon Port Cards in the Level 1 Trigger electronic system serving the Endcap Cathode Strip Chamber (CSC) sub-detector at the CMS experiment at CERN. After presenting an overview of the existing system and upgrade requirements, we describe the new Muon Port Card FPGA mezzanine and its firmware developed to drive the new 3.2Gbps optical links. Results of initial tests with the existing and upgraded CSC Track Finder boards and further plans are given in the concluding sections.

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Commissioning of the Upgraded CSC Endcap Muon Port Cards at CMS

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ABSTRACT: There are 180 1.6Gbps optical links from 60 Muon Port Cards (MPC) to the Cathode Strip Chamber Track Finder (CSCTF) in the original system. Before the upgrade the MPC was able to provide up to three trigger primitives from a cluster of nine CSC chambers to the Level 1 CSCTF. With an LHC luminosity increase to 10^{35} $cm^{-2}s^{-1}$ at full energy of 7TeV/beam, the simulation studies suggest that we can expect 2..3 times more trigger primitives per bunch crossing from the front-end electronics. To comply with this requirement, the MPC, CSCTF, and optical cables need to be upgraded. The upgraded MPC allows transmission of all the 18 trigger primitives from the peripheral crate. This feature would allow searches for physics signatures of muon jets that require more trigger primitives per trigger sector. At the same time, it is very desirable to preserve all the old optical links for compatibility with the older Track Finder during transition period at the beginning of Run 2. Installation of the upgraded MPC boards and the new optical cables has been completed at the CMS detector in the summer of 2014. We describe the final design of the new MPC mezzanine FPGA, its firmware, and results of tests in laboratory and in situ with the old and new CSCTF boards.

KEYWORDS: Trigger concepts and systems (hardware and software); Optical detector readout concepts; Trigger algorithms

Contents

1. Introduction

After completion of the major upgrade which took place from 2012 to 2014 the CMS Endcap Cathode Strip Chambers (CSC) system [1] comprises 540 chambers located in the Underground Experimental Cavern (UXC) of the detector, with four layers (or "stations") of chambers in each endcap. The Level 1 CSC Trigger system includes the following components:

- Cathode and Anode Front-End electronics mounted directly on CSC chambers in the UXC area;
- Peripheral electronics housed in sixty 9Ux400 mm crates on the periphery of the return yokes of CMS, also in the UXC area: these electronics are the Trigger Motherboards (TMB), Muon Port Card (MPC), Clock and Control Board (CCB);
- The Track Finder (TF) crate in the CMS Underground Support Cavern (USC) with 12 Sector Processors (SP), one CCB and one Muon Sorter (MS) board.

The TMB produces two combined anode and cathode trigger primitives called Local Charged Tracks (LCT) and transmits them to the MPC via the custom peripheral backplane. Each LCT is represented by a 32-bit word that contains the anode and cathode hit coordinate and pattern type, as well as a trigger primitive quality. The MPC selects the three best primitives out of 18 based on quality value and transmits them to the SP via the optical links at 1.6Gbps. Each SP serves a 60 degree sector in each endcap, so there are 12 SP boards in the TF crate (Fig.1). Each SP reconstructs up to three tracks. They are transmitted to a final stage of the CSC trigger, the MS board via the custom TF backplane. The MS selects the four best CSC trigger tracks out of 36 and transmits them via four copper links to the CMS Global Muon Trigger crate, where they are combined with the Drift Tube (DT) and Resistive Plate Chambers (RPC) muon candidates.

The initial implementation described above has been in operation since 2009 and provided satisfactory performance for Run 1 of the LHC. However, in order to accommodate the increase in energy and luminosity in Run 2 after the LHC upgrade, the Level 1 hardware needs to be

significantly modified. Additionally, before the upgrade, only 15 pre-selected trigger primitives out of 90 were sent from 5 MPC boards to a respective SP in each 60 degree trigger sector. This reduces the efficiency for events with multiple muons in a small geometrical region and may lead to inefficiency in very high pile-up conditions [2]. Thus, the main goal was to modify the MPC in such a way that it provides all the 18 LCTs to the upgraded SP while the link to the old CSCTF is still in operation. The new SP, called the MTF7, is designed at the University of Florida, based on a large and powerful Xilinx Virtex-7 FPGA and is implemented in the uTCA standard [3]. The new CSCTF occupies three uTCA crates (Fig.1) and will be running in parallel with the old Track Finder at the beginning of Run 2.

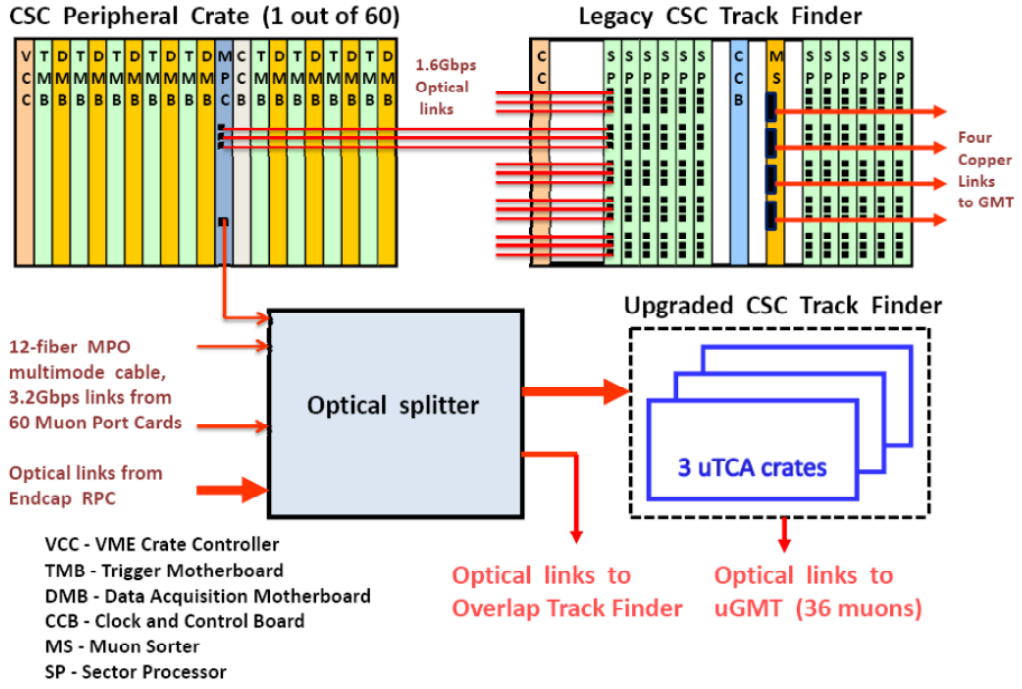

Figure 1: Block diagram of the upgraded CSC Level 1 trigger system

Each MTF7 board in the upgraded CSCTF must consider LCTs from the neighboring sector's chambers that overlap with its own sector in order to provide better track reconstruction on the sector's edge. It is sufficient for each MTF7 to consider overlapping chambers on only one side of the sector. To implement this requirement, the LCTs from chambers on the edge of each sector should be transmitted to two MTF7 boards simultaneously using the optical splitter shown on Fig.1.

Our initial results on the MPC upgrade design were presented in [4]. The main idea is to replace the older Virtex-E mezzanine card with a new one, comprising not only the higher performance FPGA, but also an optical transmitter. The 9U baseboard remains unchanged. The three old optical links previously located on the baseboard remain there, supported by the new FPGA. In 2013-2014 we completed the final design, production and tests of all new mezzanines. Below we provide more details about the functionality of the new board, various

tests we have performed, and our experience with the installation and commissioning at the CMS in late 2014-early 2015.

2. Spartan-6 FPGA Mezzanine and Optical Transmitter

The Spartan-6 FPGA was chosen for several reasons. First, the GTP transceivers support transmission rate up to 3.75Gbps and the largest device has 8 such links; this is sufficient (after minor modifications in the present data format) to transmit all 18 LCTs. The largest 900-ball package has enough inputs and outputs to implement all the inter-board connections, and, of critical importance, they all are fully compatible with the 3.3V CMOS logic levels on the baseboard. The other advantages are low power consumption and low cost. The first prototype was designed in the fall of 2011 and extensively tested. It carried the XC6SLX150T-3FGG900C FPGA with two XCF32P PROMs and the SNAP12 plug-in transmitter card. The main clocks for the FPGA core logic and the GTP blocks are derived from the LHC 40.08MHz clock using the QPLL device with a dedicated 160.314MHz oscillator.

The firmware was modified to allow internal operation at 160MHz. The configuration time of 108ms to load the FPGA from PROMs is achievable with the external clock of 40MHz provided to the USERCLK pin of the FPGA from an external oscillator. It takes ~20 minutes to program the compressed svf file of ~68MB into two XCF32P PROMs via the VME bus to upgrade the firmware remotely, when needed.

The production mezzanine was designed in 2013 and had very few minor changes (Fig.2). The optical transmitter board however has been redesigned to accommodate more reliable connector (Samtec QSS-025-01-L-D-A) and a pluggable Avago AFBR-810 transmitter instead of the SNAP12 device (the Avago part is not pin compatible with the SNAP12 standard). The MTF7 optical receiver is based on an Avago AFBR-820 counterpart.

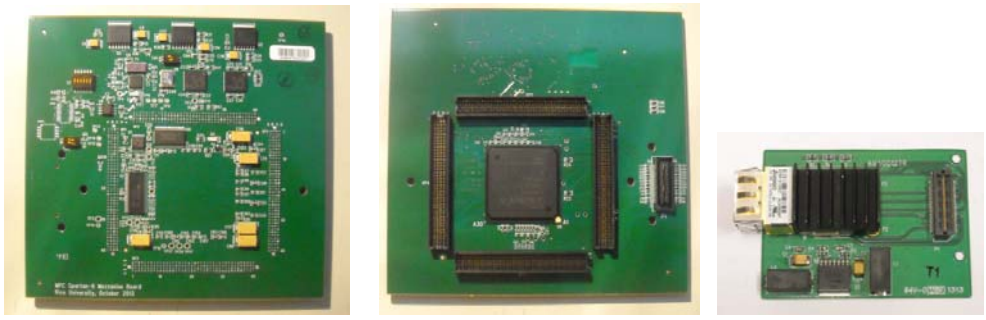

Figure 2: Top and bottom views of the new Spartan-6 FPGA mezzanine board (left and middle) and pluggable optical transmitter (right)

85 mezzanines and 85 optical boards have been fabricated and tested in early 2014. The only, but major, problem at this step was that on almost half of mezzanines the QPLL didn't produce correct clock outputs or didn't lock to its input clock. The problem was traced back to QPLL crystals which, apparently, were damaged during assembly at the factory. 42 crystals out of 85 were replaced manually in our lab and all replacements worked well without any issues. We didn't proceed with the further failure analysis due to its excessive cost.

3. Optical Cables and Optical Power Budget

The new optical path is based on trunk cables. The trunk cable is constituted by 48 multimode (50/125 um, OM3) optical fibers, bundled into 4 cords terminated with MPO (female type) connectors on both sides (Fig.3). The operation wavelength is 850 nm. The length of fan-out cords is L2=1.1m. On the UXC side they are connected directly to the MPC front panel. There is a short (~30 cm) pigtail cable from the front panel to the Avago transmitter (Fig.4). On the USC end they are connected to a patch panel. The lengths of trunk cables L1 vary from 63 to 117 meters, depending on the CSC station and endcap.

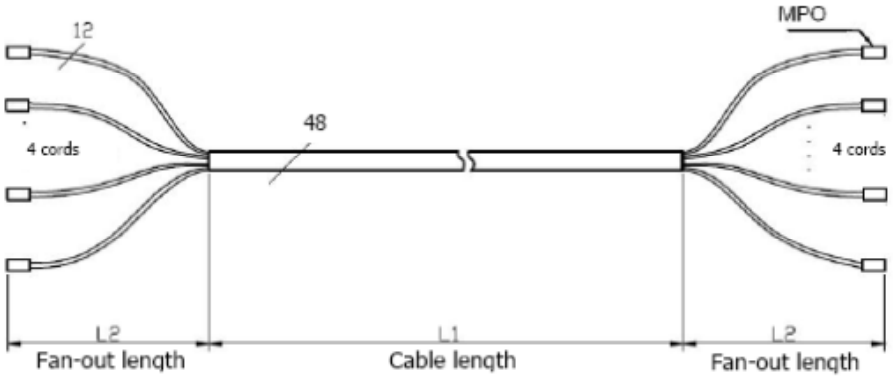

Figure 3: Optical trunk cable used for CSC Level 1 Trigger system

The cable diameter is below 15 mm. The cable material composition is halogen free and frame retardant in accordance with the CERN safety instructions. The trunk cables were assembled with pulling sleeves at both ends to protect the connectors during the installation process. On both sides of the cable, the fan-out was defined staggered in pairs to avoid having 4 connectors terminated at the same point and consequently reducing the volume inside the pulling sleeve. Two samples of the trunk cable were analyzed by CMS experts to validate the cable characteristics and performance. The cable passed all tests and the order for the total quantity was placed through a CERN contract. All 36 cables were tested before installation. Installation took several weeks and was done by a CERN crew.

To calculate the worst-case estimate of power budget (PB), one needs to subtract the minimum receiver sensitivity (PR) from the transmitter power (PT): PB = PT-PR. For the Avago AFBR-810 transmitter and AFBR-820 receiver at 3.2Gbps PB = -1.5dB-(-13dB) = 11.5dB.

After calculating a link's power budget one can calculate the power margin (PM), which represents the amount of power available after subtracting attenuation or link loss (LL) from the power budget (PB). The average LL values are 0.5dB for connector/splice; 3dB for a 2-way splitter; 6dB for a 4-way splitter; higher-order loss in MMF of 0.5dB; fiber attenuation of 1dB/km. Assuming 6 connectors/splices and one 4-way splitter in our link, the estimate is:

PM = PB-LL = 11.5dB - 0.5dB – 6x0.5dB – 6dB - 0.1dB (100 m fiber) = 1.9dB

A PM greater than zero indicates that the power budget is sufficient to operate the receiver.

4. Irradiation and Production Tests

Requirements and effects of radiation on electronic components in the CSC Endcap system are discussed in detail in [5]. Here we will discuss only the tests related to two critical components on the upgraded MPC: the PROM and FPGA. The XCF32P PROM was irradiated with 1 MeV equivalent fluence at ~10.5×10^{12} neutron/cm^2 at the TAMU cyclotron (College Station, TX USA) in April 2013. It was equivalent to ~30kRad, or 30 years of LHC exposure in the area where the inner ME1/1 chambers are located. The content of the device was read back and found intact, as expected.

The Spartan-6 XC6SLX150T FPGA was irradiated at the UC Davis 66 MeV proton synchrotron in April 2013. Initially, the device was irradiated with 1kRad at a rate of 1 Rad/sec, that is convenient to detect Single Event Upsets (SEU). The average time between SEU was from 5 to 15 seconds and average dose to get an error ~13 Rad. With the accumulated fluence of 3×10^{11} protons/cm^2, the cross section of SEU is 2.5×10^{-9} cm^2. Assuming 10-year fluence of neutrons with energy E>100 KeV of ~10^{11} cm^{-2} [6] at full LHC design luminosity in the area where the MPC is located, the worst case SEU rate would be 5×10^{-6}, or one SEU in approximately 55 hours. We also irradiated the FPGA with 100 kRad at a rate of 360Rad/s which is much higher than anticipated in our area. There were many upsets, but the device survived the test and was still functional. The other active parts, including the Avago AFBR810 transmitter, were tested earlier [5] or by other groups and found in agreement with our requirements.

All new mezzanines, coupled with pluggable optical transmitters, passed initial data transmission tests at Rice in spring of 2014. All old and new optical links were tested. Test software allows injection of pseudo-random bit stream (PRBS) and random patterns from the transmitter and their verification on a receiver end. All the components are located in one VME crate. In the second half of 2014 we have assembled a more sophisticated test stand (Figs.4-5) with the uTCA crate and the MTF7 prototype on a receiver end and used software developed at the University of Florida for various data transmission tests.

Figure 4: Upgraded MPC baseboard (left) and a test stand at Rice University (right)

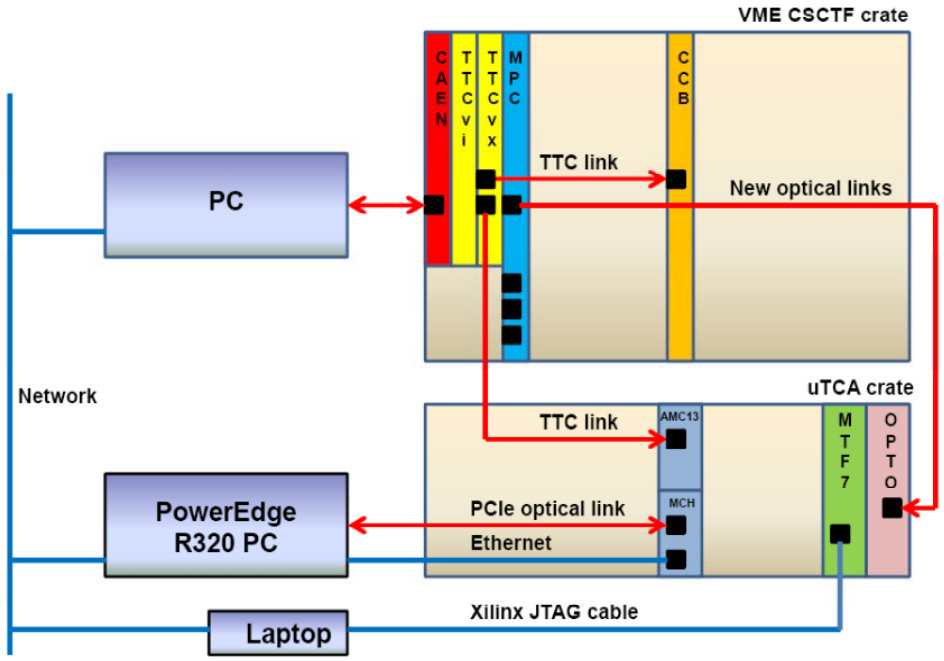

Figure 5: Block diagram of the uTCA-VME test stand at Rice

As previously mentioned, the MPC boards are located in the underground cavern, and are subject to radiation effects. They require, along with other electronic boards in this area, periodical (once every few minutes) reconfiguration from their PROMs to mitigate SEU. The CSCTF is located in the underground control room where the radiation effects are negligible and periodical reconfiguration is not required, so it was essential to test data transmission with periodical reconfiguration on the transmission side. We ran such a test with much higher frequency of "Hard Resets" (~1 Hz) and found that once every few hundred iterations (one iteration comprises transmission of 512 data frames at 3.2Gbps and their check from spy FIFO in the MTF7) there was data corruption in random optical channels and random bits. The effect was rare, but reproducible. We explain this corruption by unsynchronized clocks on both ends of the link. We applied a reset to GTH blocks on a receiver end after every reconfiguration on a transmission end and the problem went away.

5. Installation at CMS and Integration Tests

In addition to data transmission tests described in Section 4, every new mezzanine was tested in the fully loaded peripheral crate and data transmissions from 9 Trigger Motherboards and sorting logic were verified. In the first half of 2014 five upgraded MPC boards were installed at UXC and participated in several mid-week and global cosmic runs. At this step we were able to verify the timing of old optical links and make some minor modifications in the firmware to fully comply with existing timing settings.

The majority of mezzanines were replaced during a 2-week period in the summer of 2014. Since the detector operated in cosmic data taking at this time, a batch of few boards was taken

upstairs at a convenient time; mezzanines were replaced in the CMS laboratory space on the surface and then the upgraded boards were taken to the UXC hall for installation. The next batch was upgraded at a next opportunity and so on. The functionality of old links was confirmed within few days. The first prototype of the MTF7 Sector Processor was installed in the USC only later in summer, so the initial tests of new optical links were delayed until early September. All new optical cables were laid out by this time. Most of new links were validated within few days with PRBS patterns being sent from MPC boards and checked at the MTF7 receivers with a Xilinx IBERT software. We discovered two boards which didn't produce light on any new optical links. They were replaced and sent back to Rice for repair. Poor soldering on an optical transmitter was found on one of these boards; on another board a short pigtail fiber was replaced. Since the start of LHC Run 2 in the spring of 2015 all the legacy optical links operate properly. In summer of 2015, all the MTF7-based Sector Processors were installed at USC, new optical links connected using production patch panels, and data transmission tests with the PRBS patterns repeated. Few broken fibers were identified and replaced.

Online Data Quality Monitoring (DQM) plots are available for the legacy CSCTF. They provide cathode half-strip numbers and anode wire groups on a per chamber basis for each endcap and every CSC station; 36 plots in total. They are available to shifters and experts and allow to identify hardware related problems very quickly. Later they will be added for the upgraded CSCTF as well.

6. Conclusion

During the LHC shutdown in 2013-14 we have upgraded all the CSC Endcap Muon Port Cards with new Spartan-6 mezzanines and re-installed them in the experimental hall, along with the new optical cables to the upgraded CSCTF. The new firmware allows transmission all the trigger patterns to the new CSCTF simultaneously with the three "best" ones to the legacy CSCTF. Operation with cosmic triggers during several months in 2014-15 have validated all optical links. Based on initial data analysis, old optical links operate reliably; new links are being validated. Commissioning of the upgraded CSCTF is scheduled for early 2016.

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