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Ref: LAB II CO/Int./CC/74-2

THE SPS TIMING SYSTEM PROPOSAL

FINAL

by

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MAY 1974

SWITZERLAND

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ABSTRACT

This note describes the principles and design criteria of the timing system for the SPS. This includes the control philosophy and the command structure of the timing modules. The global timing transmission is discussed and the local interaction required at each auxiliary building is outlined. Also the distribution of these signals in the auxiliary building via means of the General Purpose Multiplexer is explained. Finally detailed specifications of the timing modules plus full operating instructions are included. The modules concerned are the general purpose timing modules, TIMING TG1 and TIMING TG2 , the manual timing module TIMING TM, the two fanout modules TIMING TFBB and TIMING TFBL and the visual display test module TIMING TD.

The SPS Timing System Proposal

1. INTRODUCTION

The correct operation of the SPS is absolutely dependent, amongst other parameters, upon an accurate and reliable timing system. This proposal describes such a system.

The environment of the SPS, in particular its physical size and its required mode of operation, greatly influenced the design criteria of the timing system. The versatility of the SPS dictates that the timing system itself must be extremely flexible. This flexibility is achieved at the generation end by using a computer to provide the cycle information for the Master Timing Generator unit (MTG). At the user end the flexibility is provided by distributing the timing signals through the General Purpose Multiplexer (GP.MPX) system. The timing repeatability precision is not affected by the various lengths of the GP.MPX Bus.

2. PS - SPS DIALOGUE

In order for correct beam injection to occur the timing system of the SPS must be synchronised to that of the PS. The dialogue between the two machines is of the master - slave relationship where the PS is the master. Under no circumstances whatsoever can the SPS delay the programmed cycle of the PS. If, for any reason, the SPS is not ready to accept injection it must miss that injection period and wait for another Injection Prepulse response from the PS. (Fig.1a)

The SPS generates a 'Beam Required' signal which is transmitted to the PS. This signal informs the PS that the SPS is ready for injection. The PS interrogates this line twice during the injection sequence, the first test occuring approximately one second before ejection. This is the Linac test and if the line was inactive at that time the Linac pulse will be dumped at the output of the Linac and the injection sequence terminated. But if the line was active it is interrogated again 300 mSec. before ejection. This is the Booster-PS test and if the SPS was unable to continue the injection sequence the beam will

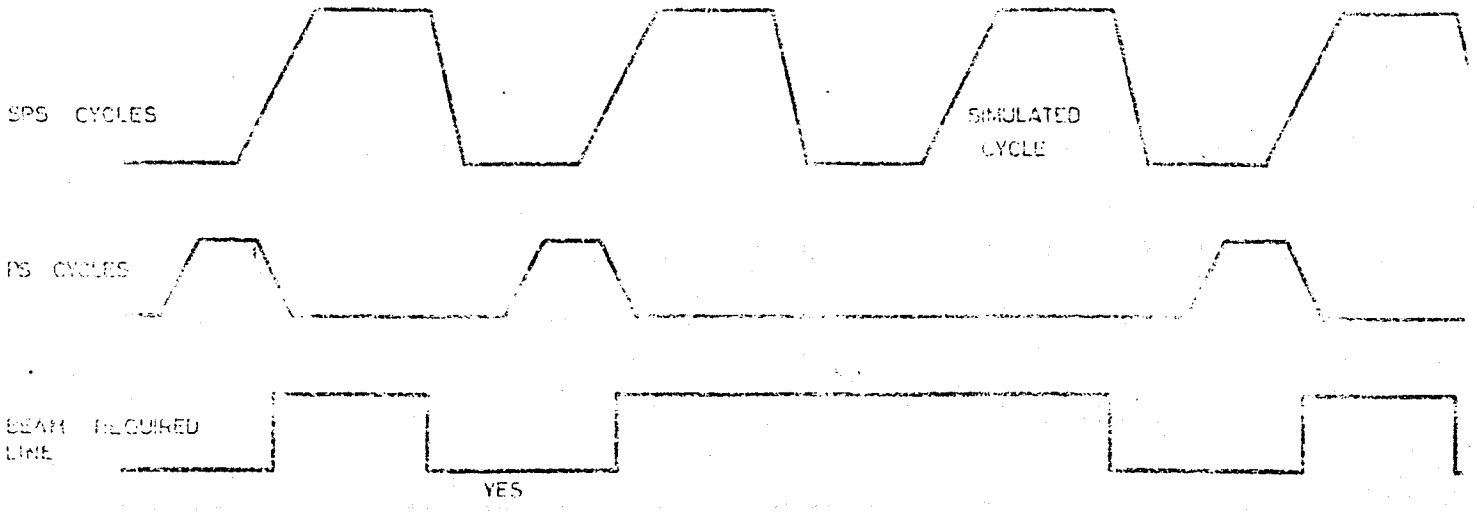


FIG. 1a

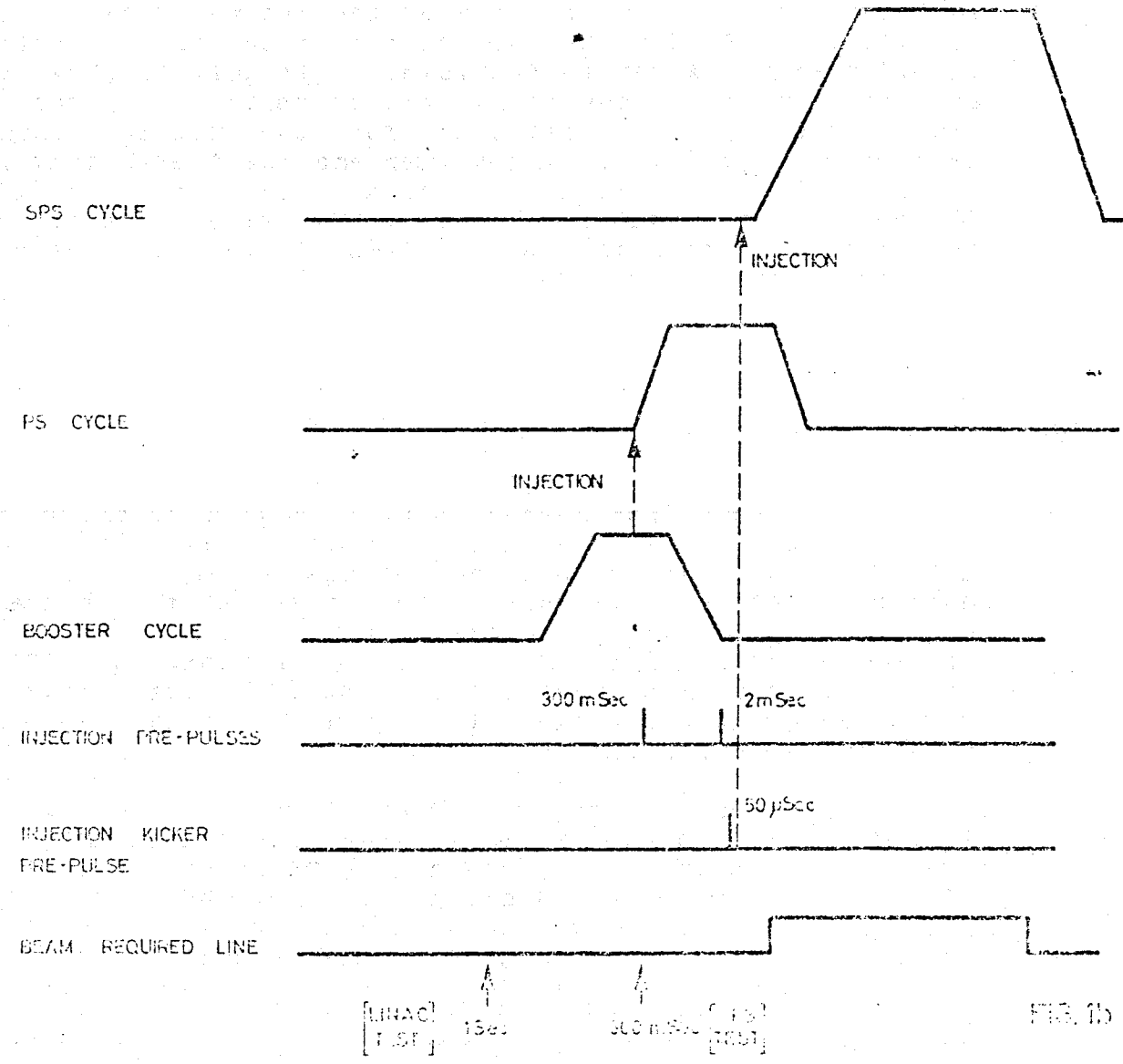


FIG. 1b

FIG.1 PS-SPS DIALOGUE

be dumped in the PS at the lowest energy possible. If the test was successful the PS commences its acceleration cycle to SPS injection level at 10 GeV.

Besides interrogating the Beam Required line from the SPS the PS also transmits three injection pre-pulses to the SPS. The first pulse occurs just before the PS acceleration cycle, approximately 300 mSec prior to ejection. A second pulse is transmitted to the SPS informing it that beam was successfully de-bunched during the acceleration cycle and that ejection from the PS will definitely occur 2 mSec. + or- 2uSec. later. This pulse is used to generate the Reset signal in the SPS. Finally the Injection Kicker Pre-pulse is transmitted 50 uSec before injection. [Ref.1]

3. THE GENERAL SPS TIMING PHILOSOPHY

The basic time unit for the SPS is 1mSec. This time information is transmitted to the user by the Clock Train which consists of a series of pulses at 1mSec. intervals with a repeatability accuracy of + or - 1uS. The clock is referenced to the injection kicker pre-pulse at the start of each cycle. (Fig.2a) Under normal operating conditions all timing operations will be referenced to this clock.

In conjunction with the 1mSec clock a coded Event Train is also transmitted. [Ref.2, Ref.3] This code uniquely identifies specific operations during a cycle, eg. start of front porch, slow extraction, dump etc. When a timing module receives and recognises a valid Event Code it waits for the next clock pulse which it interprets as the Event Marker Pulse. The instant at which the events actually start will be coincident with the appropriate clock pulse. (Fig.2b) This guarantees a repeatability accuracy of + or - 1uS for each event. The Event Code can be programmed by the Master Timing Generator to occur during any 1mSec. time interval. (Fig.2c) It is possible for a number of different Events to occur during the same one millisecond time interval.

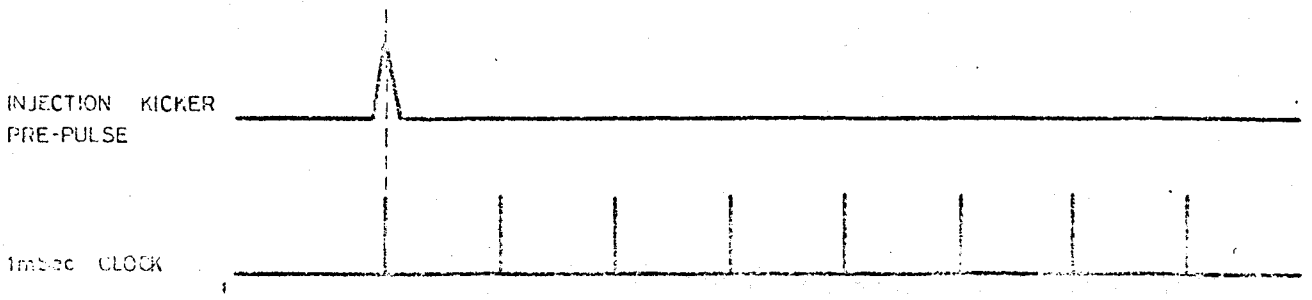


FIG. 2a

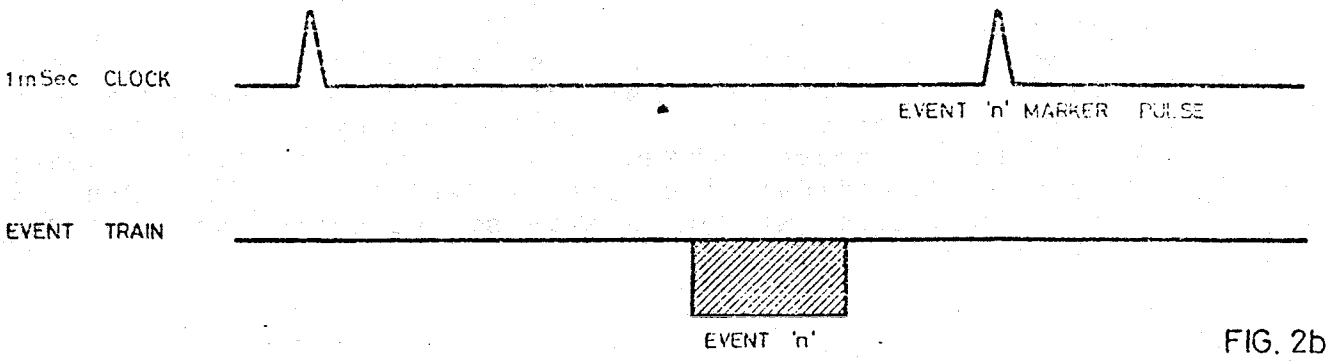


FIG. 2b

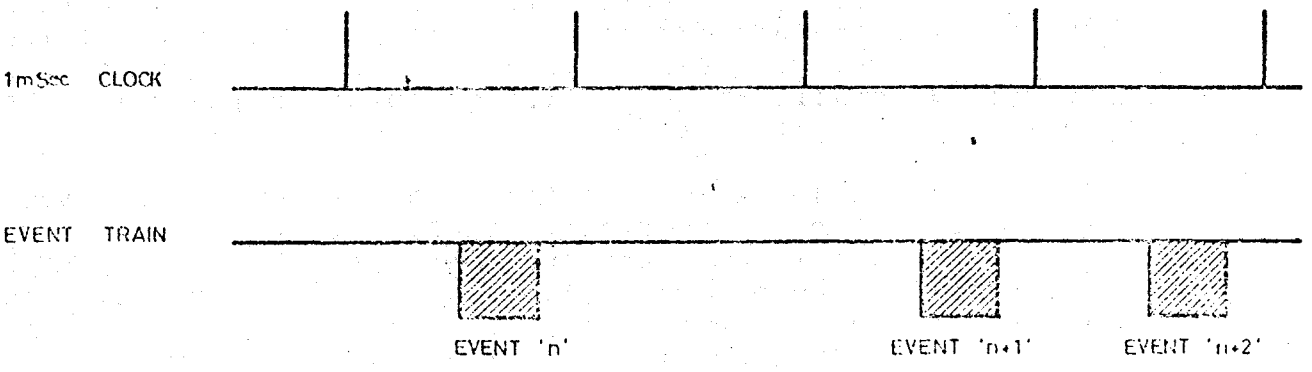
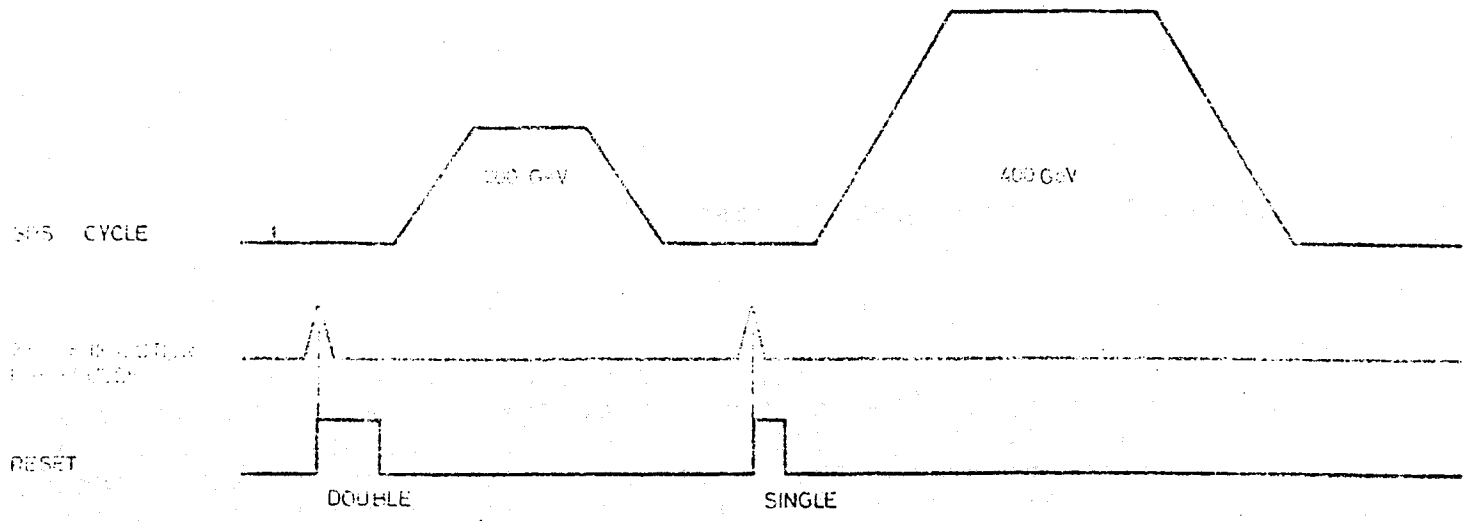


FIG. 2c

FIG. 2 GENERAL TIMING WAVEFORMS



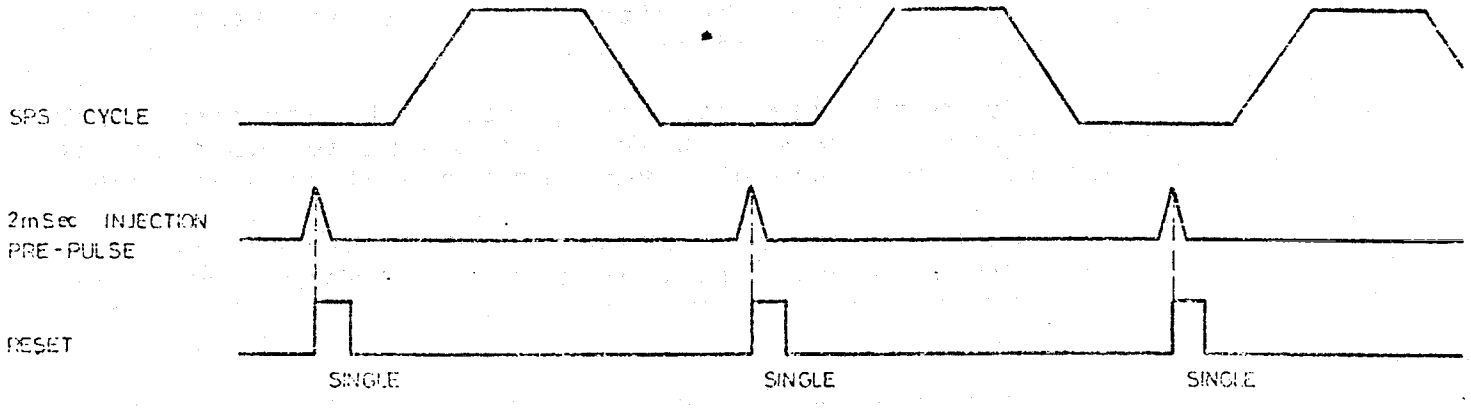


FIG. 2d

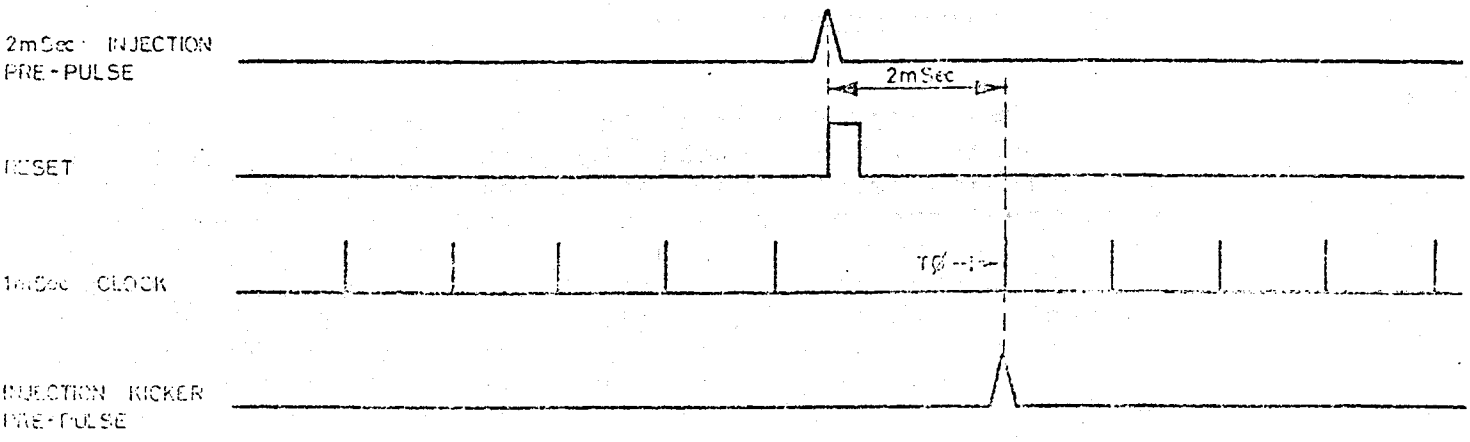


FIG. 2

FIG. 2 GENERAL TIMING WAVEFORMS (cont.)

The most significant binary bit of each event code is the Simulated Cycle bit. The MTG sets this bit to a logic '1' if the SPS cycle is being simulated, i.e. no beam present. This bit is tested in the GP.MPX Timing Connection Unit (Fig.6) where a flag is set if the cycle is being simulated. This flag may be used to generate an interrupt, or alternatively the General Purpose Computer may use it as a status bit. In both cases the computer receives the information through CAMAC. The connection unit will normally be situated in the same rack as the CAMAC crate controlling the GP.MPX.

To enable users to initialize their equipment for each cycle a reset pulse is transmitted 2mS prior to injection. Two types of reset signals will be generated.

a) Double - prior to injection of double cycle.
b) Single - prior to injection of single cycle and prior to second injection of double cycle. (Fig.2d)

Both the resets halt the 1mSec clock which remains disabled until the injection kicker pre-pulse occurs, consequently the first clock pulse after a reset will always be at time zero (T0) (Fig.2e)

4. GLOBAL TIMING DISTRIBUTION

The MTG situated in the Control Building must transmit the timing signals to each auxiliary building. The transmission may be accomplished as a 'star' connected system or as a global series connection. (Fig.3) Although previous timing systems eg. PS. DNPL [Ref.4] tended to utilise the 'star' approach as it was generally simpler to impliment and afforded more user isolation the SPS will use the global transmission system. This is because for large accelerators, such as the SPS or NAL, [Ref 4] the cost of the extra terminated cables that are required becomes significant. Furthermore for the MTG to perform on-line data validation checks on the star system additional circuitry and cabling would be required at each user end of the star.

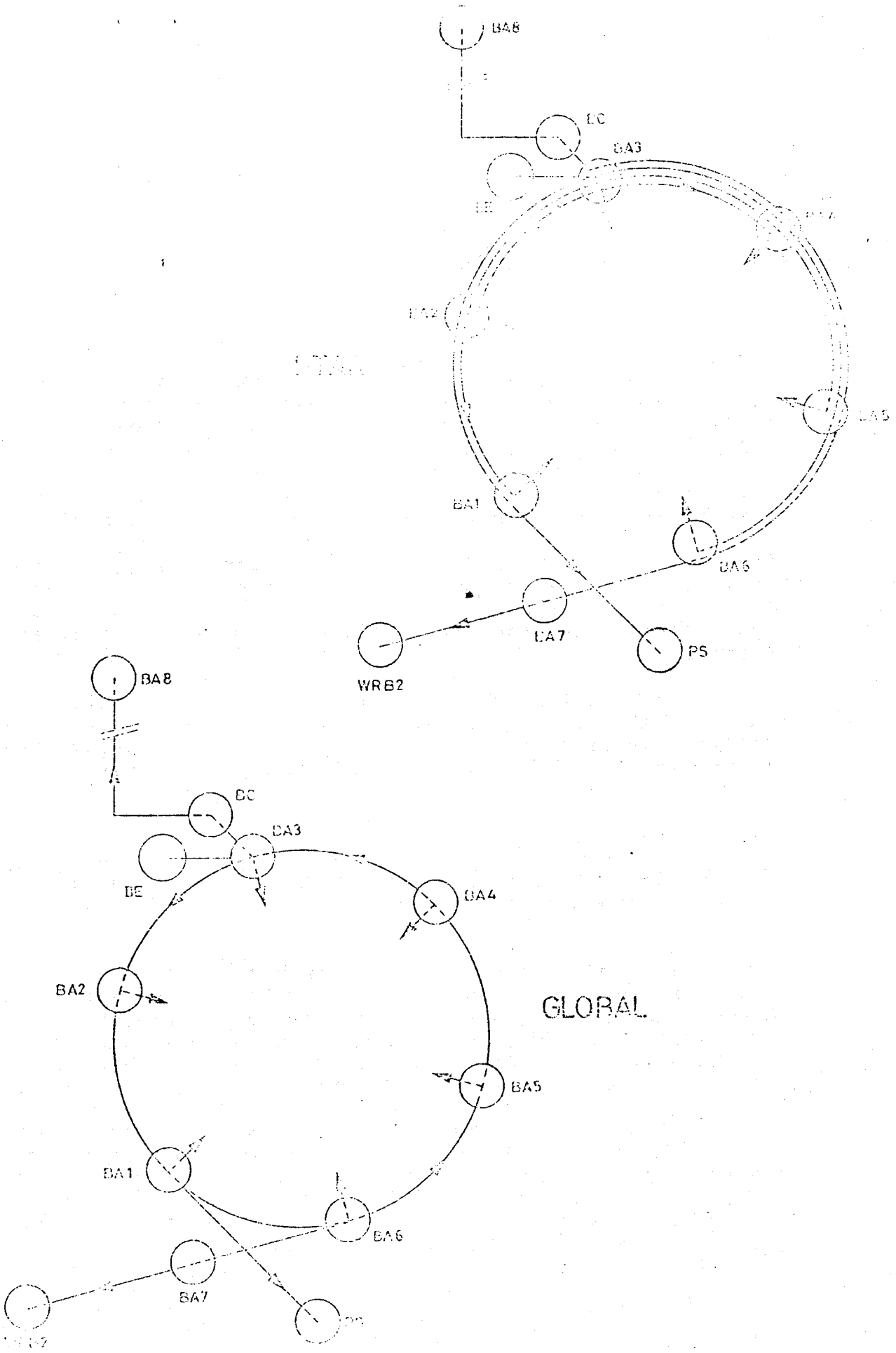


FIG. 3 INTER-BUILDING CONNECTIONS

Also the global distribution system requires only one cable passing round the periphery of the accelerator. At each auxiliary building the timing signals are 'tapped off' the main cable and connected to the GP.MPX by means of the repeater units. (Fig.4) It is extremely important that good isolation exists between the user and the main timing cable in order to prevent the user from corrupting downstream timing information. There must be good common mode isolation between each auxiliary building and between signals generated and transmitted in those buildings. Transformer isolation is ideal for both applications as the transformer acts as a band-pass filter.

As both the origin and the final destination of the global signals is the MTG itself it is a relatively simple exercise to include logic for checking the transmitted information. Two modes of checking are available:-

1) Digital

The number of bits transmitted is compared with the number of bits received. This can be achieved by a simple up/down counter in the MTG.

2) Time

The total inherent propogation time for the global transmission, including the transmission time from the head of the access shaft to the repeater units in each auxiliary building, is 42.5uSec which must be constant within + or- 1.0 uSec. (Fig.5a) This can be checked by standard time of flight techniques.

Both modes will be essential during the system installation and commissioning stages as diagnostic tools. During run time mode 2) could be included in the pre-check procedure prior to injection acceptance, whilst 1) will be extremely useful as a monitor of the overall system performance. It is not intended that this mode will function on an interactive basis during a cycle.

Fig.5a clearly indicates that whilst the beam travels in a clockwise direction the timing signals are transmitted from the control building in an anti-clockwise direction. This approach provides the users with the maximum possible warning time between TO and the arrival of the beam at each super-period. It can

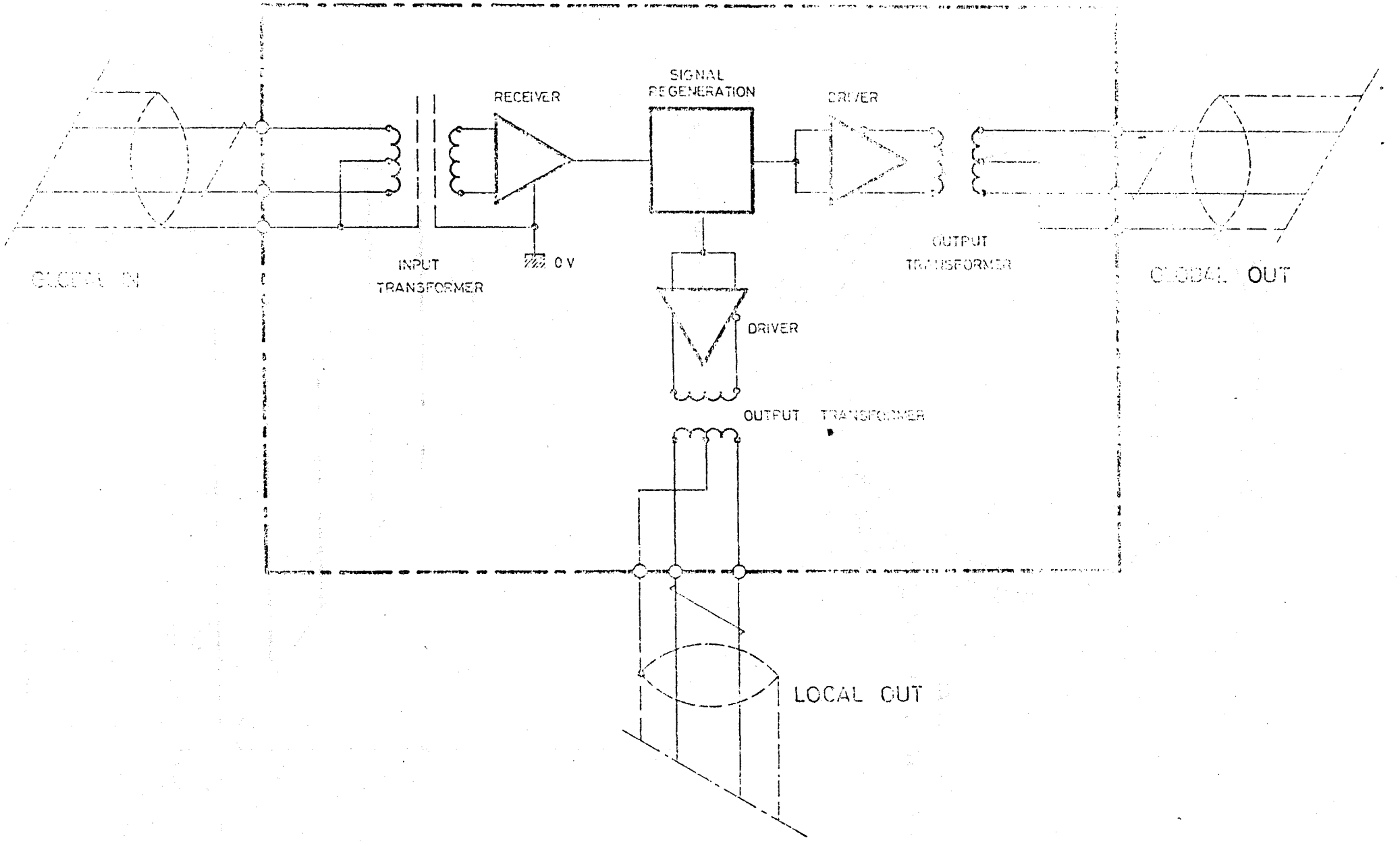


FIG.4 REPEATER UNIT

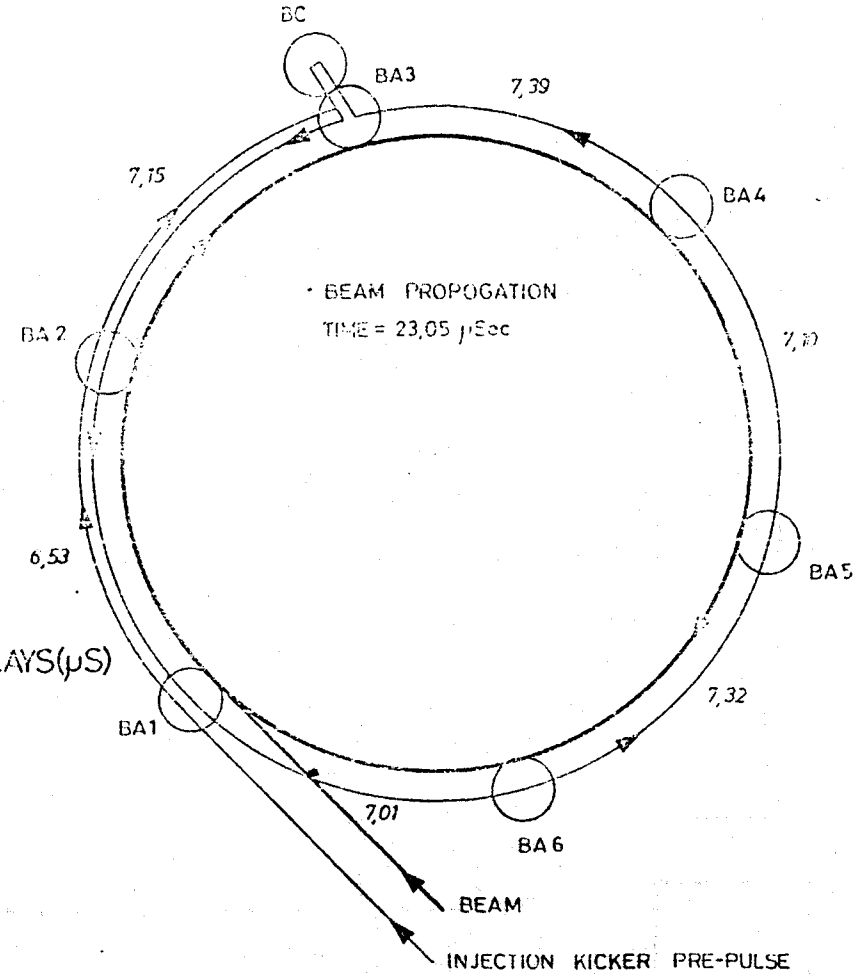


FIG. 5a TIMING SIGNAL PROPOGATION DELAYS(μS)

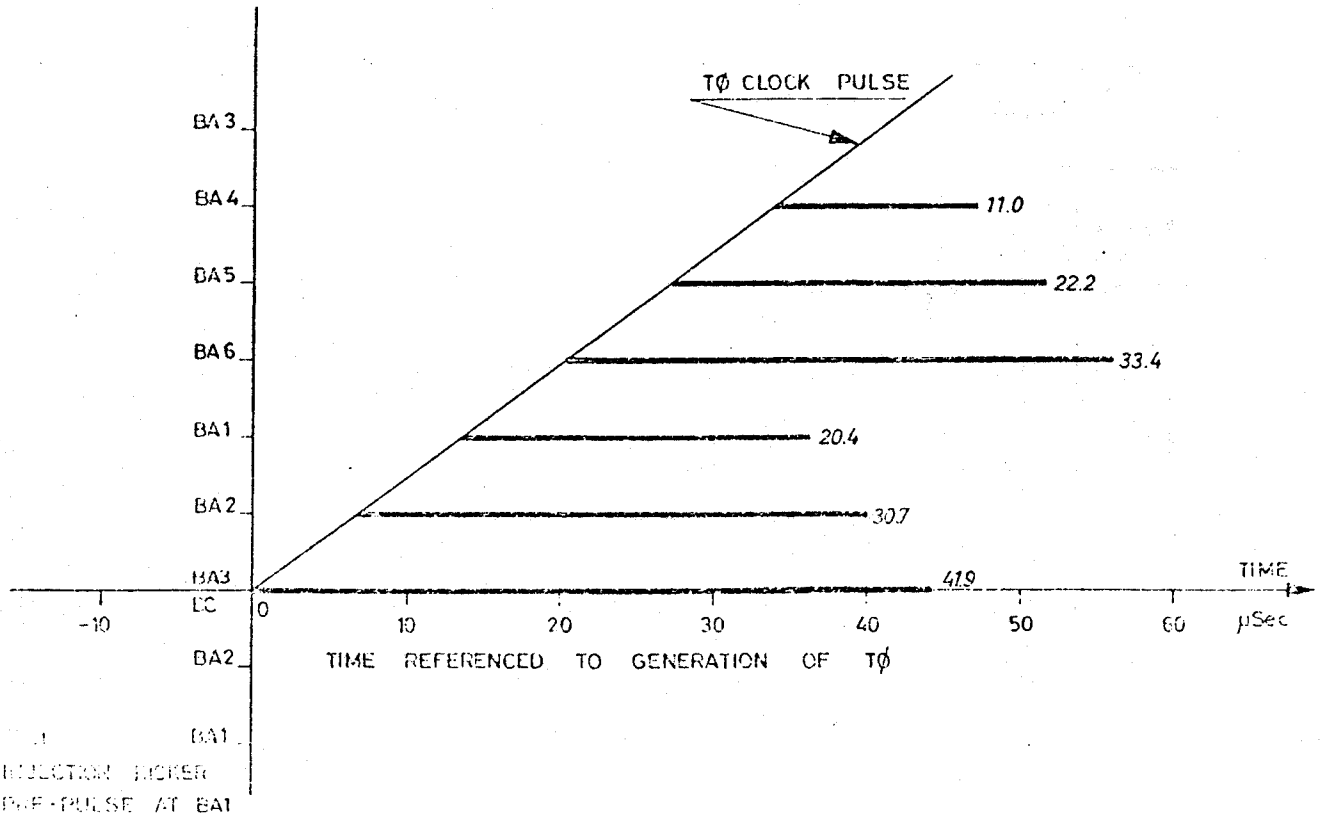


FIG. 5b CHART INDICATING ARRIVAL OF BEAM (μSec) REFERENCED TO TØ AT EACH AUXILIARY BUILDING

be seen from the chart (Fig.5b) that this time varies from 41.9 uSec at BA3 to 11.0uSec at BA4. If the signals were transmitted in a clockwise direction there would be a minimum warning time of only 2.5uSec at BA2.

5. LOCAL TIMING DISTRIBUTION

The timing signals are distributed throughout the auxiliary buildings by means of the GP.MPX. (Fig.6) The overall concept of the GP.MPX makes it ideally suited for this task. [Ref 6]

In each MPX Station Crate the Tete de Station unit receives the bi-phase timing signals from the MPX bus and translates them to binary code. These signals, at TTL levels, are then transmitted onto the Station Crate Dataway. (Fig.7) The signals are listed in Table 1. The 1mSec clock and the Reset signals are taken to the front panel of the Timing Tete de Station module where they are connected to Lemo connectors through buffer isolators. User timing modules will be inserted into the Station crates where they receive the global timing information via the dataway. Note that the translation from bi-phase to binary performed by the Tete de Station simplifies the logic necessary in each user timing module.

All timing modules will have blue anodised front panels in order to provide an obvious means of identification when inserted amongst the GP.MPX modules.

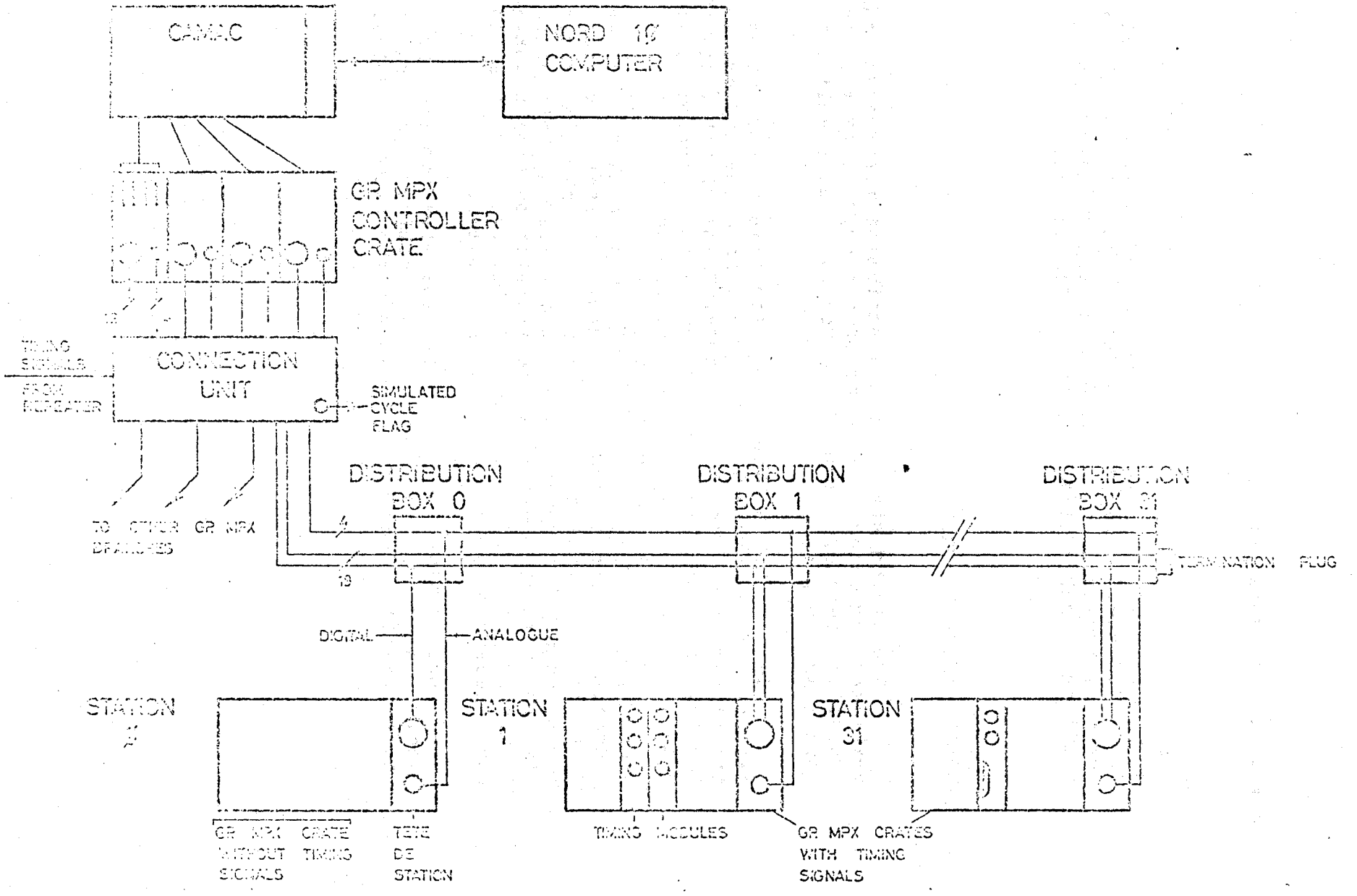


FIG. 6 TIMING DISTRIBUTION THROUGH THE GR MPX

TABLE 1.

DATAWAY PIN NO	SIGNAL IDENTIFICATION	GENERAL COMMENTS
17	1mSec CLOCK	All the signals on pins 17 > 22 inclusive are TTL compatible.
18	BINARY EVENT CODE	
19	EVENT CODE CLOCK	
20	EVENT STROBE	
21	RESET	SINGLE 20uS DOUBLE 40uS
22	INTER-MODULE LINK	Output from TG2

6. SIGNAL STANDARDS

a) Global

The global signals are transmitted on one pod of a standard six pod video cable. The audio twisted pair of the pod is used to transmit the Event Train whilst the larger diameter video pair transmits the Clock Train plus the Reset signals. All global signals are transmitted as a Manchester bi-phase code. This code, coupled with the characteristics of the repeater units, provides good noise immunity. The amplitude of the signals are + and - 5 volts.

b) Local

In this context local is defined as the transmission medium between the local outputs of the repeater units and the input to the Tele de Station unit in the GP.MPX crate. The two twisted pairs required for the timing signals are contained in the main GP.MPX bus cable. (Fig.6) Again the Manchester bi-phase code is used but the signal levels are at 0 and + 5 volts. This is

to make it compatible with the standard power supply of the GP.MPX and also to reduce the possibility of crosstalk from the timing signals onto the multiplexer data lines.

c) User

Three types of outputs are provided:

1..For connecting to users external equipment.
Blocking oscillator levels, BNC 50 ohm connector.

Timing signals for driving users external equipment will be generated by a blocking oscillator circuit. The circuit will provide a transformer isolated positive pulse of 20 volts amplitude into a 50 ohm load. The pulse width will be 2uSec with a rising edge of less than 50nSec.

2..For connecting to users CAMAC equipment.
TTL levels, Lemo 00 connector.

Negative logic TTL levels are used compatible with the CAMAC unterminated signal standards. Each output will be capable of driving a minimum of 30 TTL loads. The output signals are time-stretched by monostables to 10uSec. in order to make them compatible with all CAMAC interrupt registers. This enables the user to generate an interrupt during any selected part of the SPS cycle.

3..For connecting to users equipment situated in the same GP.MPX crate.
TTL levels.

This signal is generated by the general timing module TIMING TG2 (see module description for full details). It is intended for users who have a number of modules which require a common timing pulse. The timing module generating the signal and the user modules receiving the signal must all be in the same GP.MPX crate. User GP.MPX modules which utilize this line should isolate the signal before transmitting it to their external equipment.

7. TIMING MODULES

Six different types of modules are described in detail. The two general timing modules, TIMING TG1 and TIMING TG2, will normally be used by the users for generating the majority of their timing signals. The manual timing module TIMING TM enables the users to change their timing parameters manually. Normally these can only be changed by the computer operating system. The fan-out module TIMING TFBB accepts either a blocking oscillator or a TTL level input and generates six completely isolated blocking oscillator type outputs. The other fan-out module TIMING TFBL has a similar signal specification but it generates ten blocking oscillator outputs which are connected to two pin Lemo connectors type 0. Finally the display module TIMING TD is a test module which, when connected to either the general or manual timing modules, visually indicates the programmed parameters of that module.

The two general purpose timing modules are both able to generate two blocking oscillator type output pulses. The outputs of TIMING TG1 are of the format:

Output A = En + x
Output B = En + y

where En is the selected event and x and y are the respective delays, in milliseconds, between the event and the two output pulses.

Module TIMING TG2 has the format:

Output 1 = En + m
Output 2 = En + m + p

where En is either the selected event or the external start, m is the delay between En and Output 1 and p is the delay between Output 1 and Output 2. Both the delays can be in either millisecond or external clock units.

The main difference between the general modules is the trigger point for the second counter. For TIMING TG2 and TIMING TM this point occurs at the completion of the first delay counter whilst the counters of TIMING TG1 are both triggered when the selected event has been detected.

Also a number of integrated circuits and front panel connectors have been omitted from TIMING TG1 to reduce cost. (see module descriptions for full details)

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