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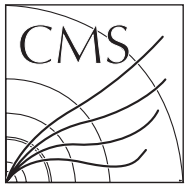

The Compact Muon Solenoid Experiment

Conference Report

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Experience from design, prototyping and production of a DC-DC conversion powering scheme for the CMS Phase-1 Pixel Upgrade

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for the CMS Collaboration

Abstract

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The testing program is outlined, results from mass production are presented and issues that have been encountered are described. In addition, two system level challenges, namely the choice of output voltage in the presence of large, load-dependent voltage drops, and the thermal management required to remove the heat load caused by the DC-DC converters, are discussed.

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Experience from Design, Prototyping and Production of a DC-DC Conversion Powering Scheme for the CMS Phase-1 Pixel Upgrade

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ABSTRACT: The CMS Collaboration has adopted a DC-DC conversion powering scheme for the Phase-1 Upgrade of its pixel detector. DC-DC buck converters with a conversion ratio of around 3 are installed on the support structures, outside of the sensitive tracking region, requiring a re-design of the low and high voltage distribution to the pixel modules. After several years of R&D, the project has entered the production phase. A total of 1800 DC-DC converters are being produced, and rigorous quality assurance and control is being employed during the production process.
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KEYWORDS: Particle tracking detectors (Solid-state detectors); Si microstrip and pad detectors; Voltage distributions.

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Contents

1. The CMS Phase-1 Pixel Upgrade

The CMS experiment [1] at the CERN LHC features a silicon pixel detector as its innermost component. The present device is composed of 1440 hybrid pixel modules, arranged in three barrel layers (BPIX) and two endcap disks per side (FPIX). In total there are 66 million pixels of size $100 \times 150\,\mu\mathrm{m}^2$. The sensor technology is n^+-in-n.

The present pixel detector has worked very well during LHC Run 1 (2010-2012). However, the pixel detector was designed for an instantaneous luminosity of $1.0 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. It is expected that the LHC instantaneous luminosity will increase to $2.0 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ already before Long Shutdown 2, scheduled for 2018. Under these circumstances, the current readout chip would suffer from a significant inefficiency, mainly due to buffer overflow, of up to 16 % for a bunch spacing of 25 ns. Therefore the CMS collaboration will replace its pixel detector during the extended year-end technical stop 2016/2017 [2]. The new detector will feature a layout with four barrel layers and three disks per side. The innermost barrel layer will move closer to the beam line (from 4.4 cm to 3.0 cm in radius), to improve impact parameter resolution and vertexing. A new readout chip with increased buffers and faster, digital readout will ensure the efficiency remains high. The material will be reduced by moving to an evaporative CO_2 cooling system and by relocating electronics boards. The overall module concept, pixel size and sensor polarity remain the same.

The additional detection layers increase the number of readout chips (ROCs) by a factor of about 1.9. Since the operating voltages will not change, the current required by the new pixel detector is also

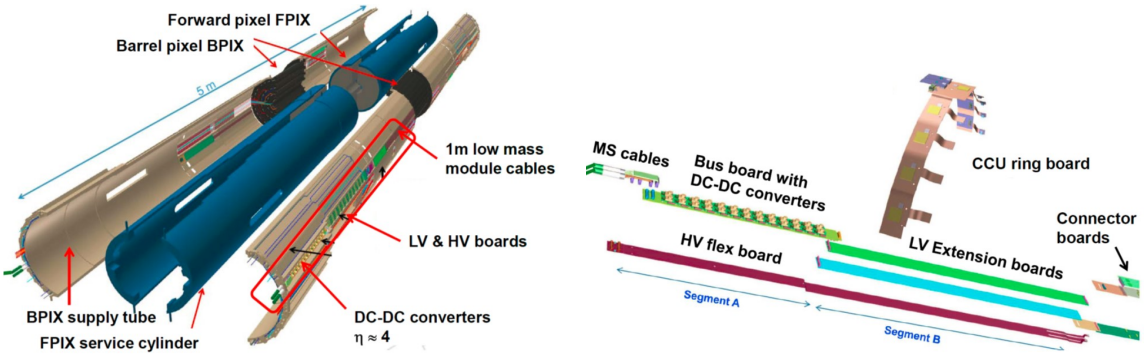

Figure 1. Left: drawing of the pixel detector including support structures. The supply tube (grey) is organized in longitudinal slots. In the drawing one slot (red frame) is filled with electronics components. The DC-DC converters inside the service cylinder are not shown. Right: exploded view of the power-related electronics components for BPIX. Except for the control ring board, which spans one half cylinder (eight slots), only components of one slot are shown.

a factor of 1.9 higher than that needed by the present device, leading to a factor of about 3.6 higher resistive losses on the 50 m long supply cables. A powering scheme based on the DC-DC conversion technique is employed, which allows the operation of the new detector with the existing cable plant and power supplies.

2. The Powering Scheme and its Implementation

Step down DC-DC converters are used to generate the low voltages (LV) for the pixel modules' readout chips. After irradiation to their respective expected doses, the ROCs in layer 1 and FPIX require a digital supply voltage of 2.5 V, BPIX layer 2 requires 2.6 V, and BPIX layers 3 and 4 require 2.4 V. A dedicated ROC is under development for layer 1, explaining why layer 2 requires a higher voltage, despite layer 1 being closer to the interaction point. The minimum analogue voltage is 1.6 V for all modules. The DC-DC converters supply a voltage of 2.4 V to the analogue part of the ROC. The digital part of the ROC and the Token Bit Manager (TBM), a chip used to control the readout on the pixel module, are supplied with 3.5 V for FPIX and layer 2 of BPIX, while a voltage of 3.3 V is chosen for BPIX layers 1, 3 and 4 (the choice of output voltage is treated in more detail in Sect. 5.1). The DC-DC converters receive an input voltage of 10 V. The conversion ratio, defined as the ratio of input voltage to output voltage, is thus in the range of 3-4.

The input voltage is generated by CAEN A4603 power supplies, which are installed in the experimental cavern. A modification was required to raise the voltage they supply to the desired value. In addition their remote sensing feature was replaced by a control loop regulating with time scales of hundreds of milliseconds, much slower than the bandwidth of the DC-DC converters' internal voltage regulation. In this way interference between the two regulations are avoided.

The DC-DC converters will be installed on the pixel service structures (Fig. 1 (left)), namely inside the FPIX service cylinder and on the outside of the BPIX supply tube, at a pseudorapidity[1]

[1]The pseudorapidity η is defined as $\eta = -\ln(\tan(\theta/2))$, with θ being the polar angle in the CMS coordinate system. In this coordinate system the z axis points along the anti-clockwise beam direction, the x axis points towards the centre of the LHC ring, and the y axis points upwards. The polar angle is defined with respect to the positive z-axis.

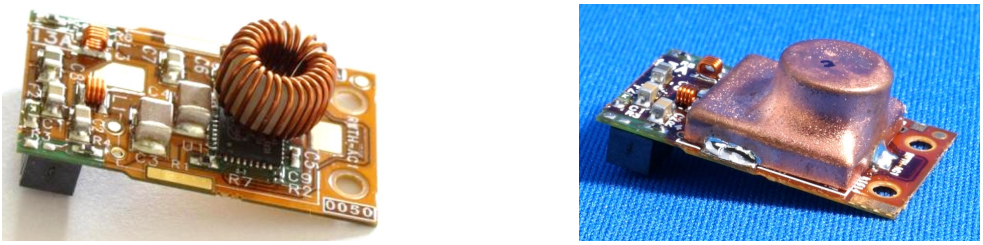

Figure 2. Photos of PIX_V13 DC-DC converters. The left photo shows a board before mounting of the electromagnetic shield, while on the right a complete, shielded DC-DC converter can be seen.

of about 4. This is outside the active tracking volume, making the material added by the DC-DC converters less critical than it would be if located in the pixel detector volume itself. The distances between the DC-DC converters and the pixel modules are 1-2 m.
The digital current required by the pixel modules depends on the chips' activity and thus on the hit rate. Pixel modules in the inner layers require more current than outer modules. Between one and four pixel modules are served by one pair of DC-DC converters, resulting in maximum currents of about 2.4 A and 1.7 A on the DC-DC converters that supply the digital and analogue part of the ROC, respectively. The total number of DC-DC converters that will be installed in the pixel detector amounts to 1184. Of those 384 are required for FPIX, while 800 are used for BPIX.
The power distribution requires several electronics boards. Here the BPIX system is discussed as an example; the FPIX implementation is similar, but differs in the details. The BPIX supply tube is organized in slots (Fig. 1 (right)).The DC-DC converters are plugged to a motherboard ("bus board"), into which the multi-service (MS) cables, coming from the power supplies, are plugged. Low voltage "extension boards" connect these bus boards via "adapter boards" to "connector boards". The 1 m long low-mass module cables plug into these connector boards. In addition, the high voltage (HV) required to deplete the silicon sensors is distributed via a high voltage flex board. Finally, a control board based on the CCU ASIC [3], the "CCU ring board", is required to control various devices on the supply tube, including the DC-DC converters, as detailed in the next section.

3. DC-DC Buck Converters for the Phase-1 Pixel Detector

The DC-DC converters used for the Phase-1 Pixel Upgrade, referred to as "PIX_V13", are of the "buck" topology. Photos are shown in Fig. 2. The power transistors, the voltage regulation loop, the protection features, and the remote control are embedded in an ASIC, the "FEAST2" chip designed by CERN [4]. This radiation-tolerant chip is a generic development, used in several experiments. The chip is mounted on a 2-layer PCB, which has a footprint of $2.8 \times 1.7\,\mathrm{cm}^2$. The PCB hosts the input and output noise filters, the air-core inductor, the voltage divider used to set the output voltage, the circuit used to set the switching frequency, a slow fuse that triggers on an over-current at the input side, circuitry related to the remote control signals, the connector, and an electromagnetic shield. The PCB, the inductor and the shield are custom developments for the CMS Pixel project, optimized for its special requirements, such as space limitations. The switching frequency is set to 1.5 MHz.
The chip can be enabled remotely, and outputs a status bit, the so-called "power-good" signal. For

the pixel application, the logic of the enabling was inverted with respect to the default mode of the chip, such that a "high" signal disables the chip. The advantage of this is that the DC-DC converters are enabled even when they do not receive a signal on the enable pin, e.g. when no remote control is connected, or when the respective circuitry is defective. The parallel ports of the CCU are used to send the enable signal and to receive the status bit.
The inductor is a solenoid with a plastic core. The inductance amounts to about 430 nH. The shield consists of a thermo-formed polycarbonate Lexan foil with a 60 μm thick layer of copper galvanically deposited on the outside. It covers not only the inductor, but a rectangular area that hosts the noisy part of the circuit. The shield is filled with thermal grease and acts also as a cooling contact for the inductor. It is soldered to several pads that are on ground potential. Care was taken to avoid electrical contact between the grounded shield and the components inside the shield, including potting at a location where the distance was tight. Both the inductor and the shield need to be soldered by hand.
A large ground plane on the back side is used to bring the DC-DC converter in thermal contact with the cooling system. The weight of the DC-DC converter, including the thermal grease, is about 3 g.
The PIX_V13 pixel DC-DC converters are the result of several years of R&D and prototyping. It was verified that the conducted noise (propagating through the cables) is small and that electromagnetic emissions are shielded properly. Tests with pixel modules showed that the modules' performance is not affected by the presence of the DC-DC converters. The thermal management was studied using a CO_2 cooling system, and was found to work well. The dynamic behaviour during power-on and power-off sequences was explored in system tests including the modified pixel power supply, a 50 m long original supply cable, and DC-DC bus boards carrying the final number of DC-DC converters, under realistic load conditions. Up to now, no problems were observed in those tests. Much more detail can be found in [5], and in the references therein.

4. DC-DC Converter Mass Production

Failing DC-DC converters will result in up to four non-functioning pixel modules, thus strict quality assurance is crucial. In Sect. 4.1 the production, assembly and testing steps are outlined. Issues encountered are discussed in Sect. 4.2, while the production quality as observed so far, based on the status of September 2015, is covered in Sect. 4.3.

4.1 Production Steps, Quality Assurance & Control

The PCBs were optically inspected upon reception. The inductors were delivered pre-sorted into inductance classes. Coils with inductances closest to the nominal value were used preferentially. The shields were produced by an external company. Several iterations were required to reach the desired quality, in terms of shape uniformity and in particular regarding planarity and smoothness of the cutting edge. The shields were optically inspected. The chips, delivered by CERN, were not tested before assembly.
The assembly was performed by another company following the IPC-A-610D standard. The same company also handled the hand-soldering of the coil and the shield, the application of a specified amount of thermal grease, and the potting of one component inside the shield. The company performed automated optical inspection (AOI) during the assembly. High-resolution X-ray images

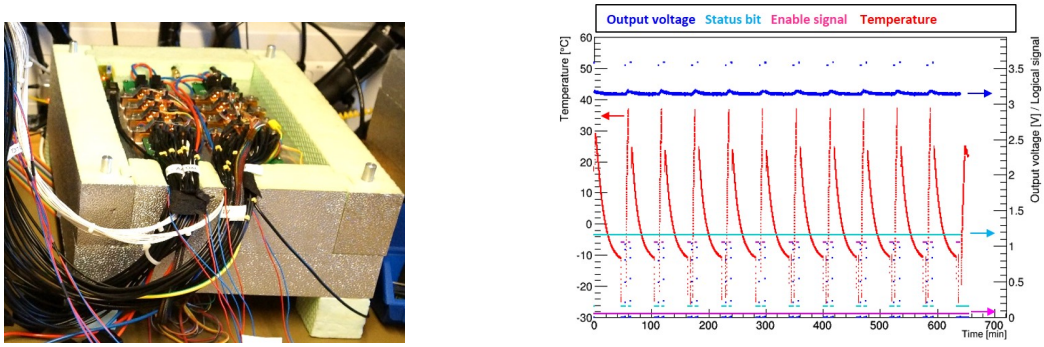

Figure 3. Left: photo of the box used for active thermal cycling of the DC-DC converters. Right: data of a typical run. The output voltage of the DC-DC converter is shown in dark blue, the enable signal in pink, the status signal in cyan, and the temperature, as measured on the converter's shield, is shown in red. The left y-axis corresponds to the temperature data, while the right y-axis corresponds to all other curves. The sudden drops in temperature are caused by switching the DC-DC converter off for a short time.

were taken of all samples, including a close-up image of the chip, and a picture of the whole PCB including the passive components. This allowed the soldering quality to be assessed and checks to be made for air inclusions (voids). The company also performed passive thermal cycling for all boards, consisting of ten cycles between -30°C and $+60$°C. All X-ray images as well as details of any manual reworking were provided by the company. Micrographs were performed on two samples in order to assess the soldering quality. Several sections were prepared, including the solder pads of the chip, and the soldering of a variety of SMD components.

After the assembly of the boards, but before the assembly of the shield, the boards were returned, temporarily, for checking. This was done because visual inspection and reworking of the complete board area are only possible before the shield has been mounted. Two boards out of each 30-board panel were optically inspected. An electrical test of each board was performed, which included a measurement of the output voltage and efficiency versus load, a check of the enabling feature, and checks of the power-good bit. Good boards were returned to the company and received their shield. Once this was complete, the boards were delivered and a second, identical electrical test was performed.

All good boards are thermally cycled in-house using a custom set-up with active loads and an FPGA controller, in order to assess infant mortality and to check for proper functionality under realistic temperatures. Each board is subjected to ten cycles between -28°C and $+20$°C. During the test, the DC-DC converters are powered and a load of 3 A is applied to each converter. Output voltages, the status signals, and the temperatures (measured with PT100 sensors on the shields) are constantly monitored. At each minimum and maximum temperature several tests are performed. The converters are switched off and on again, to check that they come up properly. Similarly, the disabling and enabling is exercised. Finally the under-voltage lock-out feature, where the DC-DC converters are internally disabled for input voltages below 5 V, is checked by raising the input voltage in steps. The set-up and data from an example "run" are shown in Fig. 3. The thermal box can house 16 DC-DC converters at a time. Each cycling, with the box fully loaded, requires about ten hours. The throughput is about 80 DC-DC converters per week.

4.2 Issues during Pre-Production and Production

Several pre-production runs, each consisting of around one hundred DC-DC converters, were launched at the initially selected assembly company. All had problems. In particular, the last pre-production run was characterised by a severe lack of solder, presumably caused by deficient deposition of the solder paste in the screen printing process. This flaw was not observed at the company, neither by optical inspection, nor by inspection of the (low-resolution) X-ray images taken. It was spotted only when DC-DC converters were observed to fail during thermal cycling. Although mass production was imminent, it was decided that the assembly company should be changed and to specify to the new company that the assembly should follow the standard IPC-A-610D, referred to as "class 3".

A pre-production run adhering to class 3 was launched at another company, followed by the mass production of 1800 DC-DC converters. The quality was excellent. The critical solder deposition is done via a jet printer, not via a stencil as in the screen printing process. Nevertheless, also here a problem was encountered. Micrographs exhibited voids in the solder of one resistor type of "0201" size. This problem had not been spotted in the X-ray images, because originally the complete area was only X-rayed in 10 % of the samples. Images taken after the problem was observed showed that the problem is clearly visible in the X-ray images and would therefore have been spotted, if such pictures had been taken. A total of 150 boards were affected, and for these board the respective components were manually replaced. The problem was attributed to the wetting behaviour of the resistors and the company switched to a different supplier. It was also decided that the complete board area should be X-rayed in all samples from then on.

4.3 Quality and Yield of the Production DC-DC Converters

The following represents the status as of September 2015. All 1800 DC-DC converters have been assembled. Of those, 1200 have gone through the electrical tests and (if they passed the electrical test) through the thermal cycling. The yield so far is 87 %. Almost all faults relate to a malfunctioning of the power-good signal, where typically the status is low (signalling that the DC-DC converter is not in good condition), while the output voltage is present and the device is working perfectly. The problem is related to the chip and has recently been fixed in another chip submission [4], unfortunately too late for the pixel project. Only eight DC-DC converters exhibit other problems, including a short in the chip, and zero, wrong or unstable output voltage. When excluding the power-good signal problem, the yield is above 99 %.

A total of 24 % of all faults have only been found during the thermal cycling, typically in the first cycle, latest in the fourth cycle. These faults correspond to (intermittent) problems with the status signal, either at low temperature or after the test of the under-voltage lock-out. This shows that the thermal cycling is useful and allows the identification of additional faults.

Figure 4 (top left) shows the distributions of the efficiency, defined as output power divided by input power, for an input voltage of 10 V and an output current of 1.5 A. The efficiency is high and the spread is small. It depends on the output voltage and amounts to 82.5 %, 84.5 %, and 85.1 % for converters with 2.4 V, 3.3 V, and 3.5 V output voltage, respectively. The RMS is 0.2 % in all cases. The distributions of the output voltages are shown in Fig. 4 (top right). The means are (so far) 2.435 V, 3.308 V, and 3.501 V, again for an output current of 1.5 A. The RMS is between 34 mV

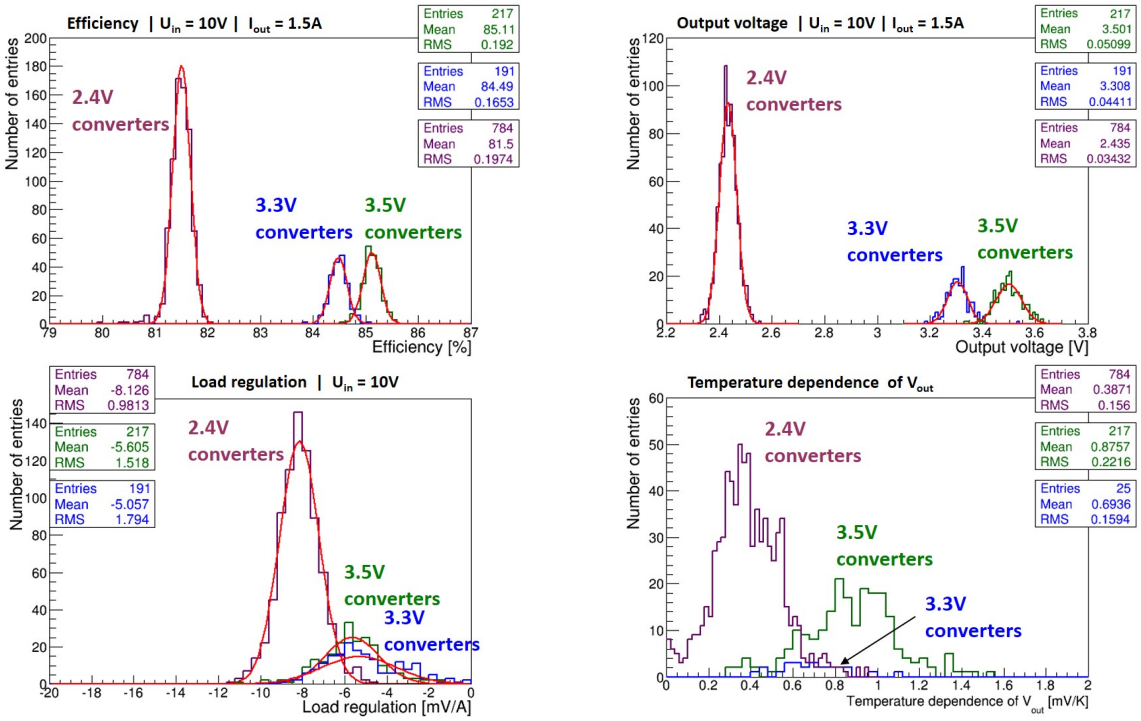

Figure 4. Distributions of efficiency (top left), output voltage (top right), load regulation (bottom left), and variation of the voltage with temperature (bottom right), from the production DC-DC converters. Devices with nominal output voltages of 2.4, 3.3 and 3.5V are shown in violet, blue, and green, respectively. The red lines show the results of Gaussian fits to the data.

and 51 mV, as expected from the rating of the resistors of the voltage divider.

The load regulation, i.e. the variation of output voltage with load, is shown in Fig. 4 (bottom left). The largest value is found for the 2.4 V converters, with a mean value of -8 mV/A. The variation of the output voltage with temperature has been studied as well (Fig. 4 (bottom right)) and is found to be of the order of 0.5 to 1 mV/K, with a rather large spread. The data stem from the thermal cycling. The temperature on a cooling contact was used to calculate the slope, and might not accurately reflect the converter's temperature change.

The difference in load regulation between samples of different output voltage might be explained by a temperature effect, as DC-DC converters with higher output voltage dissipate more power for the same load, and get warmer. This raises the output voltage.

Overall the quality of the produced DC-DC converters is excellent, the uniformity of important properties is high, and the yield is reduced only by the problem with the status signal.

5. System Aspects

5.1 Large, Load-dependent Voltage Drops

The definition of the optimal DC-DC converter output voltages has proven to be very difficult, due to the fact that the DC-DC converters do not feature remote sensing, and thus load-dependent voltage drops and other effects that influence the supply voltage have to be well understood and

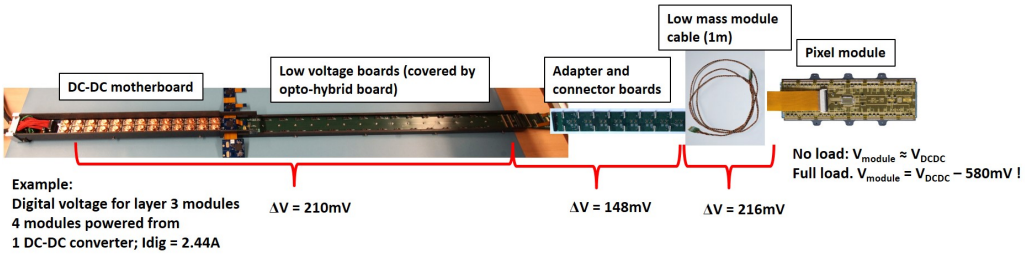

Figure 5. Picture of the power distribution, illustrating the voltage drops between DC-DC converters and pixel modules. Example values for the voltage drops, ΔV, between certain points are indicated. The values include both the supply and return paths.

taken into account. If the output voltage is too low, the readout chips will not function properly, while a too high output voltage poses a potential risk to the readout chips. The minimum required operation voltage after irradiation of the pixel modules was a priori not known and systematic studies after relevant levels of radiation became available only recently. A very recent radiation test led to the decision to raise the voltage for layer 2 from 3.3 V to 3.5 V, requiring a manual rework of 140 of the previously produced 3.3 V converters. The maximum tolerable voltage was also not precisely known, and therefore tests with readout chips operated for several weeks with a digital supply voltage of 3.6 V have been conducted.

The main effect are voltage drops on the up to 2 m distance between the DC-DC converters and the pixel modules, arising on the DC-DC bus board, the extension boards, the adapter and connector boards, and the module cables. These drops had been simulated and were later measured, once all these components became available. Since the ground planes are partly in common for several DC-DC converters, the bus board had to be operated with 13 pairs of DC-DC converters, all under nominal load. Figure 5 illustrates the problem and lists the voltage drops for one example line. The total drops are of the order of 500 mV for nominal loads. The pixel modules will thus be supplied with almost the DC-DC converter's output voltage after power-on, due to low-power default DAC settings, and with a voltage that is 500 mV below the converter's output voltage, when they consume the nominal power.

In addition, the DC-DC converter's output voltage is influenced by several other effects. The spread of the output voltage is already 35 to 50 mV. The load regulation reduces the output voltage by up to 10 mV per Ampere; the effect is thus channel dependent and 24 mV is the worst case. The temperature variation of 0.7 mV/K reduces the voltage with respect to room temperature measurements; the difference between $+20°$C and $-20°$C is 28 mV. Finally radiation effects (the expected dose is 100 kGy and the expected fluence is 2×10^{14} n_{eq}/cm^2) change the output voltage of the FEAST2 chip; radiation tests [4] indicate that the effect is of the order of 30 mV.

All effects have been added up, and the voltages have been chosen such that the minimum required voltages (Sect. 2) are guaranteed, with a margin of 100 mV.

5.2 Thermal Management

Another important system aspect is thermal management. The DC-DC converters' efficiency of about 80 % implies that 20 % of the total power is lost locally on the DC-DC converters, and the

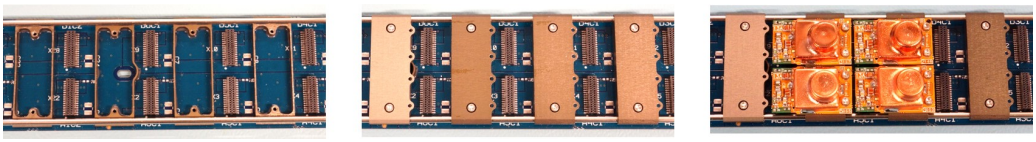

Figure 6. Photos of a part of a DC-DC bus board, in various assembly stages: with the lower pieces of the cooling bridges glued and the cooling pipes laid (left); with the upper pieces screwed onto the lower pieces (centre); and with two pairs of DC-DC converters plugged in and screwed to the upper pieces (right).

associated heat has to be removed. The heat load on one bus board is around 50 W.
The CO_2 pipes that are used to cool the pixel modules are entering through the support structures, and are used to cool the DC-DC converters and other electronics. In fact, the CO_2 is pre-heated, i.e. brought to the two-phase state, by the electronics on the support structures.
Aluminium cooling bridges, optimized with finite element calculations, are used to provide the contact between pipes and converters. A bridge cools one pair of DC-DC converters, so there are 13 bridges per bus board. Each bridge consists of two pieces, as shown in Fig. 6. The lower piece is glued onto the bus board. After the pipe is layed in during the integration, the upper piece is screwed to the lower piece. The DC-DC converters are then screwed to the upper pieces. The usage of thermal grease is foreseen.
The lower pieces have to be aligned very presicely with respect to the connectors, otherwise the plugged converters cannot be screwed to the upper pieces. A total of 520 pieces had to be glued using a dedicated jig.
The cooling bridges were anodized, in order to isolate the backside of the converters from the cooling pipes and thus to avoid ground loops.
The cooling concept has been tested under a variety of conditions, and was found to be adequate.

6. Summary and Outlook

The production of the parts for the DC-DC conversion powering system of the CMS Phase-1 Pixel Upgrade is well advanced, with board production finished and DC-DC converter production expected to finish in November 2015. From December 2015 onwards, the parts will be integrated into the support structures. A lot of experience has been gained and many obstacles were overcome. A rigorous quality assurance program was adopted to assure reliable operation of the system.

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