A 65 nm pixel readout ASIC with quick transverse momentum discrimination capabilities for the CMS Tracker at HL-LHC

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ABSTRACT: A readout ASIC for the hybrid pixel detector with the capability of performing quick recognition of particles with high transverse momentum has been designed for the requirements of the CMS Outer Tracker at the High Luminosity LHC. The particle momentum dicrimination capability represents the main challenge for this design together with the low power requirement: the constraint of low mass for the new tracker dictates a total power budget of less than 100 mW/cm^2. The choice of a 65 nm CMOS technology has made it possible to satisfy this power requirement despite the fairly large amount of logic necessary to perform the momentum discrimination and the continuous operation at 40 MHz. Several techniques for low power have been used to implement this logic that performs cluster reduction, position offset correction and coordinate encoding. A prototype chip including a large part of the final functionality and the full front-end has been realized and comprises a matrix of 16 by 3 rectangular pixels of 100 μm × 1446 μm, providing 7.65 mm^2 of segmented active area. Measurements of the analog front-end characteristics closely match the simulations and confirm the consumption of < 30 μA per pixel. Front-end characterization and irradiation results up to 150 MRad are also reported.

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Contents

1 Introduction

The High Luminosity LHC (HL-LHC) [1] requires a major upgrade of the Compact Muon Solenoid (CMS) experiment. A comprehensive description of the upgrade can be found in [2]. This work presents the upgrade of the readout ASIC for the hybrid pixel detector in the CMS Outer Tracker. One of the new requirements for this sub-detector is the capability of contributing information to the Level-1 trigger decision. Consequently, the readout ASICs need trigger functionalities never included before in a front-end module of a tracker. Bandwidth limitation and high granularity do not allow to ship the full event for every bunch crossing to the CMS back-end. Therefore, the whole event is stored on the front-end modules and it is sent when requested by a Level-1 trigger, as in the present tracker. In addition, a prompt readout path provides selected information for the Level-1 trigger decision to the back-end at the operating frequency of 40 MHz. This information, called "stubs", contains the coordinates of high transverse momentum (p_T) particles recognized locally by the readout ASIC. Back-end electronics in the counting room combines the stubs from the entire tracker to reconstruct the high p_T tracks which are used to generate the Level-1 trigger decision.

1.1 Tracker module for p_T discrimination

As shown in figure 1, the recognition of particles with high transverse momentum is based on modules, called p_T modules [3], which are made of two closely spaced detector layers. The readout electronics of the module measure the bending between the crossing points of a particle in the two nearby layers. This bending is used to reject the particles with low transverse momentum. This feature is called "Stub Finding". Two types of p_T modules [4] address different requirements in the tracker: the 2S modules include two strip sensor layers to ensure low power consumption at large
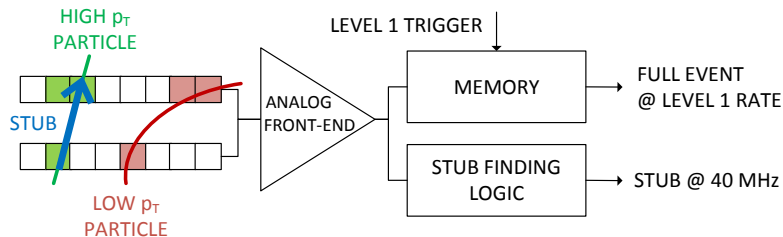
Figure 1. A simplified view of the readout electronics including p_T discrimination.

radius, while the Pixel-Strip (PS) modules combine a strip sensor with a pixelated one to provide the higher granularity required in the inner part of the tracker and a more precise position of the collision vertex along the beam axis, z_0.

1.2 Macro Pixel ASIC

The core of the PS module [5] consists mainly of the readout ASIC for the hybrid pixel detector, called Macro Pixel ASIC (MPA), and of a readout ASIC for strip detector, called Short Strip ASIC (SSA). The latter reads out the strip sensor, digitises the data and transmits them to the MPA at each bunch crossing. The MPA includes the front-end for the pixel detector, the memories where the whole event is stored for the Level-1 latency, and the Stub Finding logic. The latter combines the strip data from the SSA and the pixel data from the MPA front-end to find the high p_T particles for the L1 trigger decision. The details about the design of the full MPA can be found in [6]. This paper describes the MPA-Light: the first MPA prototype designed in a 65 nm CMOS technology.

2 Description of the MPA-Light

High complexity of the digital logic and the very low power density requirement make the MPA a very challenging project. This work addresses the challenge related to the design of a 65 nm analog front-end with a power consumption < 30 μA per pixel and explores several techniques for low power digital design. The front-end implements binary readout, while a fully synthesized logic in the chip periphery includes the Stub Finding logic for quick recognition of particles with high p_T. Input pins using a 160 MHz data rate from the SSA provide the strip data used to generate stubs. A summary of the main MPA-Light specifications can be found in table 1.

2.1 ASIC architecture

The MPA-Light is a 48 channels readout ASIC for hybrid pixel detectors designed in 65 nm CMOS technology to readout n+ on p- silicon detectors with an estimated capacitance < 500 fF per channel. As shown in figure 2, the die size is ~1.7 mm × 6.5 mm and includes pads for bump-bonding to the detector and wire-bonding for read-out and powering signals. The pixel matrix is composed by 16 × 3 pixels, where every pixel measures 100 μm × 1446 μm. The sensitive area is ~7.65 mm^2. The side edges of the ASIC extend only by 50 μm outside the pixel matrix to allow multi-chip assembly with a single sensor and therefore a minimal dead-area. At the bottom edge of the pixel matrix a row of dedicated bumps provides ground connection to the pixel sensor from the chip. Two staggered rows of wire-bond pads at the bottom edge of the periphery connect to the module

Table 1. MPA-Light specifications.

Chip size	~1.7×6.5 mm (1.7×4.5 mm active area)
Technology	65 nm CMOS (Normal and High V_T Standard Cells)
Pixel Size	$100\,\mu m \times 1446\,\mu m$
Detector type	n+ on p- (< 500 fF)
Measurement type	binary readout + event counting (testing)
Clock input	40 MHz (acquisition), 160 MHz (transmission)
Data type	Raw or encoded coordinate (stub or centroid)
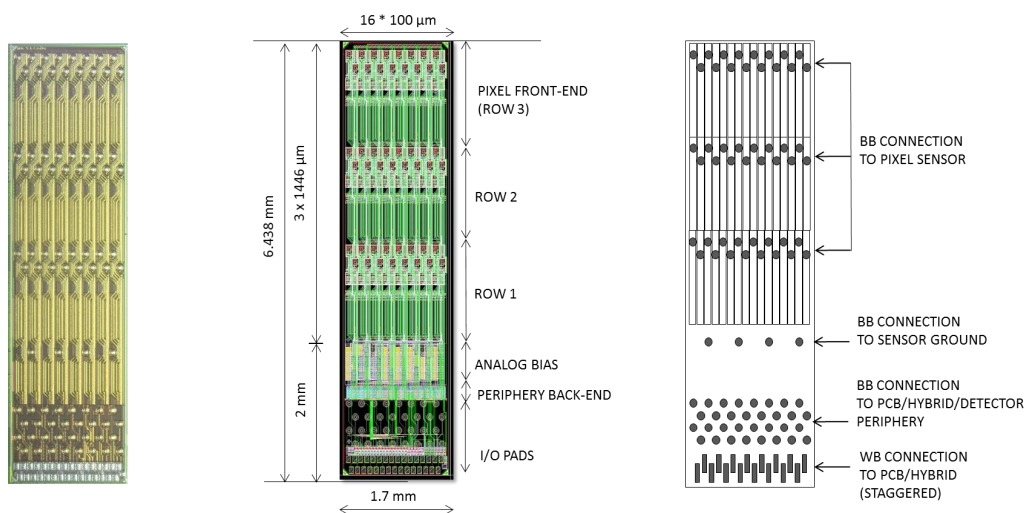
Figure 2. Left: picture of the MPA-Light. Centre: layout view of the MPA-Light with dimensions and components. Right: connectivity view of the MPA-Light (WB = wire-bond, BB = bump-bond).

substrate system. The wire-bonding pitch is 50 μm. The same signals are also provided by four rows of bump-bonds which allow a fully bump-bonded assembly with a bump-bonding pitch of 200 μm.
The chip can be operated in several modes and can be set in acquisition or configuration/readout modes by an external signal. A serial shift register is used to load the configuration, while another is used to read out the data. When acquisition starts, an internally generated signal clears the data from the previous acquisition. During acquisition, the chip needs an external 160 MHz clock through a Current Mode Logic (CML) receiver [7]. An internally derived 40 MHz clock is used for acquisition.

2.2 Pixel front-end

The pixel architecture is shown in figure 3. The analog front-end consists of a pre-amplifier with Krummenacher feedback [8] for detector leakage compensation, a shaper and a two stage discriminator with hysteresis. The details about the analog front-end can be found in [6]. A global 8-bits DAC (threshold DAC) sets the threshold for the pixel matrix and a 5-bits DAC per pixel allows to compensate the pixel-to-pixel threshold variations. Another global 8-bits DAC (calibration DAC) sets the amplitude of a pulse that can be injected with a test capacitance (Cc) of 20 fF to the front-end.
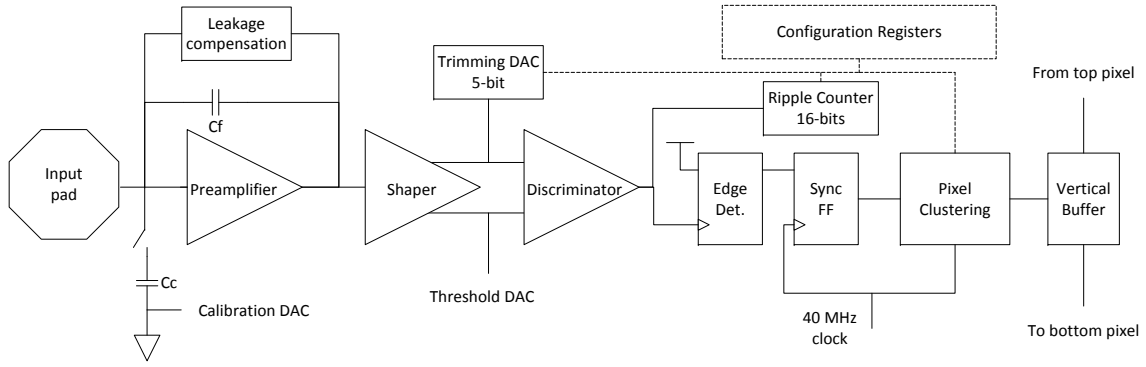
Figure 3. Pixel front-end. Dashed lines represent configuration signals.

The output of the discriminator connects to an edge detector followed by a flip-flop which synchronizes the pulses from the front-end with the 40 MHz clock. Before being transmitted to the periphery, the pixel data is reduced by the pixel clustering logic: pixel clusters larger than ~4 pixels cannot be generated by high transverse momentum particles and consequently such clusters are immediately discarded; the clusters within the defined range are instead reduced to the centre of the cluster, called centroid. The centroids are transmitted to the periphery with a fixed latency of two clock cycles.

For testing purposes, a 16-bits ripple counter connects to the discriminator output and is read out at the end of each acquisition. Configuration registers allow to disable this counter, the binary readout and the pixel clustering logic as well as to define the width of clusters accepted by the pixel clustering logic and the values for threshold equalization.

2.3 Periphery back-end

The chip periphery includes the logic shown in figure 4. It performs the quick recognition of high p_T particles using the Stub Finding logic described in details in [6]. The logic includes cluster reduction/elimination, position offset correction, coordinate sparsification and correlation logic. The block receives the pixel data from the front-end and the strip data from an external input. The strip interface runs at a frequency of 160 MHz with a strobe signal for synchronization. A deserializer prepares this data for the Stub Finding logic.

The data processing elements are pipelined. Registers store one step of the data path according to the processing mode chosen during configuration. The available modes allow to store the data from the front-end, the coordinate from the pixel encoders or the stubs from the stub sorter. A time-stamp, representing the cycle counter from the acquisition start, identifies the saved data.

The MPA-Light can also emulate the functionalities of the SSA, i.e it works as a readout chip for strip detectors, by OR-ing the pixel columns. When it is set in this mode, a serializer block sends the strip data at 160 MHz to the output. A strobe signal is generated for data synchronization.

The Stub Finding logic allows evaluating on silicon the timing and power performances obtained in simulation. Furthermore, the SSA emulator mode can be used to build a reduced size module with the capability of performing quick recognition of high p_T particles using only MPA-Light ASICs.
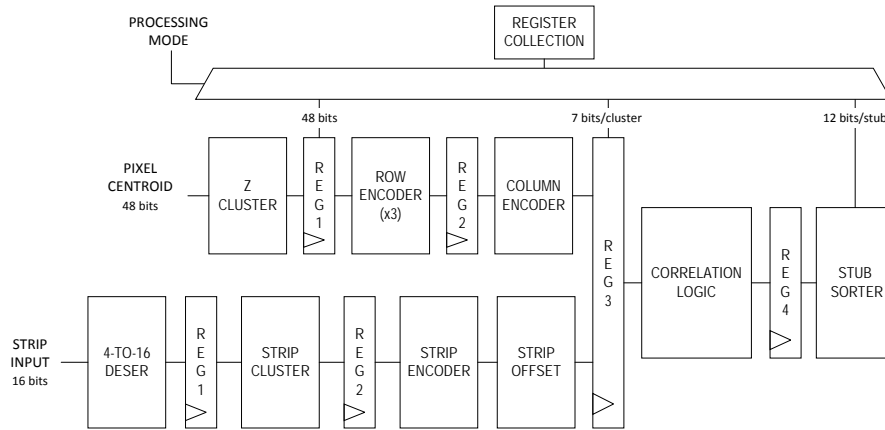
Figure 4. Periphery schematic.

3 Electrical characterization

The MPA-Light was submitted for production and the first batch was available at the beginning of 2015. Ten samples were tested so far and proved functional. A custom test set-up was developed to test and characterize the MPA-Light. It includes a mezzanine board holding the chip, an interface board for voltage and current generation and monitoring, an FPGA development board and a command line interface program running on a Linux PC. The characterization was performed using the internal test capacitor in a bare chip, without connection to a sensor. The quantity of charge injected is determined by the relationship $Q_i = C_c V$, where V is the voltage determined by the calibration DAC in the periphery. A wire-bond connection allows the measurement of the calibration DAC voltage which provides a Least Significant Bit (LSB) value of 0.035 fC when an ideal value of 20 fF is assumed for C_c and an Integral Non-Linearity (INL) $< \pm 0.5$ LSB. Power consumption confirms the simulation values, in particular the analog front-end provides a consumption of ~25 μA per channel.

3.1 Front-end characterization

A 5-bits threshold-equalization DAC per pixel allows to correct for the pixel-to-pixel threshold mismatch. Figure 5 shows the number of events counted while scanning the threshold voltage for each possible value of the 5-bits DAC. The measured dynamic range is 90 LSB (~ 9.5 ke$^-$) and the INL is ± 0.2 LSB. The r.m.s threshold variation before equalization is 16 LSB (~ 1.7 ke$^-$), while afterwards the achieved noise free variation is 0.8 LSB (~ 95 e$^-$) as shown in figure 6.

The σ of the gaussians in figure 5 corresponds to the Equivalent Noise Charge (ENC). Its distribution is shown in figure 7b and provides an r.m.s value of 1.5 LSB (~162 e$^-$). The minimum detectable charge can be calculated by quadratically adding the measured electronic noise and the threshold variation because both measurements are uncorrelated. The quadratic sum of mismatch and noise is 1.7 LSB (~175 e$^-$). After threshold equalization, the 6σ minimum threshold could be set at 10.2 LSB (~1.1 ke$^-$).
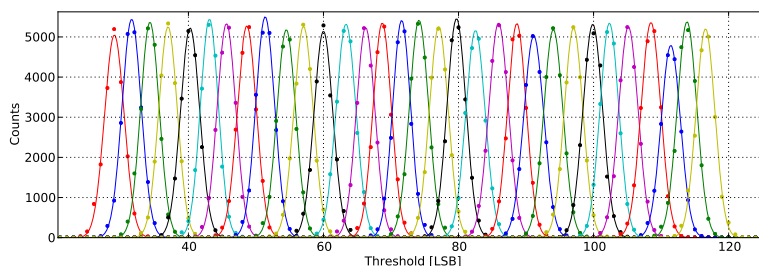
Figure 5. Baseline scan of a pixel for the 32 different DAC codes of the trimming DAC.
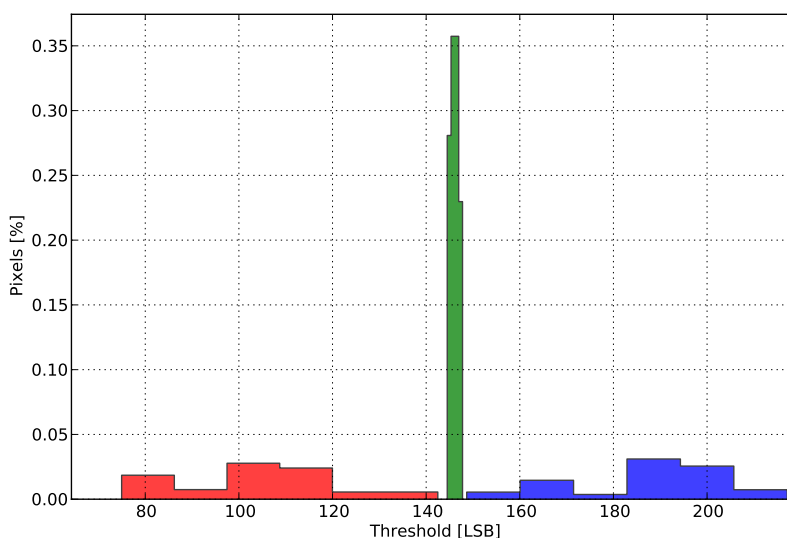

Figure 6. Red and blue histograms show the threshold distribution of all pixels with the minimum and maximum DAC codes; the green histogram shows the same distribution for calibrated matrix.

Figure 7a plots the S-curve of the whole pixel matrix for different pulse amplitudes. A thousand pulses are injected for each value of threshold. Threshold equalization is optimized for values between 0.5 fC and 1.5 fC since this is the range expected during operation. Complementary error function fitting allows the extraction of the S-curve mid-point which is the effective threshold. The front-end gain can be calculated from the distance among the effective threshold for different input charges. The measured gain is 85 ±5 mV/fC.

The binary readout allows timing characterization of the analog front-end. Charge injection time scans for different threshold values provide the shaper output as shown in figure 7c. Peaking time is 24 ±1.6 ns as expected from simulation. An important parameter to ensure correct operation at 40 MHz is the front-end time walk. It is measured as the difference between charge injection time and detection by the edge detector in the front-end. Figure 7d shows the measurements with thresholds at 0.5 fC and 1 fC which give a walk time < 15 ± 1.6 ns over a charge range from 0.5 to 9 fC. The characterization of the front-end provides results very close to simulations. Consequently, the front-end respects all the requirements and can be used without further optimization in the MPA.
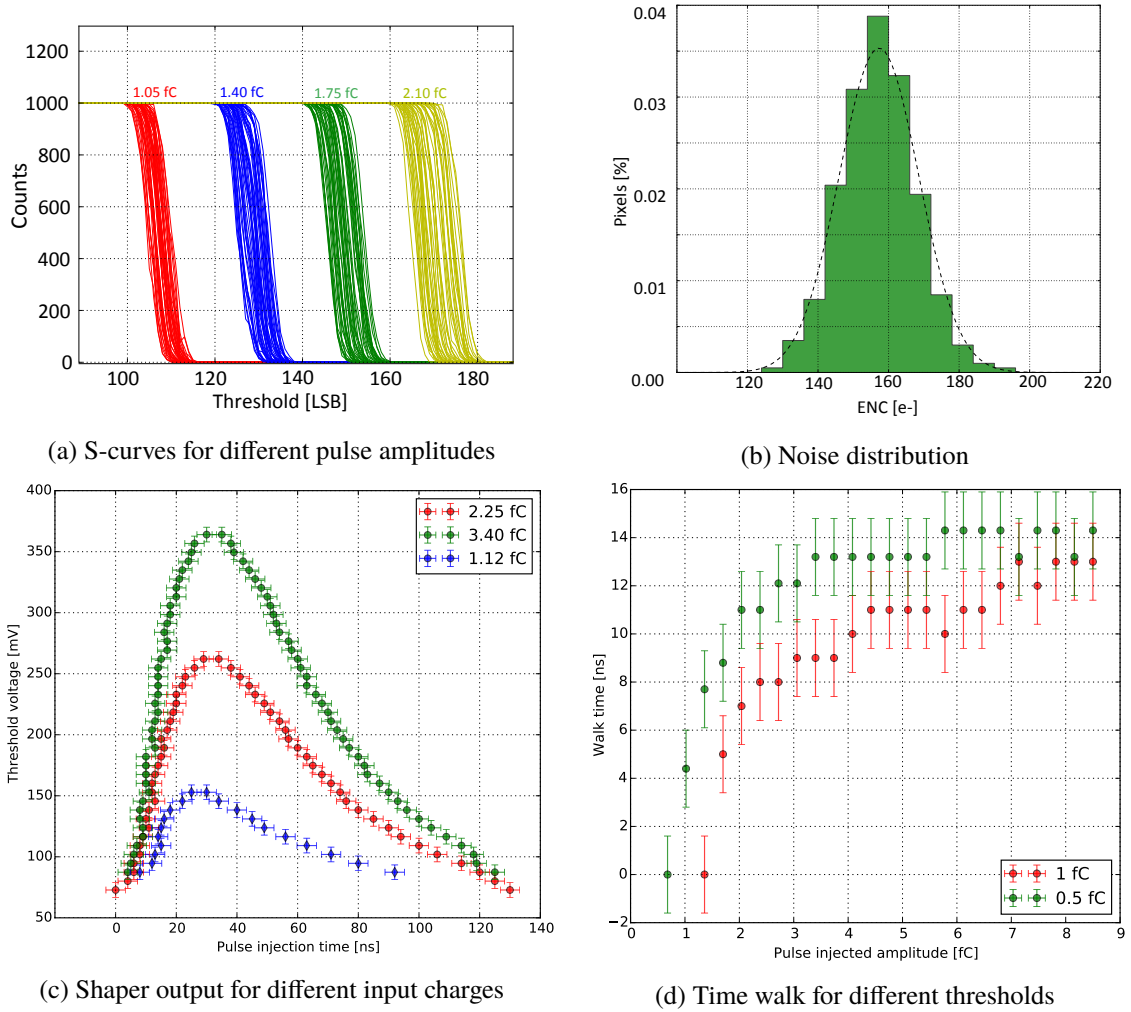
(a) S-curves for different pulse amplitudes

(b) Noise distribution

(c) Shaper output for different input charges

(d) Time walk for different thresholds

Figure 7. Front-end characterization results.

3.2 TID irradiation

The MPA is expected to be exposed to a Total Ionizing Dose (TID) smaller than 100 MRad. The MPA-Light ASIC was exposed to X-rays up to 150 MRad with a dose rate of 105 kRad/min. After the irradiation, the chip was annealed for 24 hours at 100 °C under bias. During the entire procedure, the test system monitored power consumption, front-end performance and digital logic. At 150 MRad the analog power consumption variation was −7 % while it was −4 % after annealing. The digital logic test consisted in pass/failure checks at different doses which did not show any fail up to 150 MRad. Minor variations were observed on the analog blocks: the calibration DAC LSB variation was −3 % at 150 MRad, but it increased up to −7 % after annealing (figure 8a); the threshold LSB extracted from S-curves degraded up to −15 % at 150 MRad, while it partially recovered after annealing providing a final variation of −11 % (figure 8b). The large dynamic range of the global DACs allows to correct easily the observed variations. Consequently, the MPA-Light did not show any problem with X-ray TID irradiation up to 150 MRad.
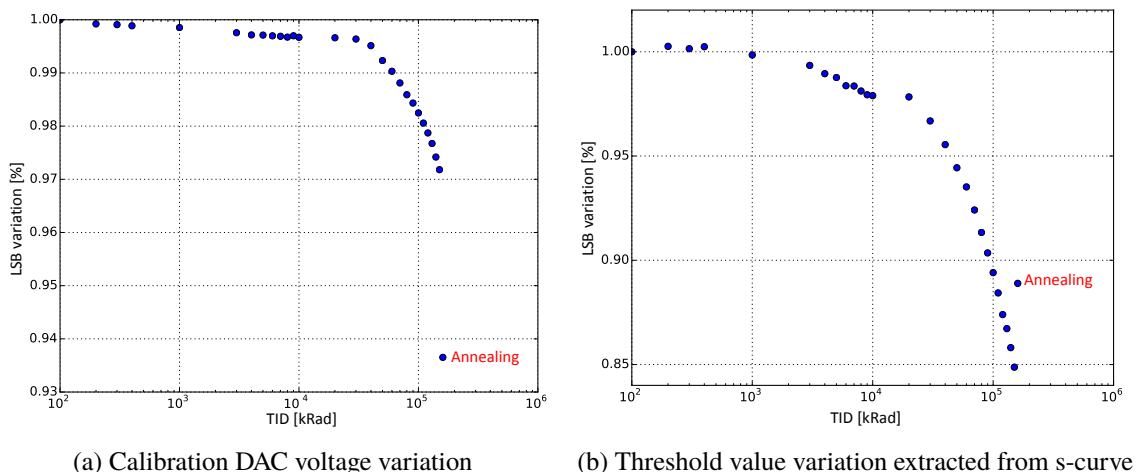
(a) Calibration DAC voltage variation

(b) Threshold value variation extracted from s-curve

Figure 8. TID irradiation results.

4 Summary

The MPA-Light chip has been designed using a commercial 65 nm CMOS technology with a macro pixel cell of $100\,\mu\text{m} \times 1446\,\mu\text{m}$. The Stub Finding logic for quick recognition of high transverse momentum particles was included and performed as expected. Front-end characterization with test pulses matched simulations closely, with a pixel-to-pixel threshold spread of $95\,\text{e}^-$ r.m.s. after equalization, an ENC of $165\,\text{e}^-$ r.m.s., a peaking time of 24 ns and a walk time < 15 ns. Irradiation with X-rays up to 150 MRad did not show any problems.

In conclusion, the success of the MPA-Light is a very important step in the MPA project because it provides a proof of the complete front-end for the next iteration and proves the feasibility of the Stub Finding logic in hybrid pixel detector with the given power budget.

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