CERN-ACC-2015-0110

Davide.Aguglia@cern.ch

Grid Interface Design for the Compact Linear Collider (CLIC)

Marija Jankovic, Alan Watson, Jon Clare, Pat Wheeler
The University of Nottingham, Nottingham, United Kingdom
Davide Aguglia
CERN, Geneva, Switzerland,

Keywords: <Converter control>, <Modular Multilevel Converters>, <Pulsed power converter>, <Power supply>, <Power quality>

Abstract

This paper discusses the grid interface challenges for CERN's proposed Compact Linear Colliders' (CLIC) klystron modulators, including a 280 MW power system optimisation. The modular multilevel converter is evaluated as a candidate topology for a Medium Voltage grid interface along with a control method for reducing the impact of klystron modulators on the electrical network.

Presented at: EPE 2015, 7-10 September 2015, Geneva, Switzerland

Geneva, Switzerland
October, 2015

Grid Interface Design for the Compact Linear Collider (CLIC)

Marija Jankovic[1], Alan Watson[1], Jon Clare[1], Pat Wheeler[1], Davide Aguglia[2]
[1]The University of Nottingham
School of EEE - University Park, NG7 2RD, Nottingham, UK
Tel.: +44 115 74 84462
eexmj8@nottingham.ac.uk; alan.watson@nottingham.ac.uk; jon.clare@nottingham.ac.uk;
pat.wheeler@nottingham.ac.uk
www.nottingham.ac.uk/
[2]CERN – European Organization for Nuclear Research
CERN, CH-1211 Geneva 23, Switzerland
Tel.: +41 22 767 55 49
davide.aguglia@cern.ch
home.web.cern.ch/

Keywords

<Converter control>, <Modular Multilevel Converters>, <Pulsed power converter>, <Power supply>, <Power quality>

Abstract

This paper discusses the grid interface challenges for CERN's proposed Compact Linear Colliders' (CLIC) klystron modulators, including a 280 MW power system optimisation. The modular multilevel converter is evaluated as a candidate topology for a Medium Voltage grid interface along with a control method for reducing the impact of klystron modulators on the electrical network.

Introduction

The CLIC is a high energy linear accelerator under feasibility study at CERN [1]. It is based on the two beams acceleration principle where the drive beams are accelerated using around 1300 klystrons operating with high voltage short pulses. The drive beams acceleration power is therefore pulsed in nature, with a 38 GW peak power (~29 MW per klystron) for 140 µs of pulse length and a repetition rate of 50 Hz [2]. The klystron modulators comprise of a capacitor bank which is discharged through a high voltage pulse transformer via the use of a solid state switch [2]. The grid interface of klystron modulators should recharge the capacitor banks between pulses and ensure that a constant average power of approximately 280 MW is drawn from the grid despite of the pulsed operation of the klystron modulators. As a result, the grid interface acts as a firewall, blocking the effect of the pulsed operation from reaching and impacting the electricity network.

The grid connection at CERN is at the transmission voltage level of 400 kV, while the capacitor bank voltages are in the range from 6 kV to 20 kV. The 1300 klystrons are distributed along a 2 – 2.5 km path, thus a well-structured power system must be designed considering both spatial and electrical distribution constraints. The power system is optimised to ensure the best trade-off between system efficiency, cost and accelerator availability. The solution should be feasible, i.e. within technical constraints. The power system structure and power electronics design considerations are presented in [3]. The power system optimisation outcomes are an optimal structure (i.e. number of converters, transformers, bus bars, etc.) and the most suitable voltage levels.

Power electronics and control design should ensure low AC power fluctuation and good regulation of the capacitor banks voltages. The AC power fluctuation should be below 2 %, regardless of the pulsed nature of the capacitor banks. This can be achieved either with converter control algorithms which will be presented here, or with a so called Fast Voltage Corrector (FVC) principle shown in [4].

The first optimisation results, presented in [5], indicate usage of multilevel topologies, in particular Modular Multilevel Converters (MMC), due to their higher efficiency, superior waveform quality and inherent capability for cell redundancy when compared to traditional topologies, such as two- or three-level converters [6, 7].

This paper focuses on the final stage of power system optimisation, including the cost of power system components, in order to define precise voltage levels and converter ratings. The final capacitor bank voltage level selection will compromise both charger and pulse forming system design (active bouncer [8] and pulse transformer [9]). Furthermore, the power electronics interface and control design are discussed. The focus is on the MMC converter under pulsed load. The MMC is commonly found in the literature in the back-to-back configuration typical for HVDC transmission system [10], where it brings huge benefits in comparison to other topologies. This paper highlights the benefits of MMC in this application.

Power system design

Both power system and power electronics should be considered together in order to find the optimal feasible solution. The optimisation diagram is depicted in Fig. 1. The inputs to the optimisation process are the specifications on the grid and klystron modulator side together with the technical constraints. These specifications relate to the voltage ratings, grid power quality, short circuit ratio, DC voltage repeatability, etc. The technical constraints relate to maximum fault currents of standard circuit breaking equipment, standard industrial cable ratings and transformers and also the spatial limitations at CERN. Based on those, global design rules are set, and power structure defined.

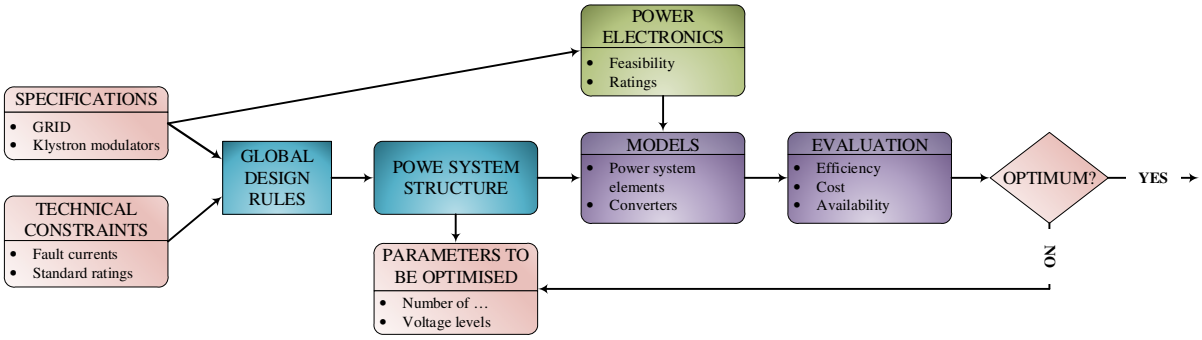


Fig. 1: Optimisation algorithm.

The power system structure considered as the most suitable for CLIC application includes step down transformers and AC/DC converters as illustrated in Fig. 2. To step down the voltage from 400 kV to medium voltage (MV) level oil insulated transformers are used, while in the second stage from MV to lower MV (LMV) level dry type transformers are used. The first MV level is defined at 30 – 33 kV which corresponds to 36 kV cables and 38 kV standard switchgears (bus bars). The LMV level V_{AC} is defined by the DC voltage V_{DC}, in equation (1). Considering DC voltages from 6 to 20 kV, suitable AC voltage levels are driven by 3.6 kV, 7.2 kV and 12 kV standard cables (3.3, 7.2 and 12 kV switchgear).

$$V_{AC} \leq \sqrt{3} \cdot \frac{1}{\sqrt{2}} \frac{V_{DC}}{2} \tag{1}$$

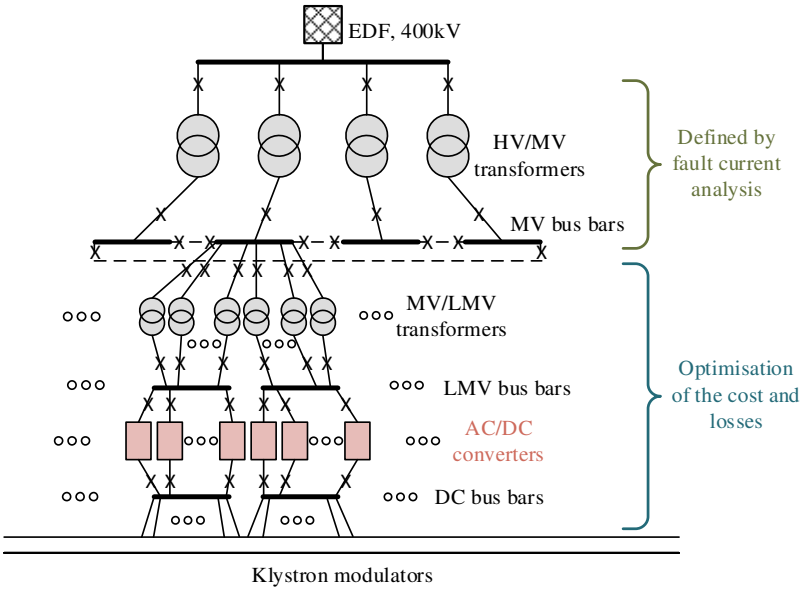


Fig. 2: Power system structure.

The presented structure has a certain amount of redundancy at each voltage level in order to maximise availability of the converter. Achieving redundancy, i.e. increasing availability of the accelerator, is one of the design rules. At the LMV level and the DC bus bars, n+1 redundancy is applied, meaning that in case of failure of one component feeding the bus bars, the remaining n components will be able to manage the power of the failed component. At the MV bus bars, paralleling of transformers at a common bus bar is not applied since this would increase fault currents, so the redundancy is provided from neighboring bus bars. The presented solution does not apply redundancy on the bus bars, i.e. in the case of bus bar failure the power system cannot be reconfigured to deliver power to all klystron modulators. In [5] the solution with parallel bus bars, providing higher availability of the accelerator, with an increase of cost, is introduced. The availability of the power system is estimated using fault tree analysis [11] and it has been shown that all considered solutions with single bus bar structure have similar unavailability of about 170 min/year while structures with parallel bus bars have unavailability of about 30 min/year.

The maximum fault currents in the case of short circuit on the MV or LMV level are limited to 20 kA which is the breaking current of standard MV circuit breakers. Based on the results from [5], the number of MV bus bars is fixed at 6, while the number of LMV bus bars is 6 in the case of 12 kV switchgear and 12 in the case of 7.2 kV switchgear. In the case of lower LMV voltages the fault currents at these bus bars are beyond the breaking capabilities of standard devices.

In [5] the efficiency of the overall system is observed for all solutions satisfying the maximum fault currents criteria. The results indicate that the overall system efficiency above 97.4 % is achieved for all solutions employing multilevel converters. Solutions employing NPC converters do not comply with the fault currents criteria (3.6 kV LMV), and the overall efficiency is around 96 % which is on the borderline of the specifications.

Having 6 distributed MV bus bars, the system can be divided into 6 equivalent sectors. Each sector starts with one MV bus bar at 30-33 kV that supplies a certain number of MV/LMV transformers at one or two LMV bus bars (depending on the voltage), as presented in Fig. 3. Each LMV bus bar supplies a certain number of AC/DC converters at one DC bus bar. Based on the losses and cost analysis, the most suitable LMV (AC) and DC voltage levels and number of converters per sector are selected.

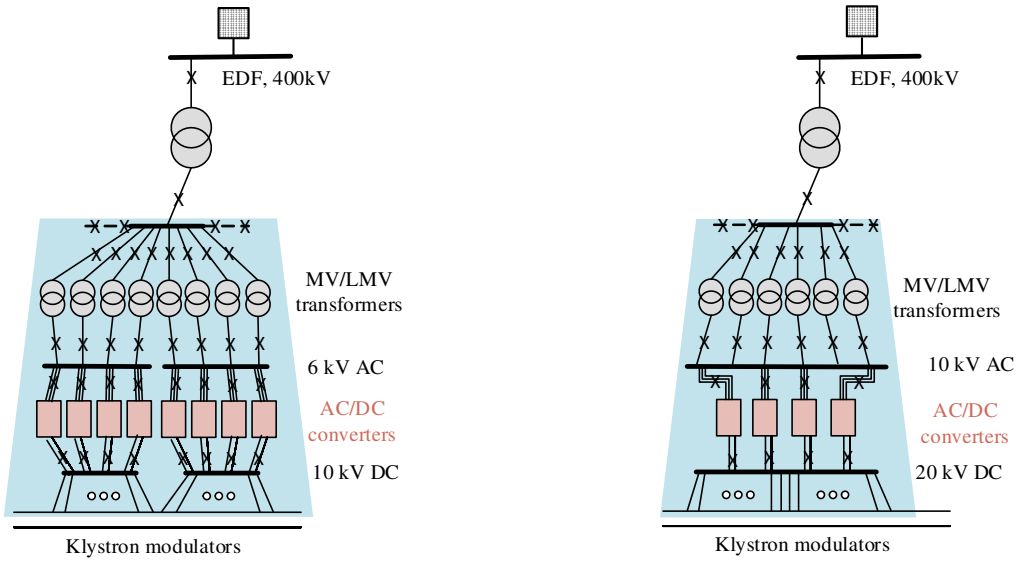


Fig. 3: One sector layout in the case of a) lower voltage range and b) higher voltage range.

The cost is estimated by taking into account available price details and models of all power system components, such as transformers, cables and converters (IGBTs, capacitors, etc). The price of enclosed rack switchgears used as bus bars is not yet included in calculations. The cost of civil engineering, including the surface galleries for cable placement and buildings for power electronics and switchgear, is included in the optimisation. The price details are taken from CERNs internal resources, as well as online available catalogues. Since the most significant amount of losses and cost relates to the power electronics, converter modeling is performed in more detail, as presented in next subsection.

Converter modeling

The first optimisation results indicated that the MMC is the most suitable topology. Since the optimisation should cover wide range of converter powers, and two ranges of possible DC and AC voltages, the selection of the components should be defined by the converter ratings. All IGBTs are rated at 1.7 kV, which corresponds to the converter cell voltages of 1 kV. The IGBTs for the MMC of the specific rating are selected on the basis of rated switch current. The cell capacitors are sized according to the amount of energy that needs to be stored in a MMC for a certain power rating. The amount of energy stored in the converter cells is given with the capacitance constant described by (2) [12, 13]:

$$H = \frac{3 \cdot 2 \cdot N \cdot E_{cell}}{P_{rat}} = \frac{3 \cdot C_{cell} \cdot V_{DC}^2}{N \cdot P_{rat}} \tag{2}$$

Where N is the number of converter cells per arm, E_{cell} is the energy stored in each cell, P_{rat} is the rated converter power, V_{DC} is the DC voltage and C_{cell} is the cell capacitance. The capacitance constant has a dimension of time, and the selected value is 40 ms, which implies that converter stores the energy that will be fully dissipated after delivering nominal power for 40 ms.

From [13] the resonance with arm inductance and cell capacitance happens for the specified value of arm inductance given by equation (3).

$$L_{res} = \frac{N}{C_{cell}(2\pi \cdot f)^2} \frac{2\left(h^2 - 1\right) + m^2 \cdot h^2}{8h^2\left(h^2 - 1\right)} \approx k_1 \frac{V_{DC}^2}{P_{rat}} \tag{3}$$

Where f is fundamental frequency of the grid, h is the harmonic order, m the modulation index and k_1 is a constant parameter. The harmonics of interest are even: 2, 4, etc. The study in [13] shows that the values of L_{arm} and C_{cell} should be such so that resonance is avoided, since it produces higher ripple in

cell voltages. The arm inductance L_{arm} is selected to have somewhat higher (30 %) inductance than the resonance inductance L_{res} at the second harmonic (h = 2 and f = 50 Hz).

The losses in the converter are divided into losses in passive components (capacitors and inductors) and losses in the active components (IGBTs and diodes). The losses of the active components are further divided into switching and conduction losses and are estimated using [14] and verified through the simulation. The switching frequency of the lower voltage MMC is set to 6500 Hz, where, the switching frequency of 20 kV DC converter is 5000 Hz. The losses are dependent on the converter rated and nominal power and rated voltage, and characteristics of the semiconductors used.

For the purpose of modelling the losses in the capacitance, an Equivalent Series Resistance (ESR) of 1 mΩ is assumed to be the only source of losses. The arm inductor is modelled as air cored inductor, known as Brooks coil [15], using copper plates. The series resistance is estimated on the basis of copper resistance.

The price of the IGBTs and cell capacitors are based on the available catalogue data [16, 17], while the price of arm inductors is estimated on the basis of current price of copper. The capacitors cost is estimated with an estimation of 0.1 $ per 1 µF for the film capacitor rated at 1 kV. From (2) it can be concluded that energy stored in cell capacitors ($6N \cdot E_{cell}$) is proportional to the converter power, meaning that the energy stored in all converters in the system would be proportional to the overall rated power. In that sense, if the price of capacitors is proportional to the energy stored in them, the price of all cell capacitors in the system should be similar regardless the converter power and voltage ratings. The differences come due to the converters overrating and availability of only discrete values of capacitances (E12 series). Similar conclusions can be drawn about the energy stored in arm inductors. The nominal current of an arm inductor is one third of the DC current, so the nominal energy stored in arm inductors is given by (4):

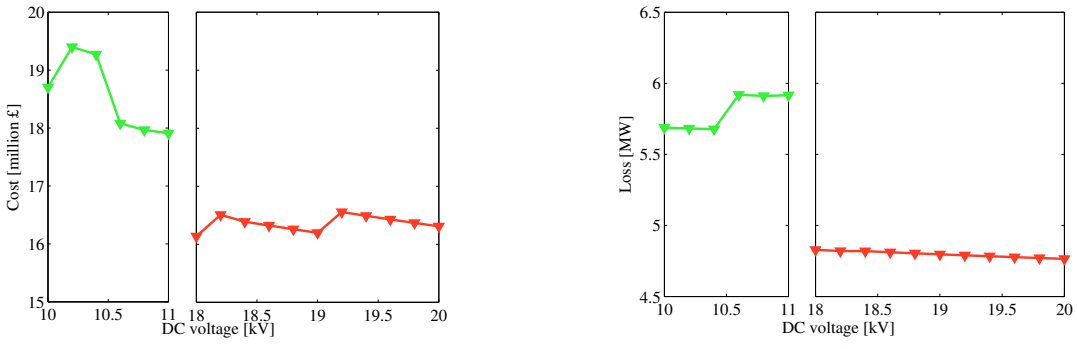
$$6E_{arm} = 6 \cdot \frac{1}{2} L_{arm} \left(\frac{I_{DC}}{3} \right)^2 = \frac{1.3}{3} \cdot k_1 \frac{V_{DC}^2 \cdot I_{DC}^2}{P_{rat}} = k_2 \cdot P_{rat} \tag{4}$$

Where k_2 is a constant parameter. Considering this, the energy stored in all the inductors of all MMCs in the system would be proportional to the system rated power, and it should not vary with the converter ratings. However, some differences in the inductors price are present as consequences of the inductor designs and converter overrating.

Optimisation results

Both price and losses should be minimised, so they are both normalised with their minimum values and then weighted with the same coefficient. For each of the possible MLV and DC voltage levels, the optimal number of transformers and converters is selected.

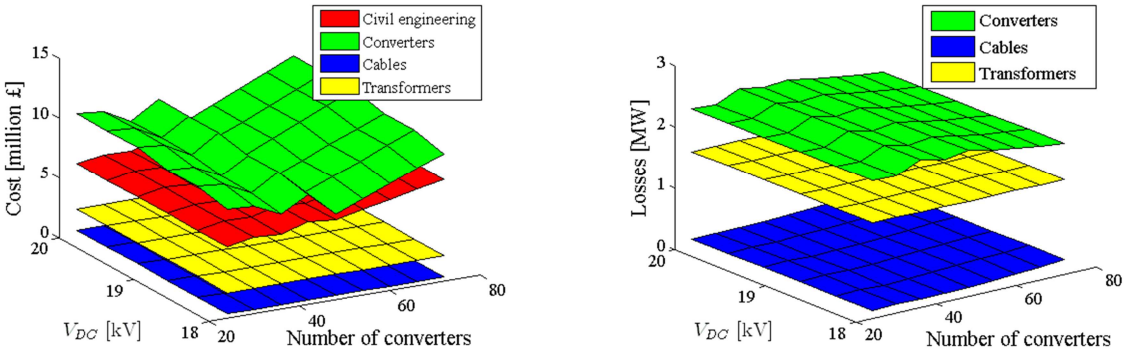
Fig. 4 shows optimisation results in terms of cost and losses of all 6 sectors, as a function of the final DC voltage level. The DC voltages between 11 and 18 kV are not observed, since there are no suitable cable and switchgear options for both LMV and DC voltage (1).



a) b)

Fig. 4: Power system a) cost and b) losses vs. V_{DC}, where green denotes lower and red higher voltage range.

As presented, both cost and losses are lower in the higher voltage range, i.e. when the DC voltage is from 18 to 20 kV (22 kV cables), when compared to lower voltage range (DC voltage between 10 and 11 kV – 12 kV cables). In the higher voltage range, the optimal number of converters is 48 giving that one DC bus bar is fed by 4 converters and it supplies about 220 modulators. Each converter is rated at 16.6 MW and nominally operates at 12.5 MW. In the higher voltage range, the influence of the DC voltage and number of converters on overall cost and losses in case of 36 MV/LMV transformers and fixed LMV voltage at 10.5 kV are presented in Fig. 5.



a) b)

Fig. 5: a) Cost and b) losses distribution as a function of number of converters and DC voltage.

Fig. 5 indicates that most of the power system cost is in converters and civil engineering, and the number of converters influences both the power electronics and civil engineering cost, while the influence of the DC voltage is not significant. The majority of losses also relates to converters, followed by the losses in MV/LMV transformers.

The power system optimisation algorithm hasn't included the load characteristics. The load is based on the periodical pulsed discharge of the capacitor banks. The active bouncer compensates the voltage droop in the klystron modulator, to ensure a flat top of the pulse [8]. The maximum voltage droop ΔV the bouncer can compensate is 1 kV, and the capacitor banks at the modulator input is sized according to that, as given by (5). The maximum voltage droop is about 10 % of the nominal voltage in the case of lower DC voltage range, and 5 % of the nominal voltage in the case of the higher voltage range. The feasibility of converter control and the influence of the DC voltage droop are discussed in the following chapter.

$$C_{in} \geq \frac{(T - t_{pul})P_{pul}}{\Delta V \cdot V_{DC}} \tag{5}$$

Considering the number of modulators, and the capacitance given with (5), the overall energy stored in main capacitor banks can be calculated. The energy stored in the main capacitor banks is directly proportional to the delivered power and the DC voltage, and inversely proportional to the voltage droop. In the case of the 1 kV droop, the energy stored in the system with the higher DC voltage (20 kV) will be twice of the energy stored in the 10 kV DC voltage system. This would influence the overall system cost, but since this is the part of modulators it hasn't been included in the optimisation process.

Converter control challenges

Multilevel topologies are selected due to demand for high efficiency, redundancy and good AC power quality. In addition, traditional two or three level topologies at specified voltage ratings would require series connected semiconductors which would further decrease the efficiency. Considering the power system structure and optimisation results, paralleling the outputs of 4 converters is applied on a common DC bus bar. From the control point of view, the parallel connection of MMCs act as one big converter with many phases, so the increase of control complexity is not expected.

The two main goals are achieving low AC power fluctuation and repeatable recharging of the capacitor banks. The capacitor banks provide attenuation of the pulsed power effect to approximately 80 – 90 %, giving the DC side power fluctuation of about 10 – 20 %. However, the AC power fluctuation needs to be further attenuated, and this can be achieved by either applying a FVC [4] or by the AC/DC converters control. Converter control can be designed to provide either enough bandwidth to attenuate DC power fluctuation requiring tracking 140 μs ramps, or suppression of AC power fluctuation despite presence of higher DC power fluctuation. Since the MMC possesses internally stored energy it is possible to achieve very low AC power fluctuation, by simply providing correct AC voltage waveforms on the AC sides.

By applying control methodology proposed in [13], the AC power fluctuation can be limited to satisfy specifications. The need for DC voltage control and other features of the application dictate somewhat modified control approach. Phase A of the MMC and the associated control algorithm are illustrated in Fig. 6. Each converter phase has two arms (*up* and *dn*) that are modulated with respect to the reference signals given by (6). The AC power control is realised through d-q current control and produces the AC voltage demands. Since the amount of power taken from the capacitor banks is imposed by the load, maintaining the energy stored in the converter implies the correction of the AC power reference (Fig. 6.b). On the DC side, the main DC voltage is controlled, providing the DC current reference, which is split to the phases (circulating currents). Additionally circulating current contains phase balancing component (blue rectangle) and arm balancing component (red rectangle). Circulating current control provides the compensation of the arm inductor voltages which when subtracted from the total DC voltage gives the DC voltage reference for arm modulation (Fig. 6.c).

$$v_{A,up}^{ref} = \frac{v_{DC,A}^{ref}}{2} - v_A^{ref} \text{ and } v_{A,dn}^{ref} = \frac{v_{DC,A}^{ref}}{2} + v_A^{ref} \tag{6}$$

Since the DC voltage contains the voltage droop with the repetition rate of 50 Hz, the pulse affects different phases with a different phase shift. During the pulse AC references for upper and lower arm are opposite, thus the voltage droop affects the two arms within the phase differently. In the case of a different pulse repetition rate, e.g. the pulse frequency of 100 Hz would not cause imbalances within the phase, while the pulse frequency of 300 Hz would affect all phases (and arms) equally. If the phase and arm balancing algorithm are not applied, the voltage droop in the DC voltage will cause the imbalances in the arm power. Imbalances in the arm power are causing the imbalances in the cell capacitor voltages, which may lead to overmodulation of the arm with lower cell capacitor voltages and distortion in AC power. The upper arm power of the phase A is given by (7). Based on the equation for arm powers averaged over 20 ms, the 50 Hz circulating current component can be computed.

$$p_{A,up} = -v_{A,up} \cdot i_{A,up} \approx -\left(v_{DC,A}^{ref} \Big/ 2 - v_A^{ref} \right) \left(i_{A,circ}^{ref} + i_A^{ref} \Big/ 2 \right) \tag{7}$$

The phase angle of the circulating current should be shifted by $\pi/2$ with respect to the angle of the DC voltage ripple 50 Hz component, i.e. all three phases will have the same angle. This means that the average converter DC power is not influenced regardless 50 Hz component ripple in the DC current. The calculated amplitude (it can be negative) of the 50 Hz component in the phase A circulating current is given by (8).

$$I_{A,circ50} = \frac{\frac{V_{DC50} \cdot I_m \cos\left(\varphi_{v50} - \varphi_{A,i}\right)}{4}}{V_m \cos\left(\varphi_{v50} - \frac{\pi}{2} - \varphi_{A,v}\right) - \frac{L_{arm} \cdot \omega \cdot I_m \cos\left(\varphi_{v50} - \varphi_{A,i}\right)}{2}} \tag{8}$$

Where V_{DC50} and φ_{v50} are amplitude and angle of the 50 Hz component in the DC voltage ripple, V_m and $\varphi_{A,v}$ are amplitude and angle of the phase A voltage reference, I_m and $\varphi_{A,i}$ are amplitude and angle of the phase A current reference, L_{arm} is arm inductance and ω is the grid angular frequency. The

calculated amplitude is different for different phase, and the DC current ripple will have a 50 Hz component. The calculated amplitude is used as a feedforward term, to the PI controller ensuring that the average cell voltages of the upper and lower arm are equal.

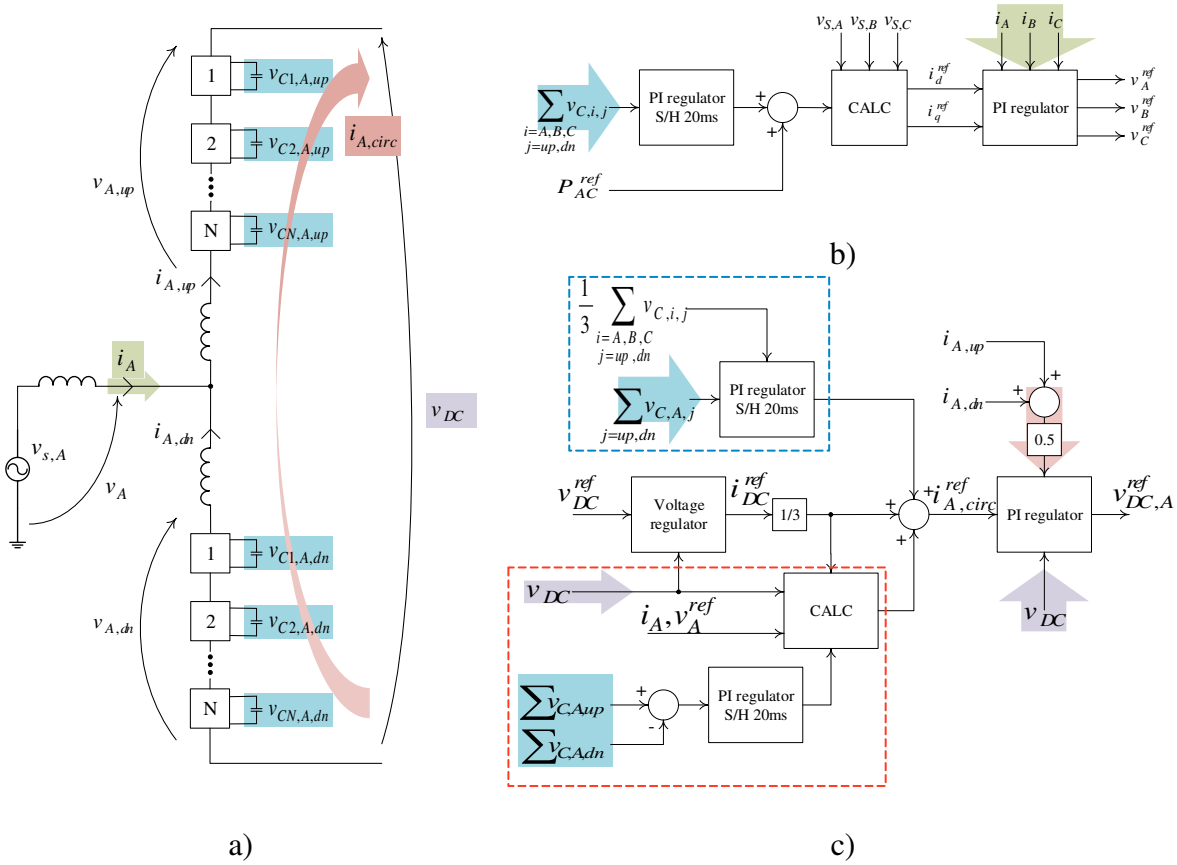


Fig. 6: a) The MMC – one phase representation; b) AC and c) DC side control.

The phase balancing loop ensures that the average cell voltages of all three phases are equal. The corrections in circulating current are purely DC and the sum of three phases is equal to zero, so that the converter DC power is not influenced.

The results obtained in the PLECS simulation environment are presented in Fig. 7 for a 16 MW MMC, providing average DC voltage of 20 kV. The DC voltage droop is 1 kV, and the pulse position is 0.524 rad shifted with respect to the phase A source voltage zero crossing. The converter has 20 cells per arm, giving 41 levels in AC voltage, and thus good quality AC voltage waveforms (Fig. 7.b). The achieved AC power fluctuation is below 1 %, which satisfies the specifications (Fig. 7.a). Fig. 7 shows a low 50 Hz component in the DC current ripple and the DC power fluctuation. This is due to the pulse position not affecting any of the phases severely. Different pulse positions would require higher 50 Hz component in one of the circulating currents.

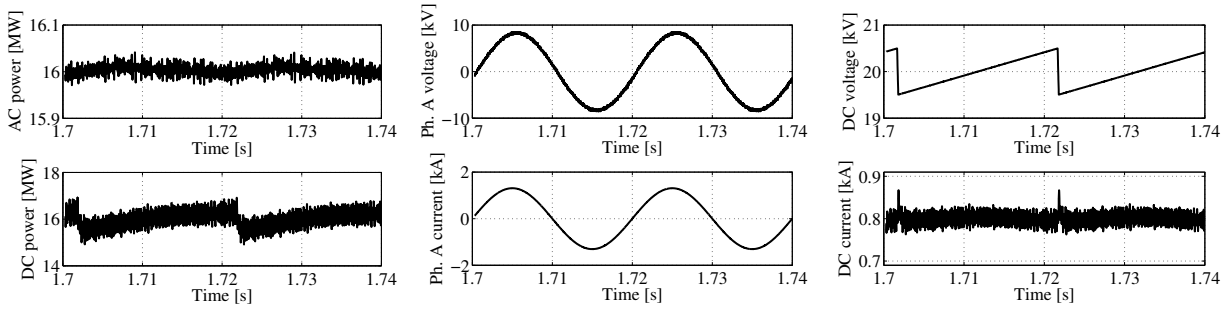


Fig. 7: a) AC and DC power; b) Phase A voltage and current and c) DC voltage and DC current.

Some of the pulse positions would have the denominator of (8) of some phase close to or crossing zero. In this case, the circulating current amplitude of that phase would get higher, and might change sign. In those situations balancing of the cell capacitors voltages is not possible. The AC and DC power fluctuation depending on the pulse position for one third of the cycle are presented in Fig. 8. As it is shown, there are two critical points for the AC power fluctuation minimisation, giving 6 critical points in the period. The pulse position will be synchronised to the grid voltages, thus, its position could be in a point where low AC power fluctuation can be achieved. Fig. 8 also presents the comparison of the control feasibility of 10 kV and 20 kV DC voltage MMC, for the DC voltage droop of 5 % and 10 %, and the DC current of 800 A. In non-critical points, the AC power fluctuation is below 1.5 % in all of the presented cases, and below 1 % in the case of the 5 % voltage droop. The 10 kV converter has benefits of less energy stored in the klystron modulators capacitor bank for the maximum voltage droop, but as a consequence higher AC power fluctuation is present. The DC power fluctuation is also dependent on the voltage droop, and it depicts the amplitude of the 50 Hz current in the DC current ripple and circulating currents.

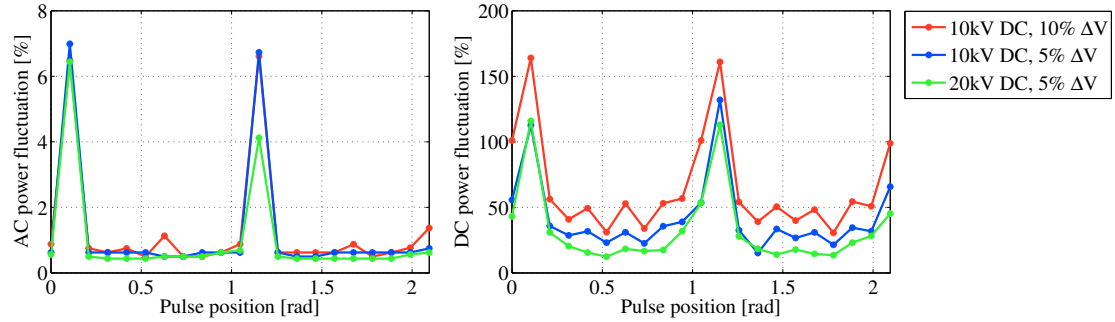


Fig. 8: AC (left) and DC (right) power fluctuation vs. pulse position for different converter ratings and relative DC voltage droop.

The pulse forming system is emulated with the pulsed current source, which is completely repeatable and ideal and it doesn't cause the DC voltage disturbances. However, realistic pulse forming system would not discharge the capacitor banks equally during each pulse, and some actions should be undertaken to achieve pre-pulse repeatability. The presented results relate to the DC voltage controller based on a PI controller with a 20 ms sample and hold at the output, giving the constant DC current reference. In the case sample and hold is not applied, the voltage controller will give the DC current reference that contains 50 Hz component. This component should be taken into account when forming circulating current references, so that the cell voltages are still balanced. PI based DC voltage controllers control the average, rather than peak DC voltage. One possibility of controlling the peak voltage is feeding forward the energy taken during pulse to the DC current reference.

Conclusion

The paper gave an insight to the challenges of the grid interface of klystron modulators, aimed for the CLICs drive beams acceleration. First, the specifications are presented, with highlights of both overall power system characteristics and grid power and DC voltage quality constraints.

A detailed analysis of power system distribution and optimisation parameters is presented. The influence of the number of converters and DC voltage level on the overall system price and losses is examined. The power system optimisation results are favouring the 20 kV DC voltage region. However, in the higher voltage region, more energy needs to be stored in klystron modulators capacitor banks for the same DC voltage droop. In that case the relative voltage droop is lower, which improves the AC power fluctuation.

The MMC topology proved to be suitable due to its high efficiency and modularity, high AC voltage quality and the ability to separate AC and DC side control. The MMC was analysed under pulsed load conditions. The principles of the control method are presented, together with supporting simulation results. The simulation results indicate AC power fluctuation below 1 % despite higher DC power

fluctuation and pulsed discharge of the DC capacitor banks. However, the proposed control method is limited to some pulse positions. Namely, there are six points within grid voltages period in which the low AC power fluctuation cannot be achieved. Since the pulse position is synchronised to the grid, there is a possibility to place the pulse in the convenient regions. The proposed control algorithm can be applied in cases of different DC voltage control algorithms, including those that control the peak voltage (pre-pulse repeatability) and those that control the mean DC voltage. The control concepts will be proven on the scaled-down experimental prototype and this will be the topic of some future papers.

References

[1] D. Dannheim, P. Lebrun, L. Linssen, D. Schulte, and S. Stapnes. "CLIC e+e- Linear Collider Studies - Input to the Snowmass process 2013," in Proc. of Snowmass on the Mississippi, Minneapolis, USA, CD-ROM paper, 2013.

[2] D. Aguglia, C. A. Martins, M. C. Bastos, D. Nisbet, D. Siemaszko, E. Sklavounou, and P. Viarouge, "Klystron modulator technology challenges for the Compact Linear Collider (CLIC)," in Proc. of IEEE Pulsed Power Conference (PPC), Chicago, USA, pp. 1413-1421, 2011.

[3] M. Jankovic, A. Watson, J. Clare, P. Wheeler, and D. Aguglia, "Grid interface challenges and candidate solutions for the Compact Linear Collider's (CLIC) klystron modulators," in Proc. of IEEE Pulsed Power Conference (PPC), San Francisco, USA, CD-ROM paper, 2013.

[4] F. C. Magallanes, D. Aguglia, P. Viarouge, C. de Almeida Martins, and J. Cros, "Design of a Solid-State Fast Voltage Compensator for klystron modulators requiring constant AC power consumption," in Proc. of Int'l Power Modulator High Voltage Conf. (IPMHVC), Santa Fe, USA, CD-ROM paper, 2014.

[5] M. Jankovic, A. Watson, J. Clare, P. Wheeler, and D. Aguglia, "Optimal Power System and Grid Interface Design Considerations for the CLICs Klystron Modulators," in Proc. of Int'l Power Modulator High Voltage Conf. (IPMHVC), Santa Fe, USA, CD-ROM paper, 2014.

[6] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in Proc. of IEEE Power Tech Conference, Bologna, Italy, CD-ROM paper, 2003.

[7] P. Rodriguez, M. D. Bellar, R. S. Munoz-Aguilar, J. Rocabert, and A. Luna, "Multilevel-clamped multilevel converters (MLC2) - an alternative approach for multilevel power conversion," in Proc. of IEEE Ind. Electr. Soc. Conf. (IECON), Melbourne, Australia, pp. 4433-4438, 2011.

[8] F. C. Magallanes, D. Aguglia, P. Viarouge, C. de Almeida Martins, and J. Cros, "A novel active bouncer system for klystron modulators with constant AC power consumption," in Proc. of IEEE Pulsed Power Conference (PPC), San Francisco, USA, CD-ROM paper, 2013.

[9] S. Candolfi, P. Viarouge, D. Aguglia, and J. Cros, "Finite element based optimal design approach for high voltage pulse transformers," in Proc. of IEEE Pulsed Power Conference (PPC), San Francisco, USA, CD-ROM paper, 2013.

[10] M. Saeedifard and R. Iravani, "Dynamic Performance of a Modular Multilevel Back-to-Back HVDC System," in IEEE Trans. on Power Delivery, vol. 25, pp. 2903-2912, 2010.

[11] M. Čepin, "Assessment of Power System Reliability: Methods and Applications," Springer London, 2011.

[12] M. Hagiwara and H. Akagi, "Control and Experiment of Pulsewidth-Modulated Modular Multilevel Converters," in IEEE Trans. on Power Electronics, vol. 24, pp. 1737-1746, 2009.

[13] M. Zygmanowski, B. Grzesik, and R. Nalepa, "Capacitance and inductance selection of the modular multilevel converter," in Proc. of *Power Electronics and Applications (EPE),* Lille, France, 2013.

[14] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless, scalable Modular Multilevel Converters for HVDC-transmission," in Proc. of IEEE Power Electronics Specialists Conference. (PESC), Rhodes, Greece, pp. 174-179, 2008.

[15] P.N. Murgatroyd, "The Brooks inductor: a study of optimal solenoid cross-sections," in Proc. of *IEE Electric Power Applications,* vol 133, pp. 309-314, 1986.

[16] Website of Dynex semiconductors. (Available on http://www.dynexsemi.com/product-area/igbt-modules/).

[17] Website of NWL capacitors (Available on http://www.nwl.com/products/capacitors/).