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Novel Active Bouncer Topology for Klystron Modulators based on Pulsed Transformers

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Active droop compensation systems, so called active bouncers, for klystron modulators based on monolithic pulse transformers perform the regulation of the output pulse voltage while simultaneously withstand all the primary current of the modulator. This imposes the utilization of high power semiconductors which can produce high switching losses and degrade the overall system efficiency. In order to overcome this issue, this paper proposes a new active bouncer topology based on the parallel connection of two different power converters: the first one is in charge of handling the majority of the primary current at high efficiency, and the second one is used to fine tune the bouncer voltage via a high bandwidth converter rated at a fraction of the first parallel connected converter. Detailed comparison between a classical active bouncer and two variants of the proposed topology are presented and based on numerical simulations.

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Abstract

Active droop compensation systems, so called active bouncers, for klystron modulators based on monolithic pulse transformers perform the regulation of the output pulse voltage while simultaneously withstand all the primary current of the modulator. This imposes the utilization of high power semiconductors which can produce high switching losses and degrade the overall system efficiency. In order to overcome this issue, this paper proposes a new active bouncer topology based on the parallel connection of two different power converters: the first one is in charge of handling the majority of the primary current at high efficiency, and the second one is used to fine tune the bouncer voltage via a high bandwidth converter rated at a fraction of the first parallel connected converter. Detailed comparison between a classical active bouncer and two variants of the proposed topology are presented and based on numerical simulations.

Introduction

The need for klystron modulators with improved performances, mainly for new linear accelerators, is growing more and more nowadays. Several existing klystron modulator topologies have been explored in the literature [1, 2, 3, 4, 5]; however, the vast majority of operational ones is based on the controlled discharge of a pre-charged capacitor bank. Therefore one of the options to achieve a precise square flat-top consists in increasing the size of the main capacitor bank, such that it experiences a limited voltage droop during the discharge. This option becomes inadvisable for medium and long pulse klystron modulators, specially taking into account not only the cost, but also the size and safety related to the stored energy. As an alternative solution, droop compensation systems or "bouncers", able to compensate a fraction of the capacitor nominal voltage (voltage droop during the pulse), have been proposed and successfully used in practice.

One of the topologies retained as a candidate for the CLIC Drive-Beam klystron modulators at CERN is based on a monolithic pulse transformer, as illustrated in Figure 1. In order to produce the required *180kV* pulse, the main capacitor bank C_{main} is pre-charged to a voltage of approximately *15kV* and discharged through a step-up transformer by closing the main switch S_1. C_{main} is dimensioned such it

experiences a voltage droop of approximately *1kV* during the pulse. In order to compensate this voltage

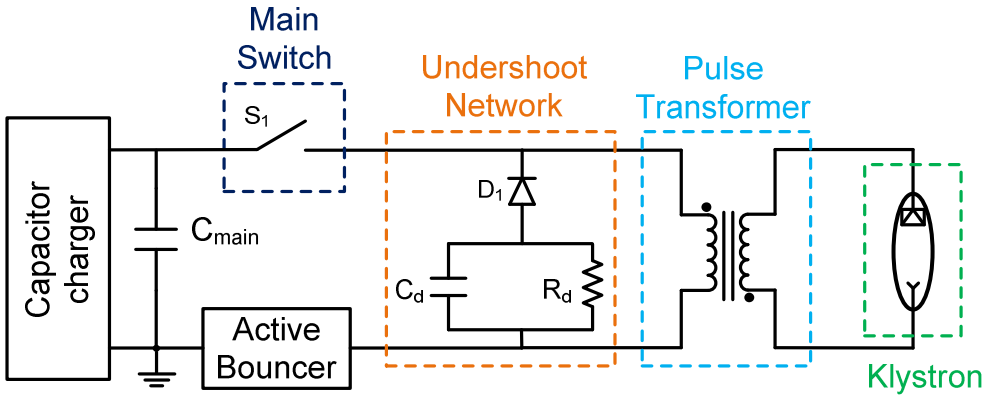

Fig. 1: Klystron modulator topology based on a monolithic pulse transformer.

droop, as well as the voltage across the transformer winding resistances and leakage inductances during the pulse (influenced also by the magnetizing current), an active bouncer circuit is installed in series with the main capacitor bank and the primary of the pulse transformer.
In this case a simple undershoot network guarantees a proper de-magnetization of the pulse transformer (which is equipped with a DC bias circuit for an inverse pre-magnetization action) between two consecutive pulses.
Table 1 shows the klystron modulator challenging specifications for the Compact Linear Collider (CLIC) [8], currently under study at CERN. We observe a rise time from *0V* to *180kV* of only *3μs*, a settling time of *5μs*, and a flat-top stability of 0.85% for a *140μs* flat-top length. The total complex will include several hundreds of these modulators synchronously pulsing and, therefore, modulator size, efficiency and cost must be optimized.

Table 1 CLIC Modulator's output pulse specification

Nominal pulse voltage	V_{kly}	180 kV
Nominal pulse current	I_{sn}	160 A
Pulse peak power	P_{mod_out}	28.8 MW
Rise & fall times	t_{rise}, t_{fall}	3 μs
Settling time	t_{set}	5 μs
Flat-top length	t_{flat}	140 μs
Repetition rate	RR	50 Hz
Voltage overshoot	V_{ovs}	1 %
Flat-Top Stability	FTS	0.85 %
Repeatability	REP	10-50 ppm

Active bouncer topology overview

Neglecting some non-linearity, the klystron behaves as a resistive load. Therefore, the modulator ideally produces a perfect current pulse. A common practice in klystron modulators consists in placing the droop compensation system in series with the main capacitor bank [6], as shown in Figure 1. However, this configuration presents an issue in applications where the rise time of the pulse is short, as when the main switch closes all the modulator current will suddenly flow into the bouncer filter capacitor, discharging it as presented in [7]. The bouncer is not able to compensate this modulator current perturbation until the current in its output filter inductances rises to the same current value, as illustrated in Figure 2.A). This perturbation must be taken into account when dimensioning the active

bouncer output filter. In [6] an active bouncer circuit with a diode connected in parallel to the output filter capacitor, as illustrated in Figure 2.B), was proposed to prevent its discharge to negative values.

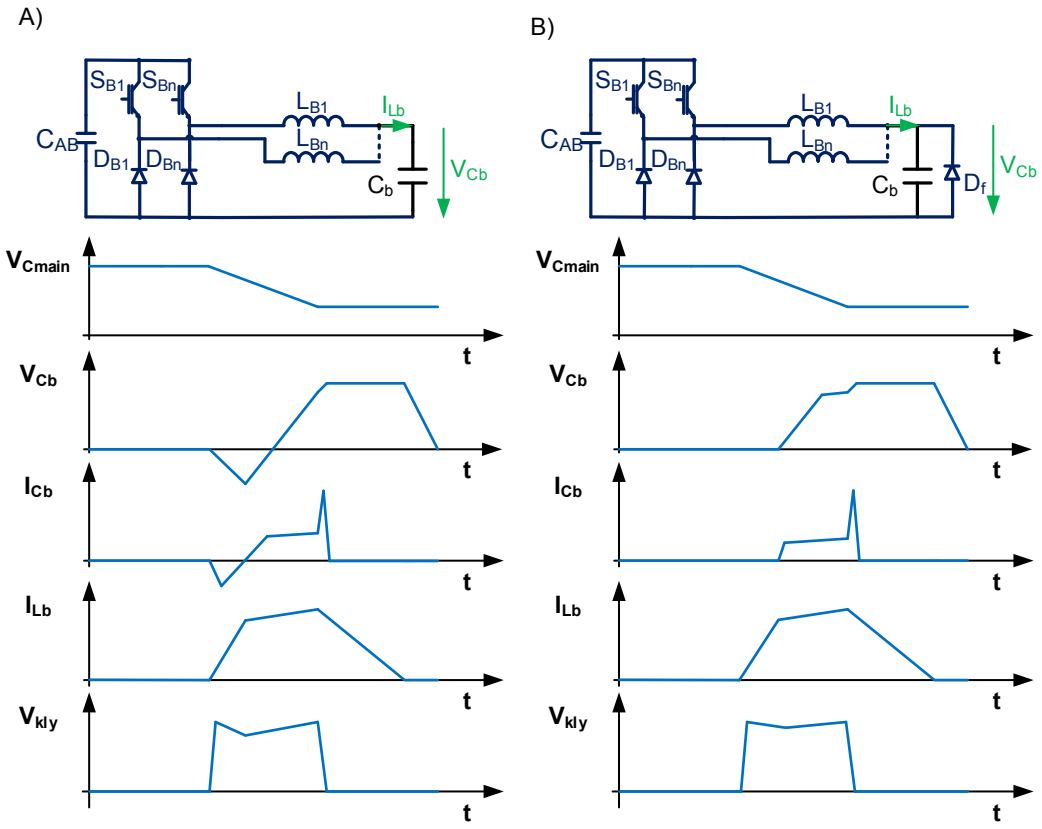

Fig. 2: Typical active bouncer topologies and associated simplified waveforms: A) Multiphase buck converter; B) Multiphase buck converter with blocking diode in parallel with the output filter capacitor.

However, in this configuration the active bouncer is still not able to charge the output filter capacitor to positive voltage values until its output current exceeds the modulator current. Therefore, this configuration is only suitable as a protection for long rise time modulator pulses. A different solution able to initialize the active bouncer output current and speed up the start of the droop compensation action in short rise time applications has to be addressed.

Proposed active bouncer topology features

In order to avoid the effects of the modulator current perturbation in short rise time applications previously introduced, the topology scheme of Figure 3 is proposed. Figure 4 illustrates the operation phases described hereafter:

1.-Current initialization: The switch S_{SC} is closed and the active bouncer topology provides V_{AB}. The current I_L rises.
2.-Pulse step-up: S_1 closes. V_{kly} rises and I_L continues to increase.
3.-Flat-top: Once V_{kly} achieves its nominal value, S_{SC} is opened and the active bouncer topology is controlled to produce an output voltage ramp on $V_{bouncer}$ to compensate for C_{main} discharge.
4.-Recovery: S_1 is opened. The pulse transformer is demagnetized through the branch composed by R_d, C_d and D_1. $V_{bouncer}$ increases its value until it equals V_{AB} voltage. Once this happens, the diode D_f is forward-biased, so the energy stored in L_b is recovered back to C_{AB} passing through the diode D_f and the free-wheeling diode(s) of the active bouncer topology.
5.-Reset: Once I_L drops down to 0V, C_b is discharged through R_R by closing S_R.

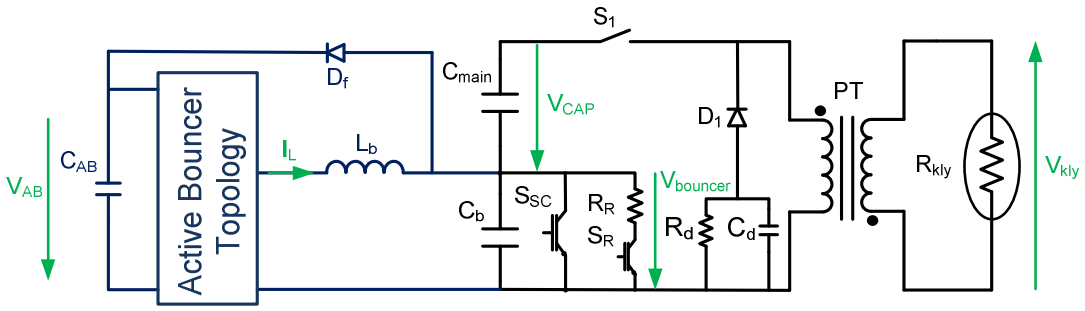

Fig. 3: Proposed topology scheme of the active bouncer.

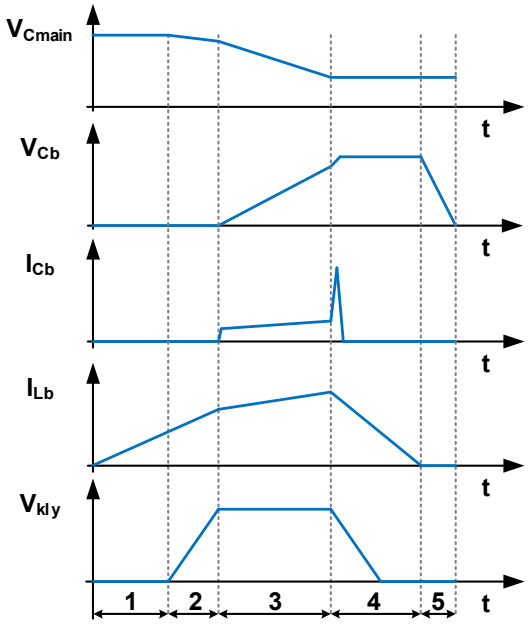

Fig. 4: Operational phases of the proposed topology.

Since S_{SC} remains permanently closed during the pulse-step up, and neglecting the voltage drop across the switch, in order to achieve the nominal current value after the rise time, the current I_L at the beginning of phase 3 must be:

$$I_L(0) = I_P - t_{rise}\frac{V_{AB}}{L_B} \quad (1)$$

where I_P is the nominal primary current of the modulator. Therefore, the initialization of the current must be triggered at the time calculated in (2) before closing S_1.

$$t_{trig\_init} = \frac{L_b}{V_{AB}} I_p - t_{rise} \quad (2)$$

Proposed active bouncers topologies

Description of the proposed active bouncers

Three topologies, illustrated in Figure 5, have been selected as candidates for the active bouncer. The first one (Figure 5.A) is based on a common multiphase buck-converter topology, as the one presented in [6]. The second and the third consist of a combination of power converters. They both share a common high-current and low switching-frequency stage, which manages all the modulator current. In

addition, a second low-current high-bandwidth stage whose only task is to produce a voltage ramp on the bouncer output filter capacitance to compensate for the main capacitor voltage discharge, is connected in parallel. On the topology shown in Figure 5.B, this low-current stage consists of a high switching-frequency buck converter; whereas on the one shown in Figure 5.C, the low current-stage consists of a power MOSFET operated in its linear region.

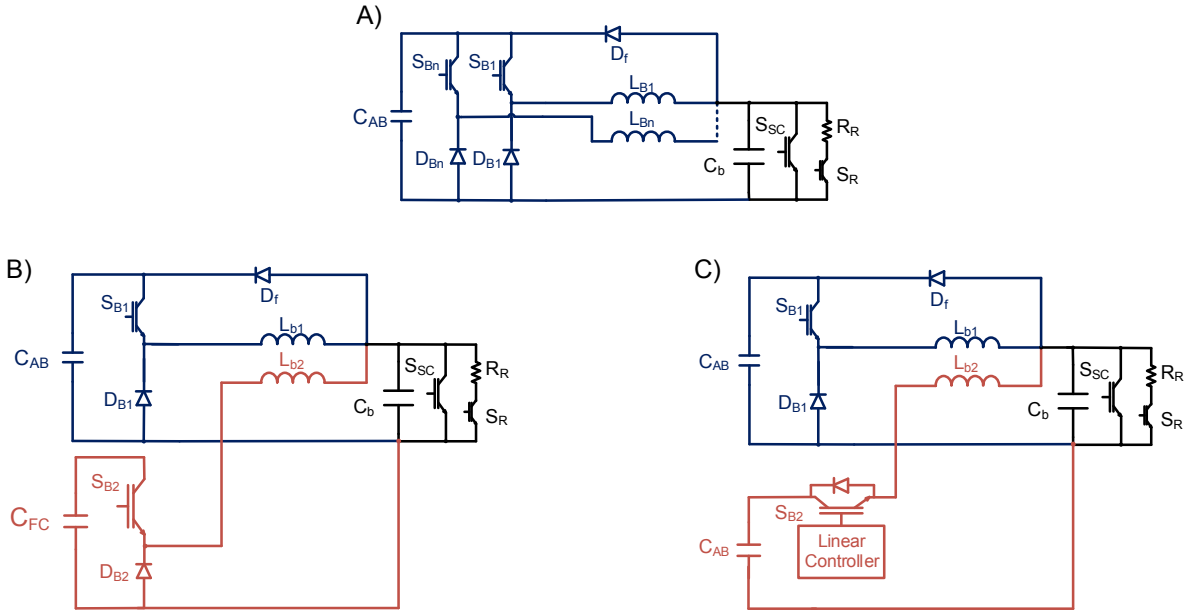

Fig. 5: Active bouncer topology candidates: A) Topology #1: Multiphase buck converter; B) Topology #2: Solution with high-current low switching-frequency buck stage combined with a low current high switching-frequency buck stage; C) Topology #3: Hybrid solution with high-current low switching-frequency buck stage and low current linear stage.

Design and performances comparisons

In order to evaluate their performances, the three topologies have been studied and optimized to respect CLIC specifications, fixing the modulator parameters presented in Table 2. Hysteretic controllers have been selected for controlling the switching stages, whereas for the linear stage a PI controller is used. The dimensioning procedure was based on a non-linear optimization approach where all the active bouncer component values (including the number of phases) and the controller parameters were considered as optimization variables. The constraints were the ones presented in Table 1, and the objective function to be minimized was the total active bouncer losses during a complete cycle. In order to reduce the computation time, simplified thermal (switching and conduction losses were evaluated for different 1700V IGBT models) and control (bandwidth, gain and phase margins) design models were used. Results were subsequently validated via numerical simulation. Table 3 presents the active bouncer optimized parameter values for the CLIC specifications.

Table 2 Fixed modulator parameters

Primary Voltage	15 kV
Main capacitor bank size	350 µF
Primary winding leakage inductance	9 µH
Primary winding equivalent resistance	11 mΩ
Secondary winding leakage inductance	9 µH
Secondary winding equivalent resistance	11 mΩ
Magnetizing Inductance	0.122 H

Table 3 Optimized Parameters for Bouncer Topologies

Topology	Topology #1	Topology #2	Topology #3
Number of phases	4	3 x High Current Stage 4 x Low Current Stage	3 x High Current Stage 1 x Low Current Stage
Switching frequency per phase	62.5 kHz	26.3 kHz High Current Stage 110.5 kHz Low Current Stage	26.3 kHz High Current Stage
Inductance value per phase	100 µH	1.8 mH High Current Stage 200 µH Low Current Stage	1.8 mH High Current Stage 1 µH Low Current Stage
C_b	1 µF	1 µF	1 µF
R_{bd}	0.5 Ω	0.3 Ω	Not required
C_{bd}	4 µF	4 µF	Not required

Figures 6, 7 and 8 show a zoom on the pulse obtained by numerical simulation for topologies 1, 2 and 3, respectively. The optimized topology #1 consists of a 4 phases buck converter using 1700V, 800A, IGBTS FZ800R17KF6C_B2 from Infineon. The maximum current and switching frequency per phase are 497A and 62.5 kHz, respectively. It is necessary to damp the LC output filter with a typical C_{bd}-R_{bd} parallel damping branch of C_{bd}=4µF and R_{bd}=0.5Ω to avoid subharmonic oscillations. The performances achieved at the secondary output are a voltage stability of 67 V and an equivalent frequency ripple of 250 kHz.

The optimized topology #2 is composed of a 3 phases high-current converter using the same 1700V, 800A, FZ800R17KF6C_B2 IGBTs from Infineon with a maximum current and switching frequency per phase of 644.3A and 26.3kHz; and a 4 phases low-current converter using 1700V, 60A, BSM50GS120DN2 from Infineon, with a maximum current and switching frequency per phase of 19A and 110kHz, respectively. A passive C_{bd}-R_{bd} damping branch is still required with values of C_{bd}=4µF and R_{bd}=0.3Ω. The performances achieved at the secondary output are a voltage stability of 49.39V and an equivalent frequency ripple of 442 kHz.

The optimized topology #3 is composed of a 3 phases high-current converter using the same 1700V, 800A, FZ800R17KF6C_B2 IGBTs with a maximum current and switching frequency per phase of 644.3A and 26.3kHz; and a low-current linear MOSFET stage with a closed-loop bandwidth of 1MHz and a maximum output current of 60A. The damping is performed by the linear stage, so no additional C_{bd}-R_{bd} passive damping branch is required in this case. The performances achieved at the output are a voltage stability of 44V and an equivalent frequency ripple of 71 kHz.

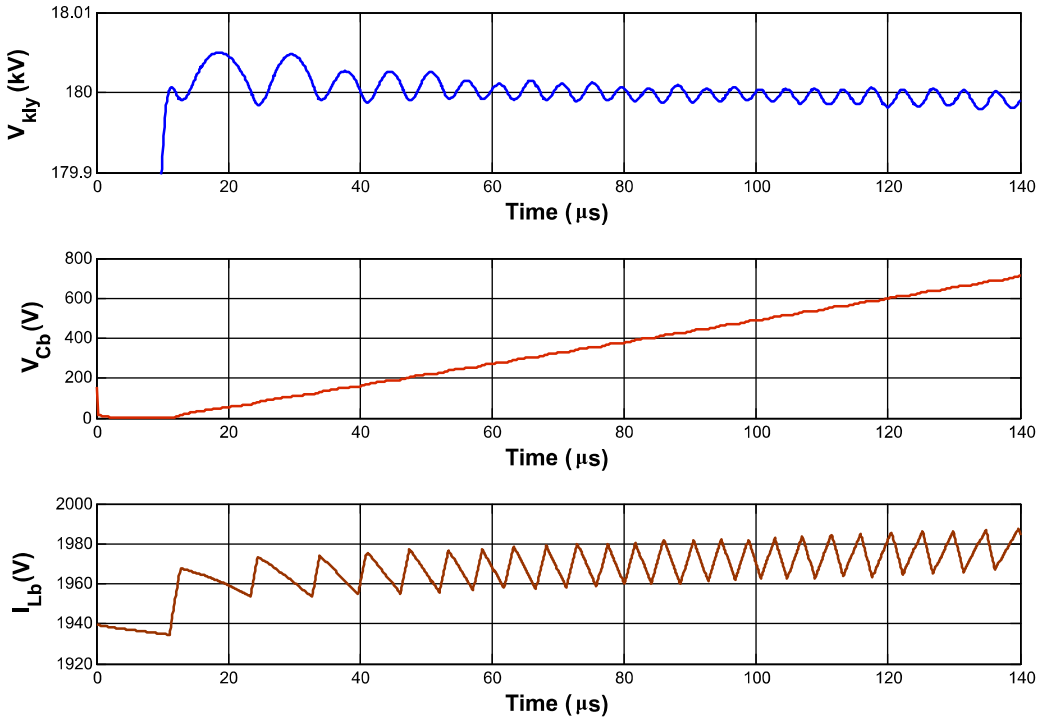

Fig. 6: Topology #1 numerical simulation results on CLIC specifications.

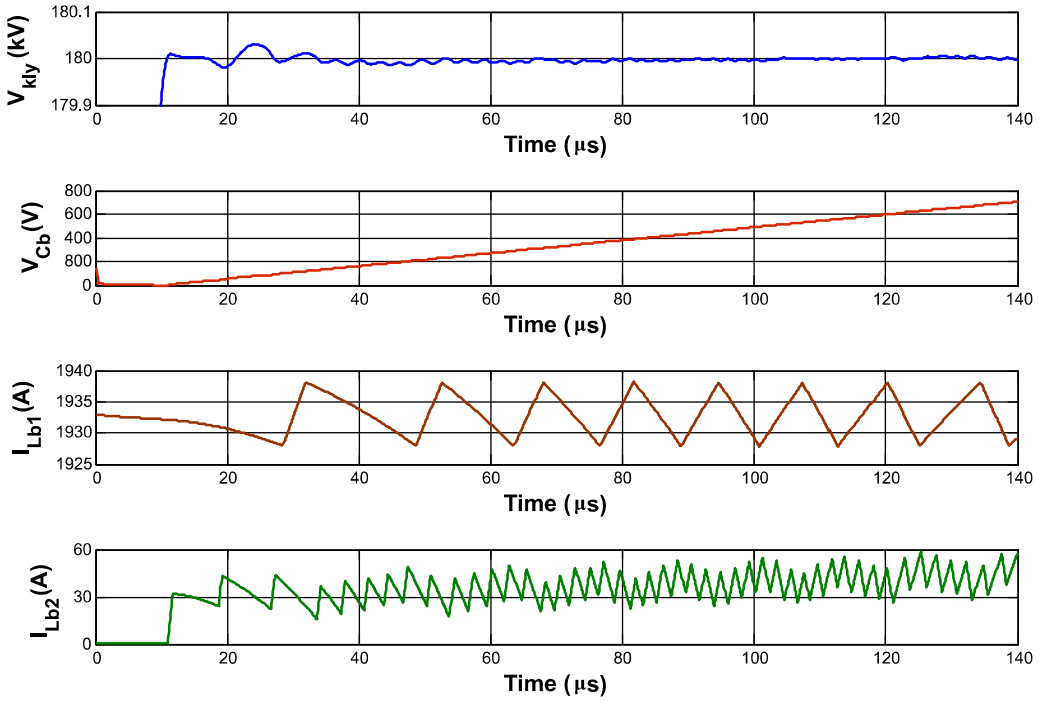

Fig. 7: Topology #2 numerical simulation results on CLIC specifications.

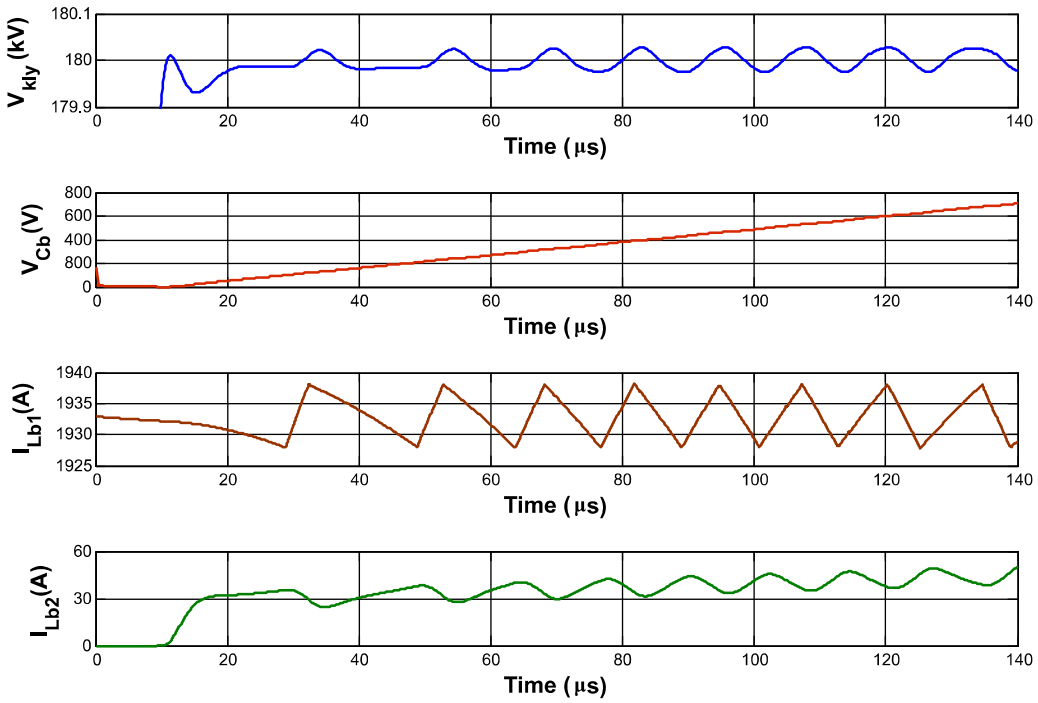

Fig. 8: Topology #3 numerical simulation results on CLIC specifications.

Table 4 summarizes and compares the characteristics and performances achieved by the different topologies evaluated by means of numerical simulations. We observe how Topologies #2 and #3 increase the filter inductance value of the high-current stage to reduce the switching frequency and, therefore, minimize the switching losses present in Topology #1. Topology #3 is the one providing the best performances, due to the high bandwidth of the linear converter. Although the average losses during the pulse are higher on Topology #3 due to the operation of the power MOSFET in its linear region, the lower losses on the bouncer reset (output filter capacitor discharge between pulses) due to the absence of the damping branch (composed of C_{bd} and R_{bd}), make this topology also the most efficient. In addition, the lower switching frequency harmonic content at the output makes possible to correct possible repeatability issues on the power system by means of a feedback loop on the low level RF control [9], in order to respect the challenging CLIC repeatability specifications (see Table 1). Therefore, topology #3 seems to be the most convenient one for the future CLIC klystron modulator active bouncer.

Table 4 Active bouncer topologies comparison

	Topology #1	Topology #2	Topology #3
Nº of phases High Current Stage	4	3	3
Nº of phases Low Current Stage	-	4	1
Av. Losses during the pulse	985 W	446 W	490W
Av. Losses on current rise	7.3 W	43.6 W	43.6 W
Av. Losses on current fall	13 W	70 W	70 W
Av. Losses on bouncer reset	110 W	110 W	30 W
Total average losses	1.12 kW	670 W	633 W
Energy recovered through diode D_f	0.20 J	55 J	55.5 J
Passive damping required?	Yes	Yes	No
Output ripple frequency	250 kHz	442 kHz	71 kHz

Total $LI^2/2$	193.45 J	1.12 kJ	1.2 kJ
Capacitor bank size	54 mF (1kV)	60 mF (1kV)	60 mF (1kV)
Output stability at 180kV	67 V	50 V	44 V
Redundancy modules required	1 module	2 modules	2 modules
Control & Electronics complexity	Medium	Medium	Low
Main challenges/difficulties	Control Loop	Control+HF stage	MOSFET stage

Conclusion

The proposed active bouncer topologies are able to comply with very fast rise time and very repeatable klystron modulators. The solution which combines a high current – low switching frequency stage with a low current - fast switching one, reveals better performances than a classical multiphase interleaved power converter active bouncer. Indeed the majority of the active bouncer current is managed by a much higher efficient power converter, and the fine voltage droop regulation is performed via a highly dynamical, and small sized, power converter. Topology #3 achieves better performances than topology #2 due to the higher bandwidth of the linear stage, and higher efficiency due to the absence of a parallel damping branch in its output filter which must be discharged between two consecutive pulses. The lower switching frequency harmonic content of Topology #3 makes also possible to compensate possible repeatability errors by means of a feedback loop on the low level RF control, in order to respect the challenging repeatability specifications of CLIC. Therefore, for the specific case of CLIC application, topology #3 would be the best solution.

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