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charles-mathieu.genton@cern.ch

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Charles-Mathieu Genton, Stefano Rocca, Fulvio Boattini
CERN, Geneva, Switzerland,

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Charles-Mathieu Genton, Stefano Rocca, Fulvio Boattini
CERN, European Organization for Nuclear Research
1211 Geneva 23, Switzerland
Tel: +41 22 766 31 15
charles-mathieu.genton@cern.ch, stefano.rocca@cern.ch, fulvio.boattini@cern.ch
http://www.cern.ch

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Abstract

In the frame of the LHC Injectors Upgrade (LIU) project, a new main power supply (MPS) for the PSBooster accelerator is required. The largest element of the new MPS is the 18 MW main power converter (MPC). The paper presents the design of the MPC control software, using Rapid Control Prototyping.

1. Introduction

The PS Booster (PSB) is the first circular accelerator of the LHC injection chain. It receives particles from the Linac (linear accelerator), increases their energy and sends them to the Proton Synchrotron (PS) ring to be further accelerated on their way to the LHC. A multi-megawatt power converter supplies the PSB magnets to provide the necessary centripetal force to the particles turning around in the accelerator. As a mean to increase performances of the LHC, the PS Booster shall increase the particles extraction energy from the present 1.4 GeV to 2 GeV. To accommodate this energy increase, a new main power converter with a peak power of 18 MW shall be installed.

The most important challenges in the realization of such a power converter are:

- 10 ppm accuracy in the control of the magnetic field (Bfield) or magnets current (Imag)
- Unity power factor operation (with respect to AC network) and power swing limited to ± 3MW

Figure 1 shows the current and voltage requirements for the power converter. The DC/DC shall control the output voltage so as to generate a nearly trapezoidal current pulse in the magnet with a peak value of 6 kA. Pulses are applied with a period of 1.2 s and continuously repeated around the clock 250 days per year.

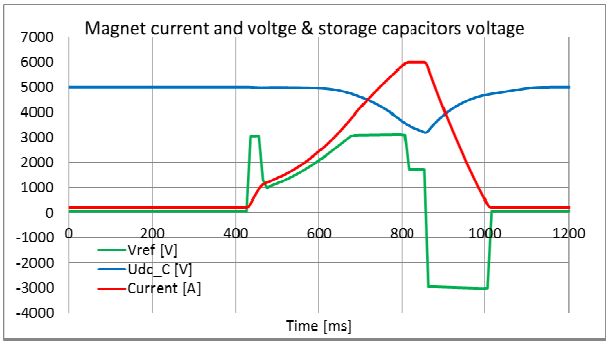

Figure 1: Current and voltage requirements

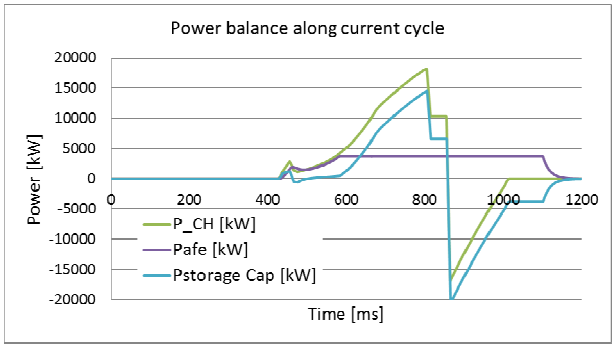

Figure 2: Power balance and load cycle

At every current pulse, the capacitor bank is discharged to 3.2 kV and charged back to its nominal value of 5 kV.

This way, although the magnets power swing goes as high as ±18 MW, the AC network sees only a nearly flat power pulse of 3 MW (Figure 2).

A major challenge of this load cycle is linked to the restriction of the IGBT minimum on-time, which is limiting the possibility to generate smooth low voltages in particular during the initial plateau of the cycle. A modification of the modulation is proposed to solve this issue.

A further requirement is a dynamical power limitation assuring that the network provides only the power for the losses of the system, for any operative condition and for any load cycle request.

The power layout of the MPC is shown in Figure 3.

The MPC consists of an AC/DC active front end (AFE), which supplies power to the DC/DC converter.

The capacitor bank is used to exchange the energy with the Booster magnets during converter pulsed operation. In this way the AFE provides only the losses required by the magnets and the converter itself [1].

The three levels NPC (3LNPC) structure [2] was chosen as the basic block for the realization of all power modules.

This structure is a de-facto standard for 3.3 kV motor drives industrial applications. The AFE is a three phase 3LNPC converter, whereas the DC/DC converter is an H-bridge, where each leg is represented by a parallel connection of three legs with 3LNPC structure. Each leg of the DCDC converter is switched at 333 Hz and is interleaved by 120 deg with respect to the others to increase the equivalent switching frequency of the H-bridge six fold to 2 kHz.

The paper describes the design of the control system of this power converter and presents results obtained using rapid control prototyping.

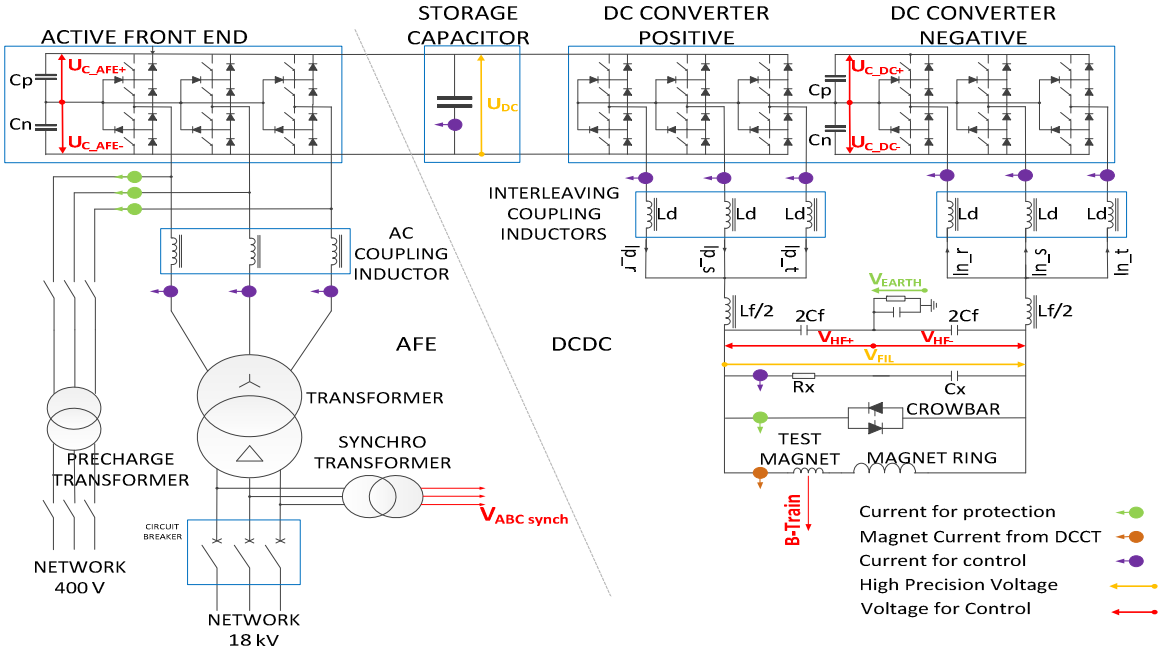

Figure 3: Power system layout

2. Control overview

The main task of the MPC control system is to track very accurately the reference signal (Bref or Iref) obtained from the CERN control center. The required accuracy is 10 ppm on either current or magnetic field.

The control is divided into two main parts:

- The AFE control (AC/DC)
- The DC/DC control

A. The AFE controller

The layout of the AFE controller is shown in Figure 4.

The AFE controller has three main functions:

- Controlling the Udc voltage;
- Controlling the AC input power factor;
- Limiting the peak power taken from the AC network.

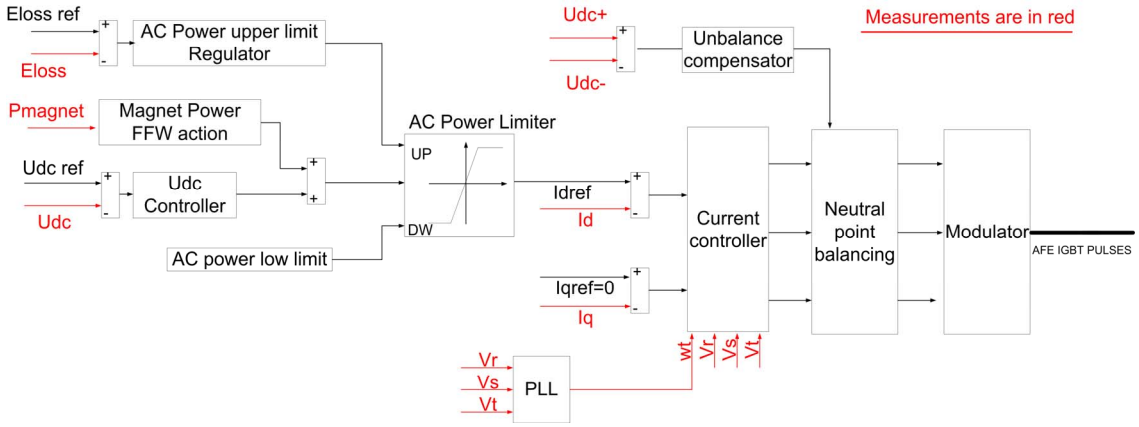

Figure 4: AFE controller layout

The three tasks are covered by the Udc voltage loop and by the current loops respectively. The outer Udc voltage loop provides the current references for the inner current loops. The saturation limits of the Udc controller are dynamically adjusted to perfectly match the rms losses of the system.

1) AFE model

AFE model for control design is developed using the system of equation (1).

$$V_x = rl_x + l\frac{dI_x}{dt} + V_{xAFE} \qquad \text{x} = \text{r, s, t.} \tag{1}$$

The decoupled system for the current loops in Park variables [3] is described by equation (2).

$$\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \frac{1}{r+sl}\left(\begin{bmatrix} V_d \\ V_q \end{bmatrix} - l\omega \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}\begin{bmatrix} I_d \\ I_q \end{bmatrix} - \begin{bmatrix} V_{dAFE} \\ V_{qAFE} \end{bmatrix}\right) \tag{2}$$

Where l is the inductance of the network and input transformer, r is its resistance and ω is the ac frequency.

The output of the voltage loop is the reference for the d axis (Idref), while the reference for the q axis (Iqref) is set to zero to obtain a unity power factor. The two current controllers generate the d and q voltage references (Figure 5). The control strategy is described in [4].

Finally, since the neutral point of an NPC converter is not stable, the balancing of the voltages U_{C_AFE+} and U_{C_AFE-} is achieved by an adjustment of the modulation indexes.

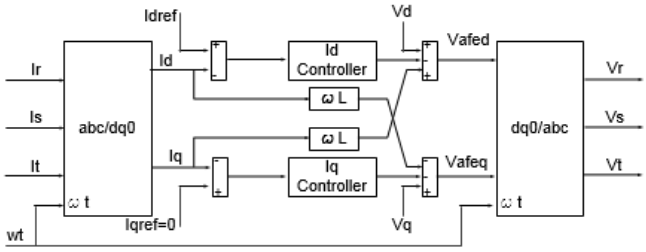

Figure 5: AFE current controller

2) AC network power control

The saturation of the Udc controller provides a limitation for the power taken from the AC network. Nevertheless, depending upon the current peak it may happen that the limitation is too high. This leads to overcharging the capacitor bank when the magnet is discharging at the end of the load cycle. The controller will act to keep the voltage constant, thus discharging the capacitor by returning power to the network producing a negative power spike. This issue is to see in Figure 16 in B. To avoid the inconvenience of back-feeding active power to the network, a dynamic power limitation is proposed as shown in Figure 6. The power absorption from the network is measured and integrated, and then reset at the beginning of each

cycle. The energy lost in one cycle is estimated and used as a reference. When the integrated power absorption reaches the reference, the upper limit of the voltage regulator is reduced to a very small value to limit further charging.

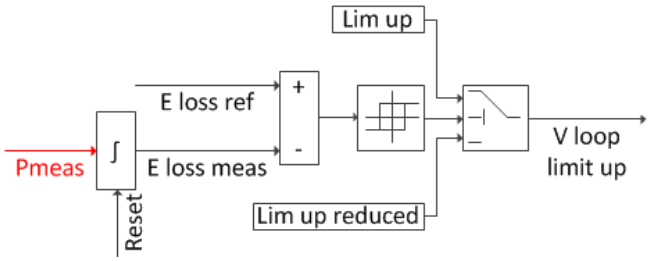

Figure 6: Dynamic power limitation

B. The DC/DC controller

The layout of the DC/DC controller is shown in Figure 7.

The controller has the following functions:

- Controlling the magnetic field (Bfield) or the magnet current (Imag)
- Controlling the magnet voltage (Vmag)
- Controlling the voltage balance U_{C_DC+}, U_{C_DC-}
- Controlling the current balance in the six output legs.

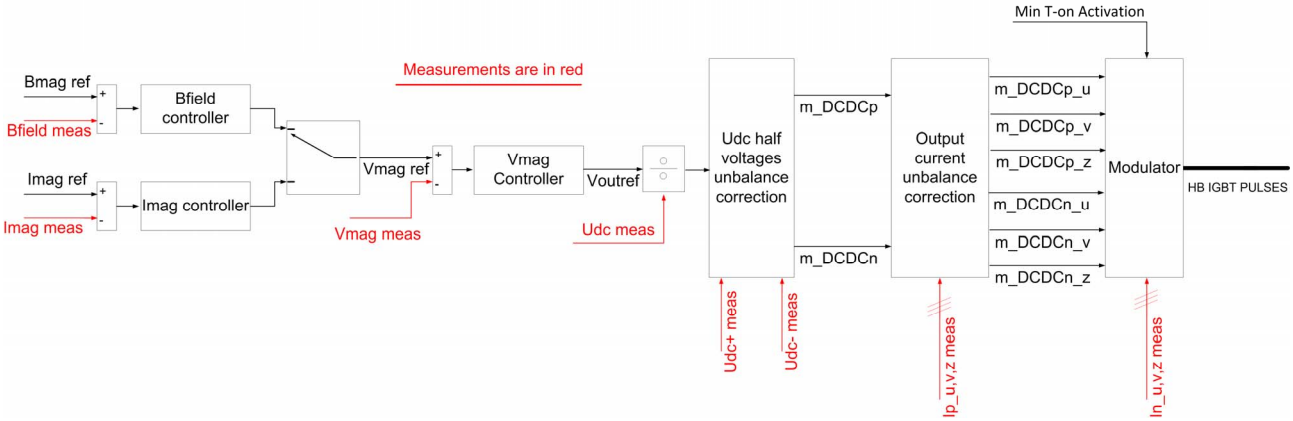

Figure 7: DC/DC controller layout

The outer loop can be either a magnetic field (Bfield) or a magnet current (Imag) controller. For the sake of control development we shall consider an Imag controller. Figure 1 shows the typical current pulse reference. The inner loop controls the magnet voltage (Vmag), while further adjustments of the modulation indexes control the semi-voltage balance according to [5], the current balance in the six legs according to [6], and the minimum IGBT on-time restriction.

1) Imag & Vmag controllers

Given the strong accuracy requirements RST controllers are used. The output of the current controller is the reference for the inner voltage loop. The controller's parameters of the current loop are calculated based on the transfer function (3) between the output of the regulator and Imag considering the delay of the inner voltage loop (T_{delay}), whereas the ones for the Udc voltage loop are calculated on the output filter transfer function (4) [7].

$$H_{sys} = \frac{I_{mag}}{V_{mag}} = \frac{1}{sL_{mag} + R_{mag}} e^{-s*T_{delay}} \tag{3}$$

$$H_{filter} = \frac{1 + R_x C_x s}{(\frac{2}{3} L_d R_x C_x C_f + L_f R_x C_x C_f)s^3 + (\frac{2}{3} L_d C_x + \frac{2}{3} L_d C_f + L_f C_x + L_f C_f)s^2 + R_x C_x s + 1} \tag{4}$$

2) Interleaving

The three legs of each module have an interleaving of 120°. This is achieved by shifting the three carriers in the modulator. The carriers have a period of 3 ms (333Hz). The index is updated at every peak of the carrier, thus every 1.5 ms. Since the carriers are shifted the voltage loop needs to have a sample time of 500µs. The idea is shown in Figure 8.

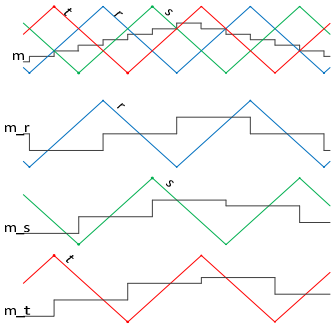

Figure 8: Interleaving and updating of the modulation indexes

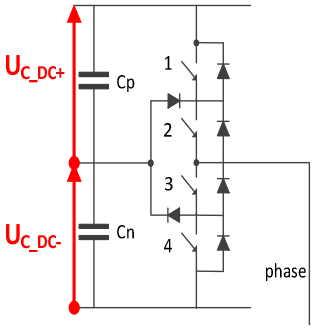

Figure 9: Single converter leg layout

The interleaving between positive and negative module is obtained by using complementary modulation indexes for the two modules as for unipolar modulation allowing an interleaving of 180°.

3) Minimum IGBT on-time restriction

One of the most challenging aspects to consider for achieving the accuracy requirement is the IGBT minimum on-time.

This restriction is seriously limiting the possibility to generate smooth low voltages.

This aspect is particularly important during injection of particles in the PSB at the very beginning of the cycle, where output voltage may be in the order of 100V.

The authors propose a modification of the standard switching pattern to eliminate minimum on-time effects from the output voltage.

For what the single IGBTs is concerned, referring to Figure 9 switch 3 is complementary to switch 1 and so are switches 4 and 2. Since only one carrier per leg is used, the modulation index of switch 2 is offset by +1.

In case of a low voltage demand, the IGBTs would need to stay in the on state for less than their minimum on-time. An offset α given to the modulation indexes of switches 1 and 2 allows having low voltages applied without violating the IGBTs' minimum on-time, see equations (5) and (6).

$$for\ m_{xx} \geq 0 \qquad \begin{cases} m_{xx1} = m_{xx} + \alpha \\ m_{xx2} = 1 - \alpha \end{cases} \tag{5}$$

$$for\ m_{xx} < 0 \qquad \begin{cases} m_{xx1} = \alpha \\ m_{xx2} = m_{xx} + 1 - \alpha \end{cases} \tag{6}$$

Figure 10 shows the case of $m_{xx} > 0$.

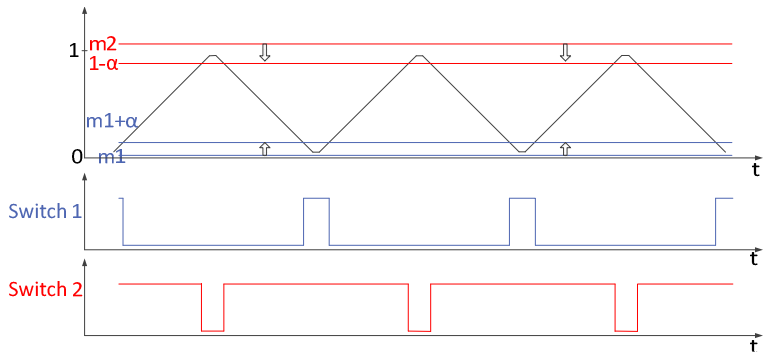

Figure 10: IGBTs' minimum on-time mode

In fact the low output voltage is supplied by the combined action of the two switches. The minimum on-time mode is activated only when the modulation index is lower than a threshold. To avoid a continuous enable-disable of the mode when working across the threshold, a hysteresis band is used.

3. The real-time simulation platform

Rapid control prototyping method is used to test the above described control system. For this purpose a real-time simulation platform is interfaced with a scaled model. The scale is 1/100 for both current and voltage, and therefore the values of resistances, inductances and capacitances are the same as those of the real converter. Based on Figure 1, the peak current is scaled from 6 kA to 60 A and the DC voltage from 5 kV to 50 V. The control is running on the simulation platform. A set of electronics cards has been developed to interface analogue and digital inputs/outputs between the simulation platform and the power model which has the same structure as the one showed in Figure 3. The realization of the Prototype as well as the simulation platform are shown in Figure 11.

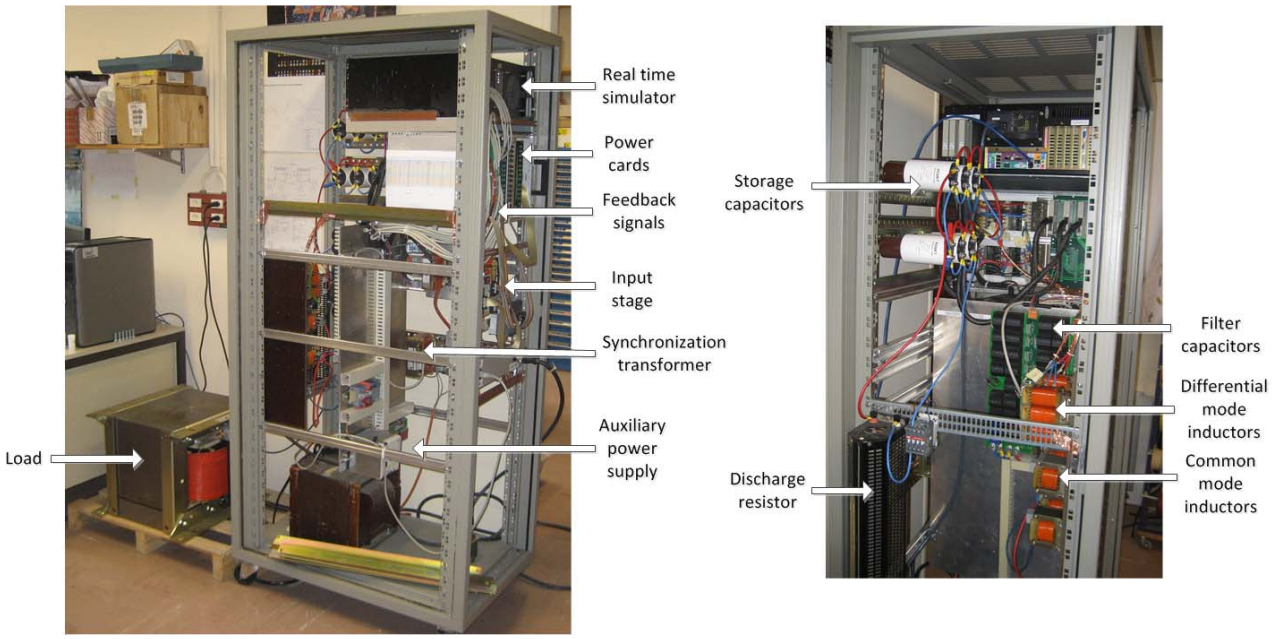

Figure 11: Power converter scaled prototype – side view (left) and back view (right)

4. Results

A. Normal cycle response

The response to a cycle with 50 A peak current is shown in Figure 12. Measurements were saved in the real time platform and plotted in Matlab. The measured current (red) follows very well its reference (black). The DC voltage (blue) gets discharged from the nominal 50 V to almost 30 V and it is completely recharged by the end of the cycle. The voltage applied to the magnet (green) presents a 50 Hz ripple which is a noise coming from the current measurement probe. However, this ripple does not have much importance for our study.

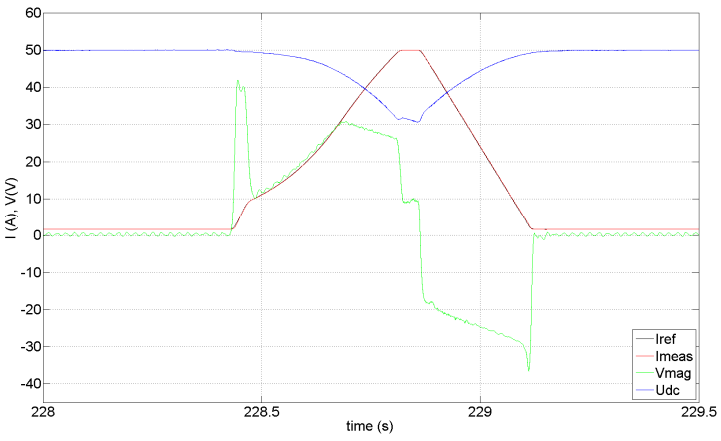

Figure 12: Acquisition over one cycle

B. Minimum IGBT on time

At low voltage requirements, a low frequency oscillation is created in the output voltage and current due to the minimum IGBT on-time, see Figure 13. This ripple is obvious in the voltage and its amplitude depends on the tuning of the controller. A remarkable reduction of the ripple is achieved when the minimum on-time mode is enabled, see Figure 14.

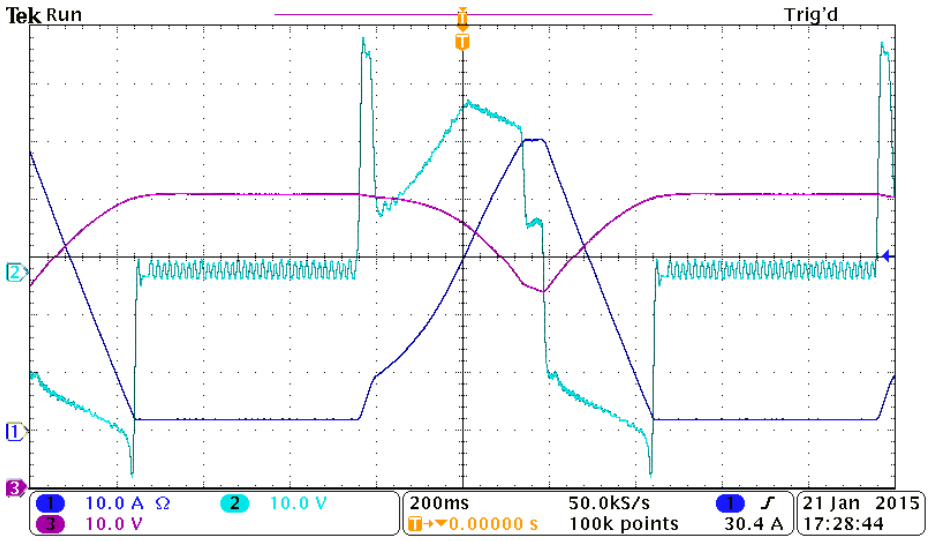

Figure 13: Cycle without minimum on-time mode

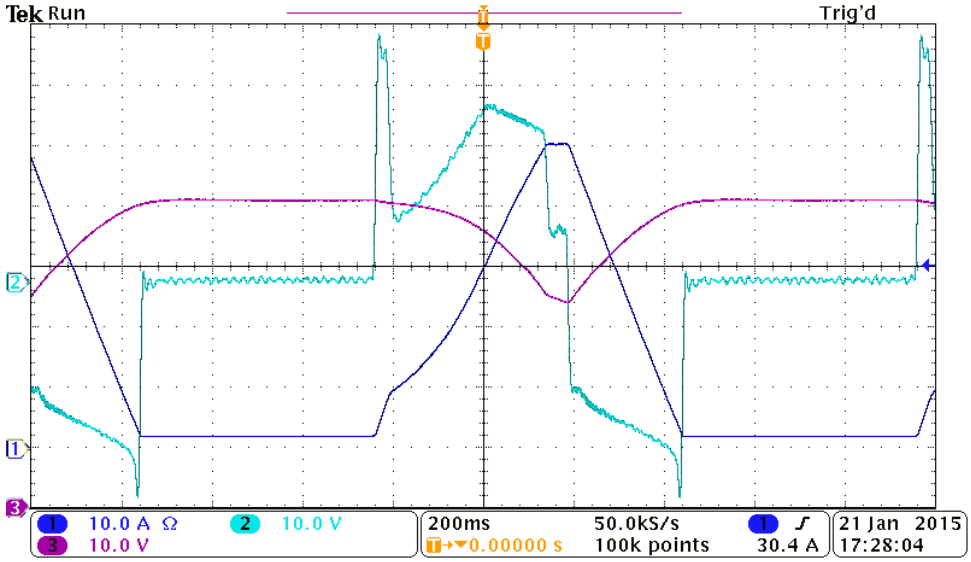

Figure 14: Cycle with minimum on-time mode

C. AFE

In this section the main features of the AFE are presented. The power absorption over one cycle is shown in Figure 15. The voltage (light blue) and the current (blue) are measured on the secondary of the input transformer, while the violet curve shows the DC-link voltage. The acquisition shows how the current evolves during the discharge and recharge of the storage capacitors. A zoom shows that the current is in phase with the voltage, thus unity power factor is achieved.

Results of the dynamic power absorption limitation are shown in Figure 16 and Figure 17. They both show acquisitions from the scaled power converter, in which a sequence of current cycles with increasing flat tops is applied. The first subplot shows the magnet current (blue) and the DC link voltage (red). The second subplot shows the power in the magnet (blue) and the power taken from the grid (red). In Figure 16 the dynamic power limitation is disabled and one can see that for smaller magnitude current cycles there is a

slight overvoltage by the end of the cycle and the power absorption gets negative, active power is fed back to the network. Figure 17 shows that the strategy explained in 2.A.2) solves the problem, since the negative power spike disappears.

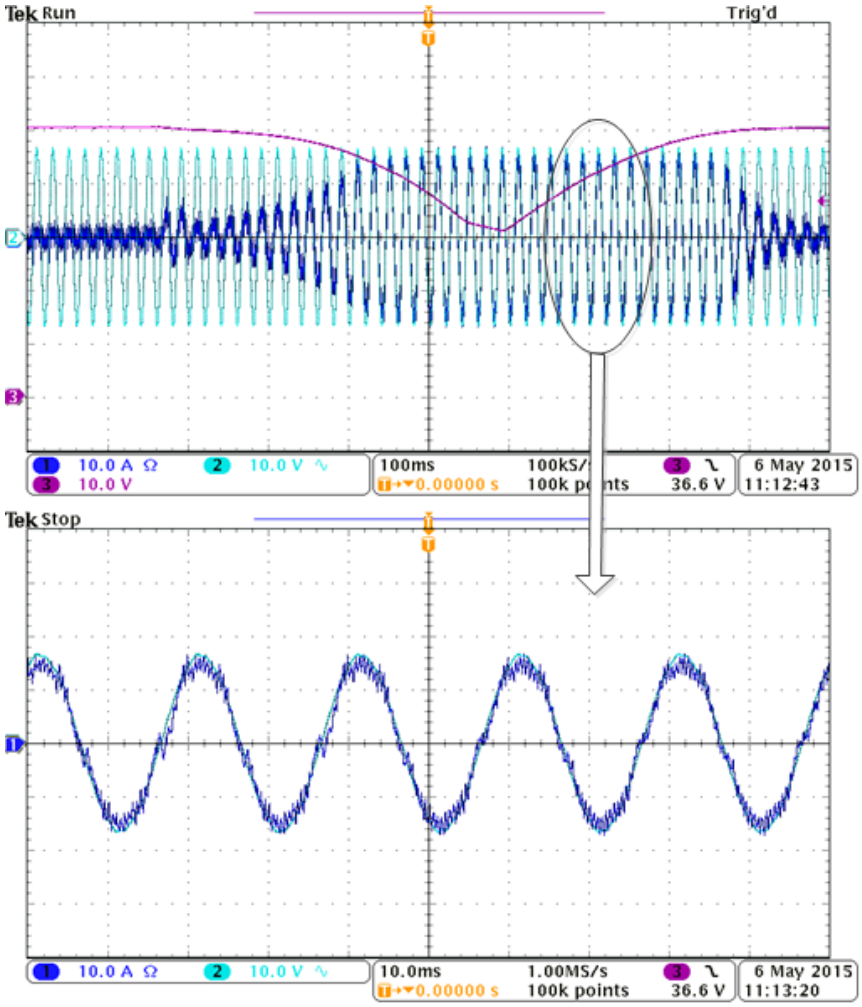

Figure 15: AFE, phase voltage and phase current

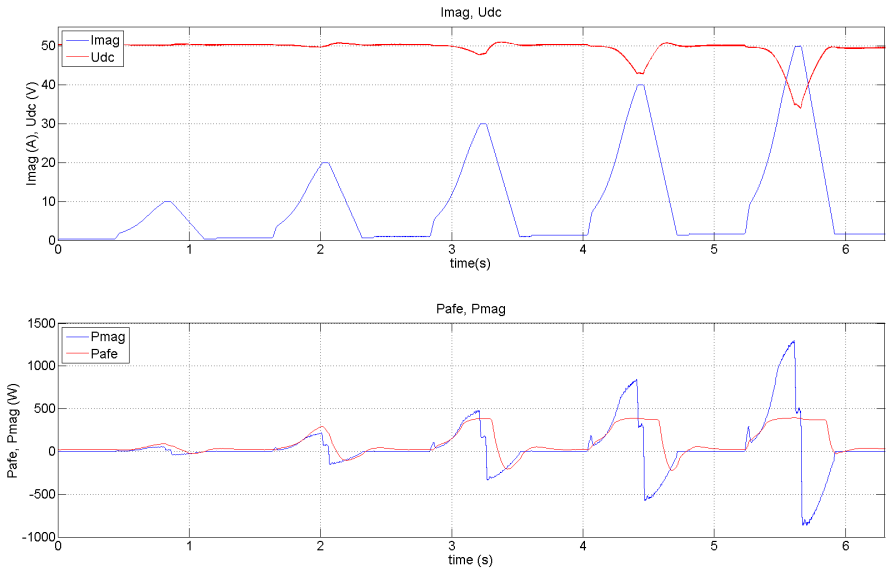

Figure 16: Power absorption without dynamic limitation

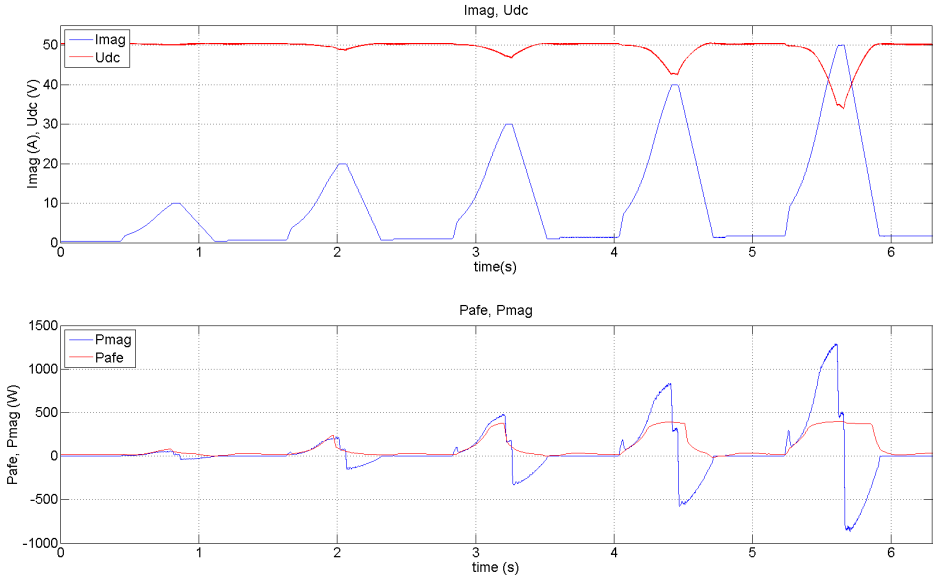

Figure 17: Power absorption with dynamic limitation

5. Conclusions

Due to the specifications of the converter and its particularities, the design of the control system becomes critical.

Rapid control prototyping is a powerful tool for design studies of the control system and tuning of the parameters. It is a practical and relatively fast way of testing and validating control strategies on real hardware.

In particular, it allows users to put innovative ideas into practice and to validate them. The compensation of the minimum IGBT on-time is a major challenge for the operation of the PS Booster at low magnet output voltage. Rapid control prototyping was successfully used to overcome the minimum on-time limitation and generate a stable low voltage during injection plateau. Similarly, it has confirmed our control strategy to dynamically limit the network power absorption to perfectly match the losses of the system.

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