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CLIC vertex detector R&D

Niloufar Alipour Tehrani*†

On behalf of the CLICdp collaboration

* *CERN, Switzerland,* † *ETH Zürich, Switzerland*

Abstract

A vertex-detector concept is under development for the proposed multi-TeV linear e^+e^- Compact Linear Collider (CLIC). To perform precision physics measurements in a challenging environment, the CLIC vertex detector pushes the technological requirements to the limits. This paper reviews the requirements for the CLIC vertex detector and gives an overview of recent R&D achievements in the domains of sensor, readout, powering and cooling.

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N. Alipour Tehrani[a,b]

[a]CERN, Geneva, Switzerland
[b]ETH Zürich, Zürich, Switzerland

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A vertex detector concept is under development for the proposed multi-TeV linear e^+e^- Compact Linear Collider (CLIC). To perform precision physics measurements in a challenging environment, the CLIC vertex detector pushes the technological requirements to the limits. This paper reviews the requirements for the CLIC vertex detector and gives an overview of recent R&D achievements in the domains of sensor, readout, powering and cooling.

Keywords: CLIC, Silicon pixel vertex detector, Solid state detectors

1. Introduction

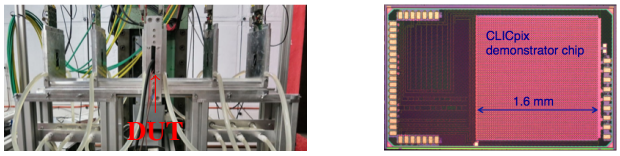
The Compact Linear Collider (CLIC) [1] concept for a future linear e^+e^- collider has the potential to complement the measurements done by the LHC experiments. With proposed centre-of-mass energies of 350 GeV, 1.4 TeV and 3 TeV and with instantaneous luminosity up to $6 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, it allows for high precision measurements of Standard Model physics and of new physics potentially discovered at the 14 TeV LHC. The precision physics requirements and experimental conditions set challenging demands for the vertex detector in terms of spatial resolution, material budget, timing resolution and efficient heat removal from sensors and readout. The CLIC vertex detector R&D programme studies different sensor technologies and focuses on integration of constraints from mechanics, power delivery and cooling.

2. Vertex detector requirements

The aim of the CLIC vertex detector is the efficient identification of heavy quarks through a precise determination of their displaced vertices in an environment with high occupancy from beam-induced backgrounds. Multi-layer barrel and endcap pixel detectors with geometrical coverage extending down to low polar angles ($\theta_{min} \approx 8°$) are foreseen to fulfill these requirements. The goal is to achieve a single-point resolution of ~3 µm with 25 µm pixel pitch and analog readout. Time slicing of ~10 ns reduces the impact of beam-induced backgrounds from physics events. A material budget of $\sim 0.2\% X_0$ per layer is required including readout, support and cabling. This can be achieved with 50 µm thick sensors on 50 µm thick ASICs and forced air-flow cooling (c.f. Section 5). Power-pulsing limits the power dissipation to 50 mW cm^{-2} (c.f. Section 4).

3. R&D on sensor and readout

R&D activities on hybrid pixel technology with low-mass interconnects is ongoing. Hardware assemblies with planar silicon and active HV-CMOS [2] sensors have been tested in the lab and during test-beam campaigns at DESY and CERN using the EUDET/AIDA telescope [3] containing 6 planes of Mimosa26 pixel sensors. Figure 1a shows a picture of the test-beam setup at DESY.



(a) (b)

Figure 1: a) EUDET/AIDA telescope used during test-beam campaigns for testing planar sensors and HV-CMOS devices. b) CLICpix chip demonstrator.

3.1. Thin sensor

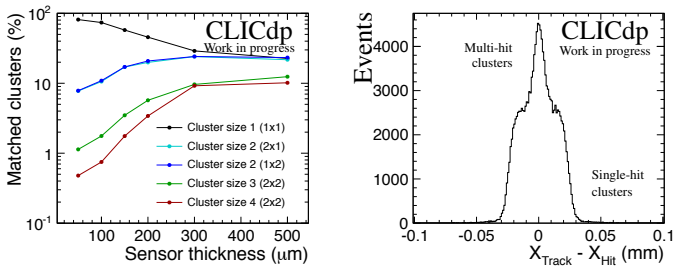
The feasibility of thin planar sensors is studied using the Timepix readout ASIC with 55 µm pixel pitch. 50 µm to 500 µm thick planar sensors are bump-bonded to 100 µm and 700 µm thick Timepix ASICs. Figure 2a shows the fraction of single and multi-hit clusters as a function of sensor thickness. A thicker sensor results in more charge sharing. The resolution of multi-hit clusters is better than that of single-hit clusters. The hit residuals for a 100 µm sensor are shown in Figure 2b. In this plot, the two structures highlight the resolution of single-hit clusters which is determined only by the pixel size, and multi-hit clusters have a smaller resolution due to information from the relative charge in each pixel.

3.2. Active HV-CMOS sensor

Active HV-CMOS sensor devices are also studied during test-beams. A capacitively coupled pixel detector (CCPDv3)

☆On behalf of the CLIC detector and physics collaboration (CLICdp)

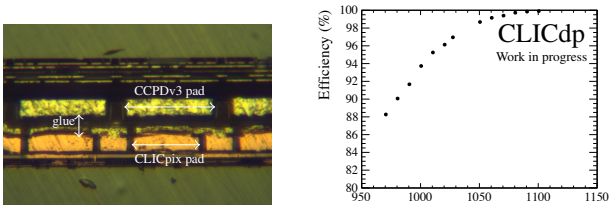
Email address: niloufar.alipour.tehrani@cern.ch (N. Alipour Tehrani)



(a) (b)

Figure 2: a) cluster-size distribution for planar sensors with different thicknesses bump-bonded to the Timepix ASICs. b) Hit residuals for a 100 μm thick sensor.

implemented in a 180 nm HV-CMOS process is used as active sensor which integrates sensor and amplifier. The CLICpix readout ASIC demonstrator [4], as shown in Figure 1b, is used to test the CCPDv3 device. With a matrix of 64×64 pixels and 25 μm pixel pitch, CLICpix is implemented in 65 nm CMOS technology. The CCPDv3 chip is capacitively coupled from its amplifier output to the CLICpix readout ASIC through a thin layer of glue. Figure 3a shows a cross-section of the device and the glue between the sensor and the CLICpix. The CCPDv3 is biased at −60 V and creates a depletion layer with fast signal collection through drift. The tested assemblies show a high single-hit detection efficiency for different thresholds, as shown in Figure 3b. For the nominal operation threshold setting of 1100 (corresponding to 1200 electrons), the efficiency is greater than 99.9%.



(a) (b)

Figure 3: a) Cross-section of a CCPDv3-CLICpix assembly taken with an optical microscope. b) Hit-detection efficiency as a function of the threshold DAC applied to CLICpix.

4. Power delivery and power pulsing

A low-mass power-delivery and power-pulsing system is developed for the vertex detector [5] and illustrated in Figure 4. The analog front-end of the readout ASICs is turned off during the 20 ms gaps between bunch trains to reduce the average power consumption. The energy needed for the readout of the ASICs is stored locally in silicon capacitors and the voltage for the analog and the digital part of the ASICs is stabilised with low-dropout (LDO) regulators. A small continuous current is provided by an FPGA-controlled current source into the vertex region through low-mass kapton cables. Figure 5a shows the tests done on a prototype with dummy loads emulating the power consumption of a half-ladder. A low current (≤300 mA) and low average power consumption (<45 mW cm^{-2}) have been measured.

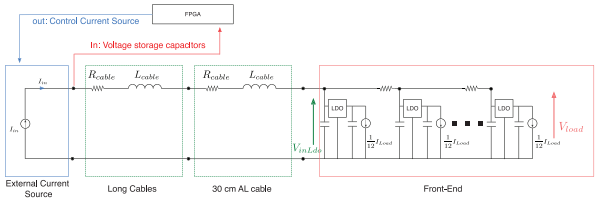
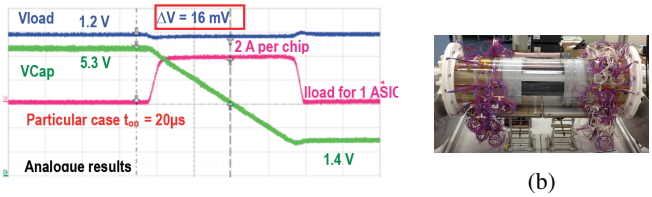


Figure 4: Diagram of the power delivery for a half-ladder.



(a) (b)

Figure 5: a) Measured output current and voltage at the last ASIC for the analog electronics after power pulsing. b) Thermal mockup of the vertex detector for tests on air-flow cooling.

5. Air-flow cooling

With the power-pulsing system, the total power consumption of the vertex detector is estimated to ∼500 W. Forced air-flow cooling is foreseen for the heat removal of the vertex detector to fulfill the material budget requirements [6]. Simulations as well as measurements with thermal mockup (Figure 5b) confirm the feasibility of this technique. The temperature increases between 10 °C to 35 °C.

6. Conclusion

The precision physics requirements at CLIC set challenging demands on the performance of the vertex detector. Hardware R&D programs study the feasability of new technologies for sensor, readout, power-pulsing and cooling.

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