CBC2: A CMS microstrip readout ASIC with logic for track-trigger modules at HL-LHC

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ABSTRACT

The CBC2 is the latest version of the CMS Binary Chip ASIC for readout of the upgraded CMS Tracker at the High Luminosity LHC. It is designed in 130 nm CMOS with 254 input channels and will be bump-bonded to a substrate to which sensors will be wire-bonded. The CBC2 is designed to instrument double layer modules, consisting of two overlaid silicon microstrip sensors with aligned microstrips, in the outer tracker. It incorporates logic to identify L1 trigger primitives in the form of "stubs": high transverse-momentum track candidates which are identified within the low momentum background by selecting correlated hits between two closely separated microstrip sensors. The first prototype modules have been assembled. The performance of the chip in recent laboratory tests is briefly reported and the status of module construction described.

1. Introduction

A major upgrade of the CMS experiment at the CERN Large Hadron Collider has now been under consideration for several years [1,2]. The objective is that the accelerator should deliver an integrated luminosity of 3000 fb^{-1} over a period of about a decade of operation for a physics programme which will include precision measurements of the newly discovered Higgs boson, further searches for new physics extended to higher masses, and deeper scrutiny of data for possible discrepancies compared to the Standard Model.

The High Luminosity LHC will require a new Tracker around 2023 because of gradual deterioration of the present detector due to accumulated radiation damage. Its replacement must satisfy several demanding requirements, including a lower material budget and increased granularity compared to the present detector, and enhanced radiation tolerance combined with tolerable power consumption and affordable cost.

Over the last few years, the goals for the new detector have evolved and some specifications are still under discussion. It was envisaged that the new tracker would have a similar angular coverage to the present system, but the design would be constrained by re-using existing services for cooling, power and optical data transmission. It was also foreseen that tracker data would be provided to the L1 trigger for the first time to contain the trigger rate to 100 kHz within a latency of 6.4 μs. Recently, CMS has converged on a baseline Tracker design using a "conventional" barrel-endcap layout but increasing the angular coverage to enhance forward region physics studies is under consideration. The question of replacing services has been reopened, which may reduce some constraints if this major task can be carried out. While using the data from the tracker in the L1 trigger is a requirement, simulation studies are not far enough advanced to be certain that the rate can be reduced sufficiently and a possible objective of L1 readout with up to 1 MHz and a latency of 10–20 μs is under study. However, in all cases on-detector data reduction is required since power and bandwidth constraints prevent transmission of all hit data to the trigger and the modules deployed will have significant differences in design from the present ones.

The earliest developments foresaw conventional outer tracker modules, plus dedicated trigger (and pixel) tracking layers. A 128-channel CMS Binary Chip (CBC) was manufactured and demonstrated in 2011 [3] to provide readout for the silicon microstrip sensors. The readout architecture followed that adopted for the original tracker using the APV25 ASIC [4,5], which did not employ zero-suppression but transmitted analogue data synchronously to the off-detector data acquisition system where the first level of data reduction was carried out. However, the CBC did not aim to provide analogue data for practical reasons; analogue optical link components are not commercially standard, and were adapted

from digital components when the present tracker was designed, and on-detector analogue to digital conversion is costly in terms of power, space and bandwidth. In addition 130 nm CMOS makes analogue memory cells harder to implement compared to the 0.25 μm technology used for the APV25. Many of the arguments justifying analogue readout were based on robustness of the system to unexpected noise, which is now much better understood by CMS, and the improved spatial precision gained by analogue information is not large in view of the multiple scattering incurred as particles traverse the detector. The CMS Tracker performance has been reported [6,7] and a more comprehensive publication is almost ready.

In view of progress with the CBC, outer tracker modules with the capability to deliver data to the trigger were proposed and a new version of the readout ASIC, the CBC2, has been designed and was delivered in early 2013. It has been optimised for a new assembly method with mass production in mind and the first prototype modules have been assembled and are under test. The chip will provide data to the L1 trigger, and will store all hit data until the L1 trigger decision has been made, when the stored data will be transmitted to the data acquisition system for full event reconstruction.

2. CBC2 design

The basic concept underlying the data selection for the trigger is to compare the binary pattern of hit strips on upper and lower sensors of a two-layer module (Fig. 1) and reject patterns that are consistent with a low transverse momentum track [8,9]. In the "2S"-module (Fig. 2) two silicon microstrip sensors are separated
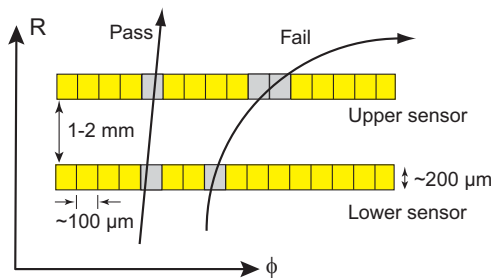

Fig. 1. The PT-module requires two sensor layers in a single module. High p_T tracks can be identified if hits lie within a narrow search window in the upper sensor. The figure illustrates the conceptual arrangement for the central barrel region of the tracker.

by a few mm, with the separation determined by the compromise between transverse momentum precision and the fake stub rate result from effects like secondary interactions and background hits from, e.g., photon conversions.

In the cylindrical barrel region, high p_T tracks can be identified if hits lie within a search window in $R–\phi$ (rows) in the second layer. The sensor separation and search window determine the p_T cut, although it should be noted that the objective is not a measurement of p_T as such but rejection of the large fraction of low p_T candidates in the detector so that trigger primitives can be transmitted within the available bandwidth. In the barrel region, the sensor segmentation in z (along the beam axis) determines the vertex measurement precision; for the outer tracker region with 5 cm strips this is not high and some dedicated layers with finer segmentation are planned. Similar considerations apply to the end-cap detectors where the same method can be deployed.

The CBC2 has evolved from the CBC design [10], both of which were fabricated in a 130 nm CMOS process. The same amplifier, with minor improvements, was used in both chips; it was designed for microstrips of up to 5 cm length, and with a load capacitance of up to about 10 pF. The CBC has 128 channels on a 50 μm pitch and with a layout intended for wire-bonding to the silicon sensor. The amplifier accepts both polarity input signals and can be either AC or DC coupled to the sensor.

Other features of the CBC design have been carried over to the CBC2. A comparator follows the amplifier stages and the comparator outputs are sampled into a pipeline memory at 40 MHz. The depth of the pipeline is programmable up to 256 allowing a level 1 trigger latency of up to 6.4 μs. If a trigger occurs, the data from the triggered time-slice (the 254 bits of data that were stored in the pipeline a latency period before) are retrieved and stored in a readout buffer which can accommodate up to 32 triggered data sets awaiting readout. If the buffer was previously empty then the serial data output begins promptly at 40 Mbps.

Critical digital blocks have been designed for SEU resistance. 40 MHz clock signals are transmitted using the Scalable Low Voltage Signaling (SLVS) standard [11]. An on-chip bias generator provides currents and voltages required by the analogue stages, programmed via an I2C slow control interface, which is also used to set up all other programmable features of the chip.

Power provision is a major concern for future trackers with existing cable cross sections imposing limits on deliverable currents. CMS has adopted a DC-DC powering scheme for the outer tracker, where higher voltages are locally translated to lower levels required by on-detector electronics. The CBC incorporates a switched capacitor DC-DC circuit
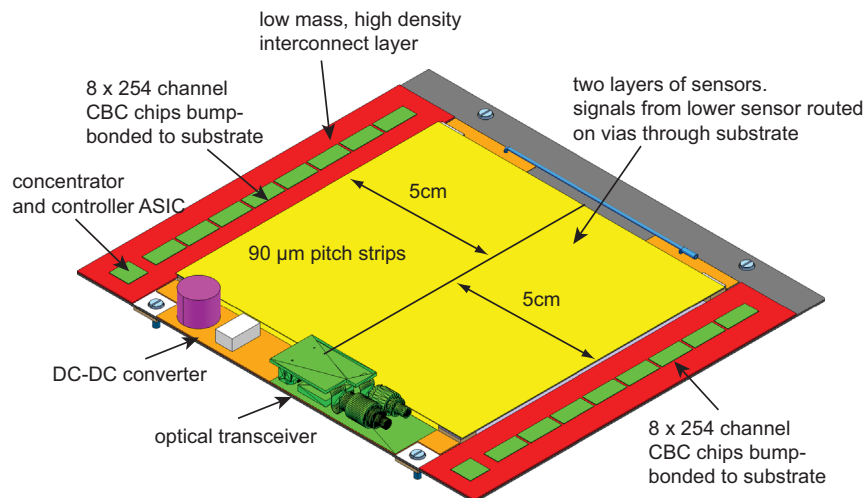

Fig. 2. A conceptual diagram of the 2S-module being developed. The sensors are wire-bonded to the substrate on the top and bottom surfaces.

designed in CERN which converts a 2.5 V supply to the lower voltage needed by the core circuitry; at present this is being evaluated for the final system. A low dropout linear regulator is also included which provides clean power to the analogue front end.

For a 5 pF load, the CBC consumes less than 300 μW/channel, including both analogue and digital stages, for ENC ≈ 850 electrons, in good agreement with simulations. More details of the CBC design and performance have been reported elsewhere [12]. The CBC has also been deployed in modules used in a telescope in a test beam with good performance [13].

It is expected that commercial assembly will be utilised in construction of the new tracker and the CBC2 has been designed with this objective in mind. The chip has been laid out with bond pads on 250 μm pitch to be bump-bonded to a substrate using a commercial technology. This has several practical advantages [14], including reduced bond inductance and simplified power and

signal connection, but requires development in collaboration with industry of the required hybrid circuits which is underway.

The CBC2 is approximately 5 mm × 11 mm in area. It contains 254 channels, so that two sensors each containing 127 strips could be connected and the correlation logic to find the track high p_T "stubs" could be implemented. The chip was sent for fabrication in September 2012 in a multi-project wafer submission, sharing the wafer surface with another large chip and one smaller one; 112 reticles were assembled on each wafer.

3. Stub-finding logic

The first stage of the stub-finding logic (Fig. 3) rejects wide clusters of hits, which are typically associated with low-momentum tracks, in both sensor layers, then for each cluster in the inner sensor
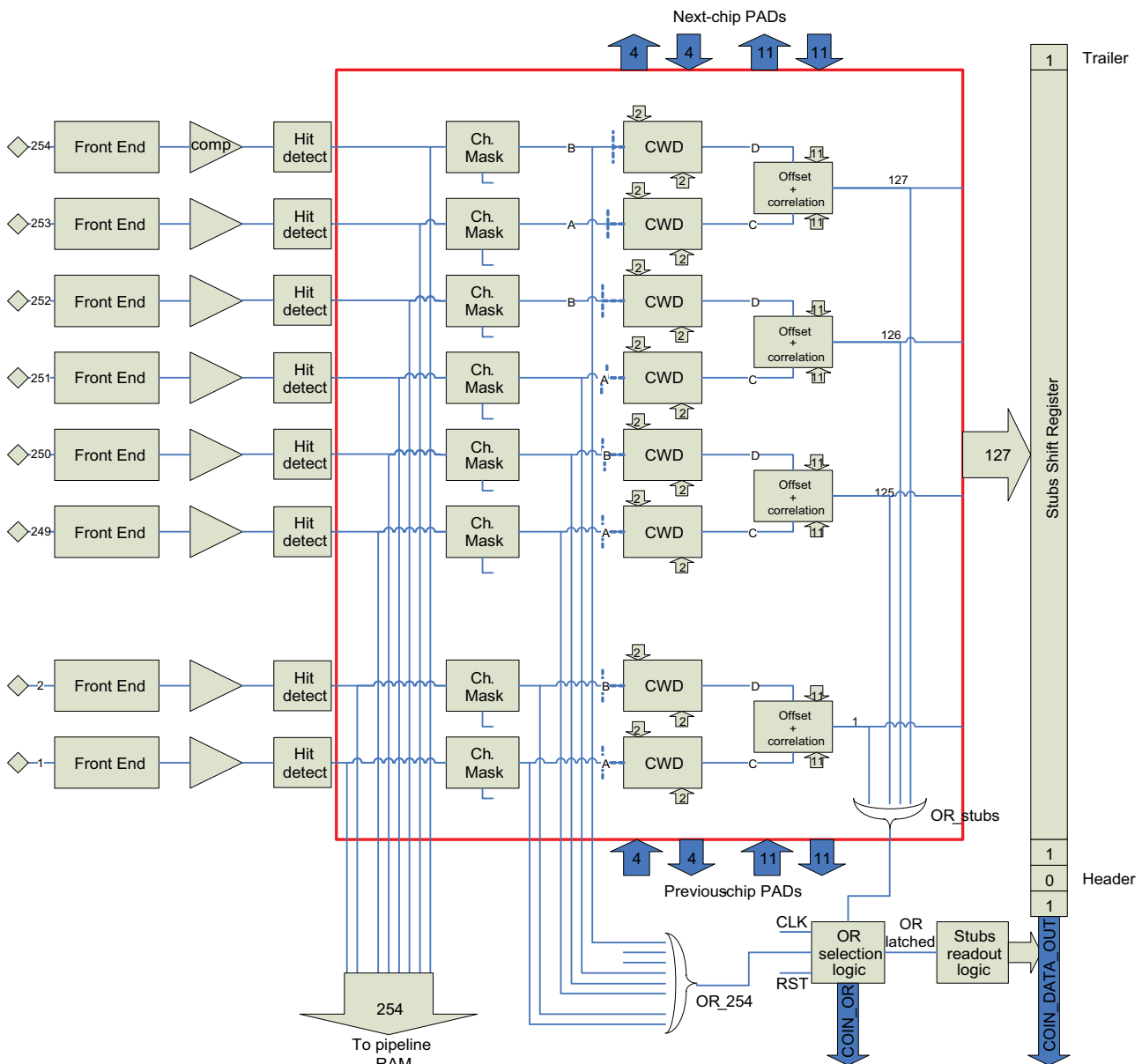

Fig. 3. The principal components of the correlation logic used to identify track stubs.

a search is made for a hit in a coincidence window in the outer sensor. A global 2-bit register defines the maximum cluster size to be 1, 2 or 3 adjacent strips; wider clusters are suppressed. The same register allows the cluster-width discrimination (CWD) to be disabled to pass every hit to the subsequent stage. At the CWD output only the central strip of a cluster is active; for a two-strip cluster, the centre is assigned to the strip with lower address. This allows more stubs in the available bandwidth.

For every central strip of an inner layer cluster, the logic block following the CWD looks for valid clusters in a programmable window in the outer layer. If a hit is found in this window, the inner strip is considered a valid stub. Noisy channels can be individually masked from the coincidence logic without affecting the values written into the pipeline RAM.

The size of the window in the outer layer defines the p_T cut. For example, in the barrel region, for a given p_T, the lateral displacement between hits in the two sensor layers depends on the radial separation of the two layers, the electric charge of the particle and the radius of the module in the tracker. In order to obtain a uniform p_T cut throughout the tracker volume the width of the coincidence window is programmable in the range ± 8 strips around the central strip. The position of the coincidence window must also be adjusted to account for geometrical lateral displacement which depends on the distance from the centre of the module; this offset is programmable in the range ± 3 strips.

The readout is controlled by the OR of all the correlation outputs, which is also transmitted off-chip as "signal ready". As a test feature the OR of *all* the channel outputs can also be selected to control the stub readout. A future version of the CBC will send stub addresses to fast parallel outputs for low-latency transmission to the L1 trigger.

Both the cluster-width discrimination and the offset correction and correlation logic rely on inputs from up to 15 neighbouring channels on each side, allowing for cluster size, offset correction and the coincidence window. To permit the logic to handle chip boundaries, on both top and bottom edges of the CBC2 15 input pads and 15 output pads are assigned for inter-chip links. However modules are designed as independent units and there is no data transmission between adjacent modules. Overlap of modules in both η and ϕ will ensure that high-p_T tracks straddling adjacent modules are not lost. Acceptance loss of stubs straddling two halves of the same module in η should be a small effect for sensor separations in the range envisaged taking into account signal charge sharing.

4. Evaluation

Testing began in February 2013, following wafer dicing and assembly of chips onto substrates. Since much of the design is almost identical to the CBC, the first stage of testing mainly involved verifying that the CBC2 behaved similarly, which was the case. New features included provision of test pulses to the input which, together with individually-programmable channel masks, can be used to fully exercise the coincidence logic. Other optimisations of the design, in particular the power conversion, also appear to have been successful although not yet studied in complete detail.

Following manual wafer probing of one wafer, 112 CBC2 chips were tested, resulting in 108 good chips with the 4 bad chips attributed to physical damage from the difficult positioning of the probe card. A second wafer has recently been probed with equally high yield. No defective channels were found on any operational CBC2s.

The main focus of recent testing has been to validate the digital logic changes, in particular, the stub-finding features. Initially this was done with test pulses and a single CBC2 chip. Recently the first small-scale prototype 2S-module has been constructed with a commercially manufactured and assembled hybrid on which just two CBC2 chips were mounted. The hybrid was designed to allow testing of inter-chip communication as well as assembly and wire-bonding to two 5 cm long, 80 μm pitch strip sensors with a few mm separation [14]. As the sensor signal line and bump-bond pad densities require a very fine line width and spacing on the printed circuit board, state-of-the-art manufacturing capabilities were required. It was produced using special substrate materials and precision laser drilled micro-vias. Flip-chip soldering of the CBC2 chips to the hybrid was also successfully tested for the first time so the assembly was an important first step in addressing some key technological challenges for the full size 2S-module hybrid.

Tests have been carried out in the lab using cosmic rays and β electrons from a Sr^{90} source [15] demonstrating full functionality (Fig. 4). The prototype 2S-module was positioned above a scintillator which was used to trigger readout of the CBC2 data which had been stored continuously in the pipeline memory at 40 Mbps. The figure shows one example of an event triggered by a β which has emulated a high-p_T stub. The level in the trigger logic output stream demonstrates that the internal logic has detected a pattern corresponding to a valid stub, following a signal in the scintillator.

The CBC2 output frame comprises a series of header bits, followed by a stream of binary data corresponding to strip hits detected in the module. Since the upper and layer strips are interleaved at the input of the CBC2, a data sequence could be represented as $[...S_{n-1}\ T_{n-1}\ S_n\ T_n\ S_{n+1}\ T_{n+1}...]$ for example, where S and T signify the two sensor layers. If the sensors are well aligned, simple patterns can be identified which represent hits matching the criteria for high-p_T stubs. A sequence like 0110 corresponds to a pair of hits, one in each layer, in close transverse proximity, while 01010 would correspond to two adjacent channels in only one of the layers, which is not a valid stub. Thus, the pattern in Fig. 4 can be recognised as a stub made up of a double-hit cluster in one layer, and a single hit in the second layer. Many other valid examples have been observed, but no invalid patterns, confirming that the logic is functioning as expected.

The first beam tests took place in late 2013 (subsequent to the conference) which allowed more detailed studies of stub-finding performance, and results will be reported in due course.

5. Conclusions

Two iterations of a new CMS outer Tracker ASIC have been successfully undertaken. The first prototype version of a 2S-module
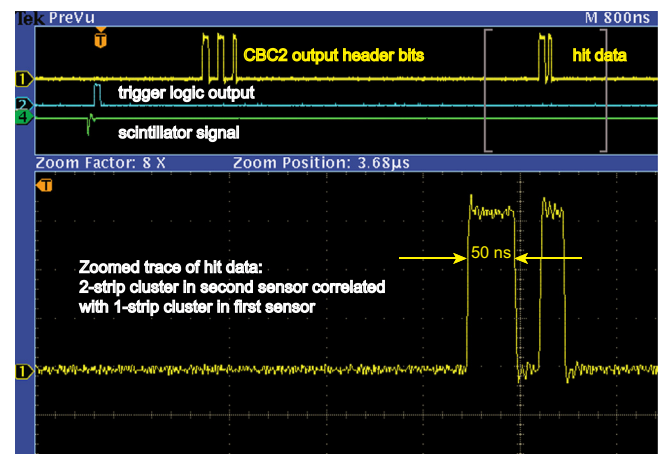

Fig. 4. An example of an oscilloscope observation of a triggered stub. A hit in one sensor generates a 25 ns wide pulse, followed by two 25 ns pulses with a 25 ns gap corresponding to a two-hit cluster in the second sensor.

has been constructed and shown to function well in a laboratory environment. The first beam tests are foreseen for late 2013. A road map for further developments exists, but the detailed schedule depends on a complete upgrade plan for CMS and the HL-LHC approval process.

Acknowledgments

References

[1] The CMS Collaboration, CMS Expression of Interest in the SLHC CERN/LHCC 2007-014, 2007.
[2] The CMS Collaboration, Technical Proposal for the Upgrade of the CMS Detector through 2020, CERN-LHCC-2011-006, 2011.
[3] M. Raymond, et al., Journal of Instrumentation 7 (2012) C01033, http://dx.doi.org/10.1088/1748-0221/7/01/C01033.
[4] The CMS Collaboration, Journal of Instrumentation 3 (2008) S08004.
[5] M. Raymond, et al., The CMS Tracker APV25 0.25 μm CMOS readout chip, in: Proceedings of the Sixth Workshop on Electronics for LHC Experiments, Cracow Poland, 2000; CERN Report CERN 2000-010, 2000, pp. 130–134.
[6] V. Khachatryan, et al., CMS Collaboration, European Physical Journal C 70 (2010) 1165 arXiv:1007.1988[physics.ins-det].
[7] A. Tropiano, PoS Vertex 2012 (2013) 046.
[8] G. Hall, M. Raymond, A. Rose, Journal of Instrumentation 5 (2010) C07012, http://dx.doi.org/10.1088/1748-0221/5/07/C07012.
[9] M. Pesaresi, G. Hall, Journal of Instrumentation 5 (2010) C08003, http://dx.doi.org/10.1088/1748-0221/5/08/C08003.
[10] D. Braga, et al., Journal of Instrumentation 7 (2012) C10003, http://dx.doi.org/10.1088/1748-0221/7/10/C10003.
[11] See ⟨http://www.jedec.org/standards-documents/results/slvs⟩.
[12] W. Ferguson, et al., Journal of Instrumentation 7 (2012) C08006, http://dx.doi.org/10.1088/1748-0221/7/08/C08006.
[13] M. Pesaresi, et al., Journal of Instrumentation 6 (2011) P04006, http://dx.doi.org/10.1088/1748-0221/6/04/P04006.
[14] G. Blanchot, et al., Journal of Instrumentation 8 (2013) C12033, http://dx.doi.org/10.1088/1748-0221/8/12/C12033 (Presented at TWEPP 2013).
[15] D. Braga, et al., Characterisation of the CBC2 readout ASIC for the CMS Strip-Tracker HL upgrade, Presented at TWEPP 2013, Journal of Instrumentation, in press, 2014.