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High-voltage pixel sensors for ATLAS upgrade ☆

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ABSTRACT

The high-voltage (HV-) CMOS pixel sensors offer several good properties: a fast charge collection by drift, the possibility to implement relatively complex CMOS in-pixel electronics and the compatibility with commercial processes. The sensor element is a deep n-well diode in a p-type substrate. The n-well contains CMOS pixel electronics. The main charge collection mechanism is drift in a shallow, high field region, which leads to a fast charge collection and a high radiation tolerance. We are currently evaluating the use of the high-voltage detectors implemented in 180 nm HV-CMOS technology for the high-luminosity ATLAS upgrade. Our approach is replacing the existing pixel and strip sensors with the CMOS sensors while keeping the presently used readout ASICs. By intelligence we mean the ability of the sensor to recognize a particle hit and generate the address information. In this way we could benefit from the advantages of the HV sensor technology such as lower cost, lower mass, lower operating voltage, smaller pitch, smaller clusters at high incidence angles. Additionally we expect to achieve a radiation hardness necessary for ATLAS upgrade. In order to test the concept, we have designed two HV-CMOS prototypes that can be readout in two ways: using pixel and strip readout chips. In the case of the pixel readout, the connection between HV-CMOS sensor and the readout ASIC can be established capacitively.

1. Introduction

High-voltage CMOS active pixel detectors are a family of active pixel detectors that unifies several good properties: fast charge collection by drift, CMOS in-pixel electronics and the compatibility with commercial processes. The sensor element is a deep n-well diode in a p-type substrate. CMOS pixel electronics is implemented inside the deep n-well. In contrast to other CMOS monolithic detectors, the collection electrode of a HV-CMOS pixel is large – it occupies about 50% of the pixel area Fig. 1 (the pixel size is 33 μm × 125 μm and the diode size 19 μm × 110 μm). Because of this we expect an efficient charge collection with small signal degradation after high irradiation doses.

Several publications describe the development of HV-CMOS sensors. The results of the proof-of-principle development stage have been presented in Refs. [1–7]. In this project stage, we have tested three detector types:

- monolithic detectors with charge integrating pixel electronics and rolling shutter readout [5,6],
- monolithic detectors with in-pixel hit detection and zero suppressed readout [1,2],

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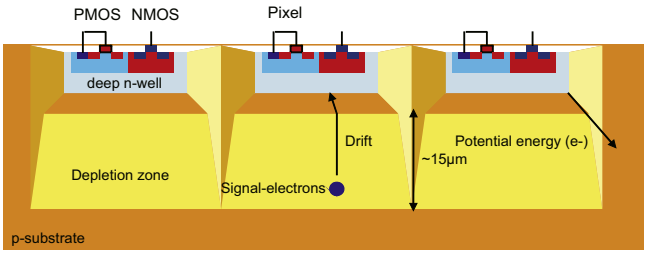

Fig. 1. Three high-voltage pixels. The pixel electronics of every pixel are enclosed by a deep n-well.

- hybrid pixel detectors based on active HV-CMOS sensors and capacitive chip to chip signal transmission [3,4].

With all these detector types we have measured sufficient signal to noise ratios (>20), even after irradiation with neutrons to 10^{15} n_{eq}/cm^2 [7]. With the rolling shutter monolithic detector we have measured $>98\%$ detection efficiency in beam test, as well as a spatial resolution of 3–4 μm [8,9].

We are developing HV-CMOS detectors for the following applications:

(1) *Experiment Mu3e at Paul Scherrer Institute* (*PSI*), *Switzerland*: A HV-CMOS pixel detector with an area of almost 2 m^2 is planned. The detector thickness should be about 50 μm. The use of in-pixel hit detection and signal processing should allow a time resolution of 100 ns. The Mu3e pixel detector and its HV-CMOS active pixel sensor have been described in Refs. [10,11]. Similar detector will be used for the Panda luminosity monitor.

(2) *High-luminosity ATLAS upgrade*: As already mentioned, we have designed two HV-CMOS prototypes. Several results obtained with the first test detector have been presented in Refs. [8–10]. In this publication we present also the results obtained with the second prototype.

2. Intelligent sensor concept

An "intelligent" HV-CMOS sensor implements pixels that respond to particle hits by generating address signals. The pre-requisite is here that the pixels can distinguish the particle signals from noise, by means of pulse height discrimination. The address signal is a pulse (current or voltage) with a defined amplitude. We encode the pixel position as the amplitude. Several pixels can be grouped and their address signals transmitted via the common line. The group of pixels is readout using one channel of a readout chip. In the case of the readout with the pixel readout chip FE-I4 [12], three HV-CMOS pixels (size 33 μm × 125 μm) are connected to one FE-I4 pixel (size 50 μm × 250 μm). When connecting to a strip readout chip, we will connect typically 100 pixels to a single channel. In both cases we obtain a pixel sensor with a higher number of pixels than the number of readout channels.

3. Test detectors

The structure of the test detector CCPD1 (HV2FEI4) has been described in Refs. [8,10]. The first publication concentrates on the readout with a pixel chip, while the second discusses the readout with a strip readout chip. The simplified pixel schematics, as implemented in CCPD1, are shown in Fig. 2.

The sensor signal is amplified with a charge sensitive amplifier (A). The amplifier output is connected to a voltage comparator (C). A four bit threshold tune D/A convertor is used for fine in-pixel adjustment of the threshold. The comparator output enables a

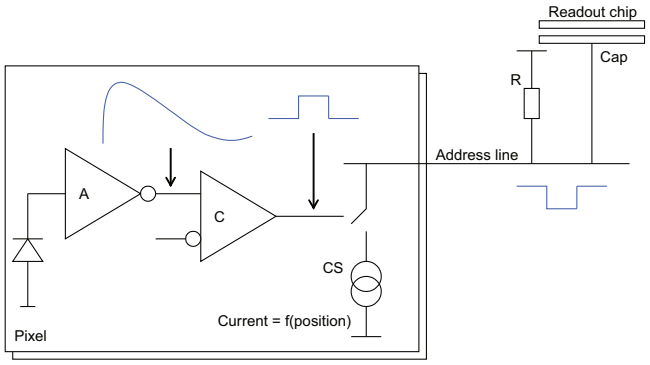

Fig. 2. Simplified pixel schematics.

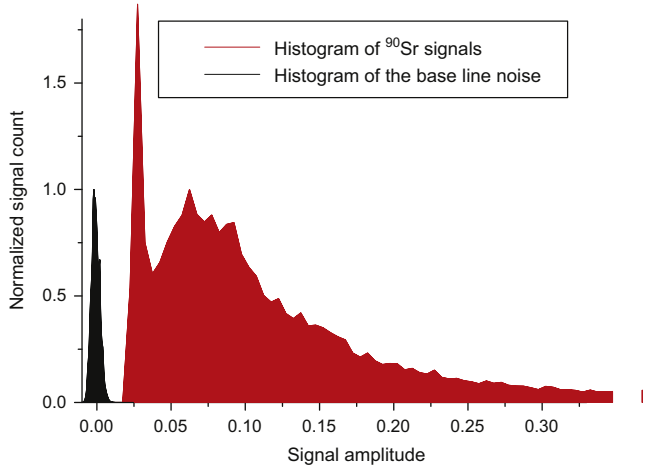

Fig. 3. Red: spectrum of beta particle signals when a CCPD1, irradiated to 10^{15} n_{eq}/cm^2, is exposed to ^{90}Sr source. Black: base line noise. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this article.)

current source (CS). The current generated by the source is a function of the pixel position. In the case of the pixel readout mode, the pixels are grouped into groups of three and connected to FE-I4 channels. The current outputs of the pixels belonging to the same group are summed and converted to voltage using a resistance (R). The voltage signal is transmitted capacitively to the readout chip. It is also possible to group the pixels into larger groups of 36 and use the same readout method of summing. Since we have less groups per matrix, than in the case of the pixel scheme, readout can be done using a strip readout chip. The experimental results performed with CCPD1 will be presented in separated publications. In this publication, we will only mention a few important results.

The capacitive signal transmission has been successfully tested with a CCPD1 glued to a FE-I4 ASIC using a flip chip machine for precise alignment. No bump bonds have been used, the bare chips were glued together. The time over threshold response of the FE-I4 shows the three signal amplitudes that correspond to the three pixel positions.

Several (one for every irradiation) CCPD1 chips have been irradiated at Jozef Stefan Institute in Ljubljana, Slovenia, with neutrons (doses 10^{15} n_{eq}/cm^2 and 10^{16} n_{eq}/cm^2), at CERN (PS) with 23 GeV protons (doses 80–380 Mrad or $1.55-7.4$ n_{eq}/cm^2) and at CERN with 10 keV x-rays (50 Mrad). Preliminary results show a relatively good signal to noise ratio after irradiation with neutrons up to the dose of 10^{15} n_{eq}/cm^2. Notice that neutrons cause mostly non-ionizing (displacement) damage in the bulk material. Fig. 3 shows the spectrum of beta particle signals when

a CCPD1, irradiated to 10^{15} n_{eq}/cm^2, is exposed to ^{90}Sr source. The spectrum has been recorded with a single pixel – the amplifier output has been measured with an oscilloscope. The measurement has been done at 5 °C to reduce the detector leakage current; the high voltage bias was −55 V. The most probable value (MPV) of the ^{90}Sr distribution is about 62 mV. The base line noise has a sigma value of about 2.9 mV. This leads to a signal to noise ratio of about 20. By performing calibration measurements with ^{55}Fe x-ray source we calculate that the ^{90}Sr MPV signal measured by the irradiated chip corresponds to 1180 e. With a fresh detector we measure about 1600 e for the nearly equal high voltage bias (−50 V). The signal decrease due to irradiation is therefore 26%.

Since CCPD1 was not designed using transistor layout techniques for radiation hardness, it suffered from ionizing damage in silicon dioxide in the case of proton and x-ray irradiations. Nevertheless, we were able to measure beta particle spectra after 80 Mrad proton irradiation.

The main improvement in the second prototype CCPD2 is the use of radiation tolerant transistor layout. We have tried several pixel layouts: in one ("partially rad-hard pixel") only the NMOS transistors with a bias current lower than 1 nA have circular gate, while the other transistors are linear. In the second layout ("fully rad-hard pixel"), almost all NMOS transistors have circular gates. In both cases, different NMOS transistors are separated with guard rings.

4. Novel address scheme

The discriminator in the CCPD1-pixels and in the partially and fully rad-hard pixels of CCPD2 uses only NMOS transistors. This realization reduces crosstalk, improves speed, but it has some limitations. The most important one is the low voltage of the output signal (amplitude <1.8 V). For some applications a CMOS signal of an amplitude of 1.8 V would be preferable. Because of this, we have implemented in CCPD2 the so called "simple pixels" with the discriminator that consists only of two transistors and generates the full-swing CMOS output.

The availability of the CMOS discriminator allows us to implement slightly different pixel address scheme. Let us for the moment consider the strip-like readout (segmented strip detector). The pixel address line propagates through all the pixels of one group (in our case 36 pixels) as a "daisy chain". In every pixel, there is a current source connected to the address line that generates current I_0. In every pixel there is also a switch that allows splitting the address line to the segment before and after the pixel. Schematic diagram is shown in Fig. 4. When a discriminator detects a particle hit, its CMOS output signal will turn off the switch. In this way the current that flows into the line connection (I_{in}) will be reduced by the amount of the current generated by all the disconnected current sources after the pixel that detected the hit. The current reduction is therefore proportional to the pixel position. Such a current mode signal is converted to voltage using a resistor.

As comparison we have depicted the old address scheme (as implemented in CCPD1 and in the fully/partially rad-hard pixels) in the same figure below. Here a particle hit turns on a current source in the hit pixel. Current sources in different pixels have different current amplitudes and all current sources are connected to the address line.

The advantage the new scheme compared to the old one is that the input current I_{in} is a monotonic function of the pixel position, also in the case of a high mismatch between the current sources. Additionally, in the case of multiple simultaneous hits, the new scheme generates a valid address of the first hit pixel, while the second scheme generates an amplitude sum, that is a measure of the "center of gravity" of the hit pixels and does not always allow a simple reconstruction of any of the hit pixel positions.

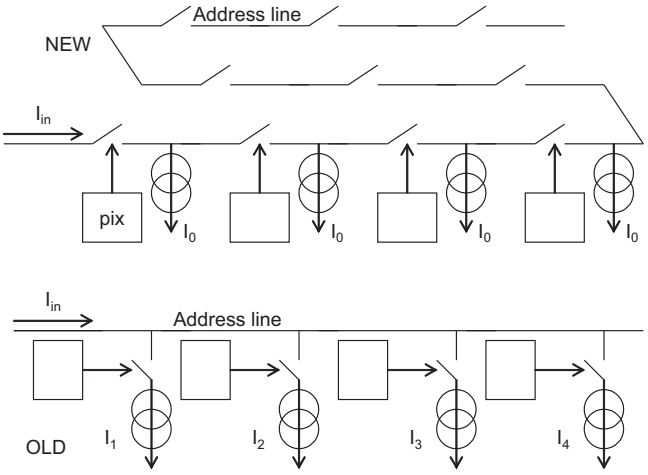

Fig. 4. Addressing schemes.

Moreover, the new scheme based on switches can be easily extended by adding more address lines (one per hit multiplicity), so that it can cope with multiple hits. For instance, one line gives the valid address of the first and the other of the last hit pixel in the "pixel chain". the In this way, a good efficiency in the case of a high occupancy can be achieved, while keeping the number of the channels per matrix much lower than in the case of the pixel readout.

5. Experimental results

Testing of CCPD2 prototype is still ongoing. The test programm can be summarized as follows:

- *Stand-alone detector tests*: They include the tests with the electrical signals (the charge injection circuit), the measurements with the radioactive sources and the laser measurements. The goals of these measurements are functionality checks, measurements of noise and threshold dispersion, estimations of minimum ionizing particle (MIP) signal amplitude and the charge collection properties.
- Measurements on irradiated samples.
- Tests of detectors bump bonded to a pixel readout chip.
- Tests of detectors readout by a strip readout chip.

We will concentrate here on the tests with the stand-alone readout fresh and irradiated samples. The results with prototypes connected to the readout chips will be presented elsewhere. The stand-alone measurements use the possibility, implemented in the detector, to connect the pixel address lines to a "monitor" wire that can be accessed from outside through an chip input pad. Additionally, several outputs of the charge sensitive amplifiers can be measured directly, which is especially useful for the spectral measurements.

An example of such a spectral measurement is shown in Fig. 5. We have exposed the sensor with the x-ray source ^{55}Fe and the beta source ^{90}Sr. The peak of the ^{55}Fe spectrum can be easily recognized and it corresponds to the photon energy of 5.9 keV or the sensor signal of about 1660 e. The most probable value of the ^{90}Sr signal depends on the sensor bias voltage. The signal was about 1700 e for 70 V bias. Measured average noise in the pixels is about 75 e (RMS) and the threshold dispersion after tuning had a sigma value of about 25 e. Such noise, threshold dispersion and

signal values should allow a good detection efficiency. This will be checked in the beam tests.

As already mentioned, the main improvement of CCPD2 versus the older prototype is the use of radiation tolerant transistor layout.

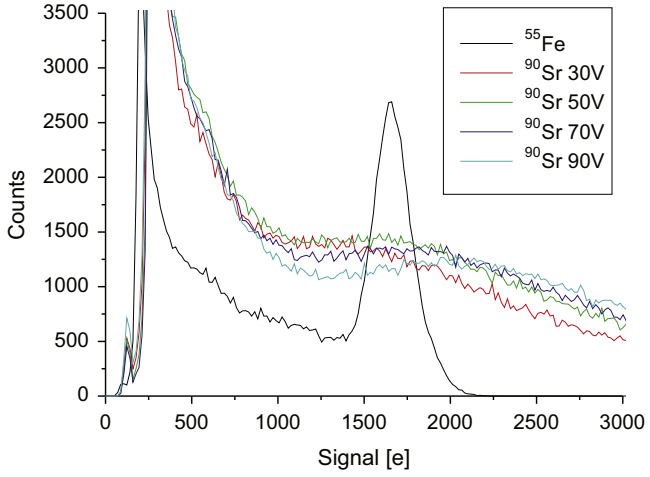

Fig. 5. Spectra of the particles irradiated by ^{55}Fe and ^{90}Sr sources and recorded with CCPD2.

We have irradiated one CCPD2 sample with 10 keV x-rays (at CERN) up to the dose of 862 Mrad with x-rays. The chip was on during the irradiation and it was annealed at 70 °C for 2 h every incremental dose step of 100 Mrad.

All the pixel types were operational after irradiation with some increase in noise: typically 150 e RMS noise were measured at room temperature. We have observed pixel amplifier gain decrease during the irradiation, while we kept the bias parameters of the amplifier constant. After re-tuning of the amplifier bias parameters the gain of the fully rad-hard amplifiers recovered to the initial values, while the gain of the partially rad-hard amplifiers remained decreased by factor of two. The gain decrease is probably caused by leakage currents in the transistors used in the amplifier. Use of enclosed transistors mitigates this problem. We have also observed an increase of HV leakage current. The current increase can be nearly completely removed by annealing. The origin of the leakage current is still unclear.

We have also tested the novel pixel type with the CMOS discriminator, particularly its advantages in the case of the segmented strip readout. The test have been done in stand-alone mode. The schematic of the measurement setup is shown in Fig. 6. The readout line is connected to the monitor pad, which is connected to an external trans-impedance amplifier (current to voltage converter). The output signals are recorded by an oscilloscope. We have used ^{55}Fe x-ray source to generate signals, and a piece of

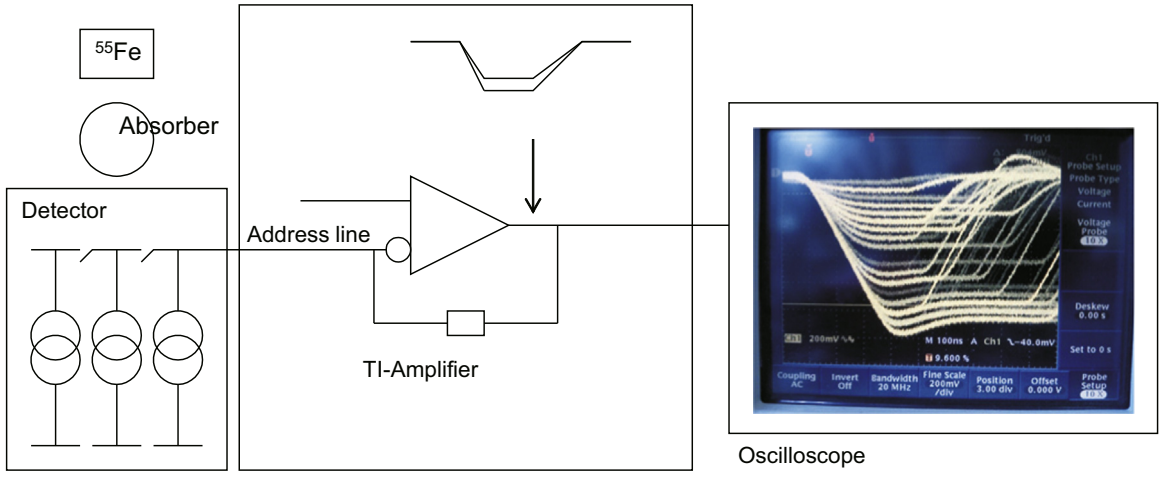

Fig. 6. Measurement setup.

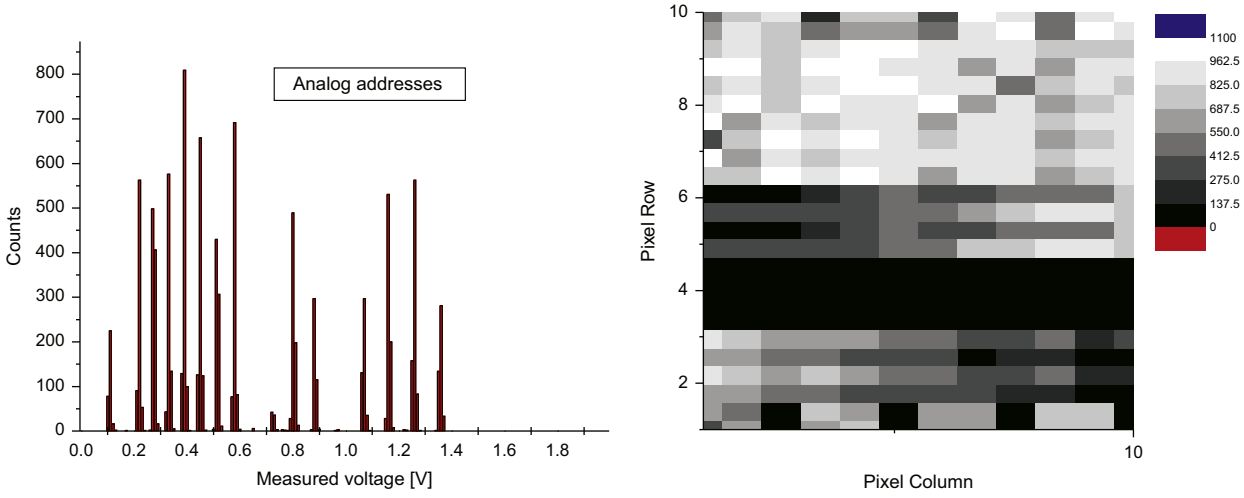

Fig. 7. ^{55}Fe shadow image recorded by CCPDs in segmented strip readout mode. Left: histogram of the received amplitudes – discrete voltage levels that encode the different pixel addresses can be clearly distinguished. Right: reconstructed shadow image.

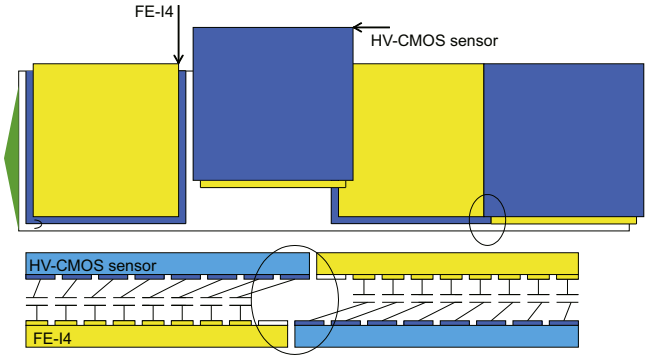

Fig. 8. Tile-like CCPD structure without insensitive regions.

wire as an absorber. The histogram of the received signal amplitudes is shown in the left side of Fig. 7.

The discrete voltage levels that encode the different pixel addresses can be clearly distinguished. Certain addresses are missing since they belong to the pixels covered by the absorber. It should be noted here that the address line connection scheme is rather complicated. The pixels are connected in a snake-like way, as indicated in Fig. 4.

Due to a design error we have only 18 address levels in a group of 36 pixels because every two neighbors share an equal address. It order to reconstruct the image, we have performed one additional calibration: we measured the address levels of each pixels separately, by applying test injection signals. This measurement gives us the address to pixel assignment, which can be used to map the measured address histogram to pixel positions. The result is shown in Fig. 7, right. The shadow of the wire can be recognized. The image non-uniformities can be related to the mentioned error in address scheme and a threshold non-uniformity.

6. Conclusion and outlook

High-voltage CMOS active pixel detectors are a family of active pixel detectors that can be implemented in standard CMOS (HV) processes and that relay on the use of high voltage (up to 100 V) to deplete the sensor diodes and improve the charge collection efficiency. HV-CMOS sensors are based on the so-called "smart diode" structure, where a collection electrode (n-well) occupies about 50% of the pixel area (the pixel size is 33 μm × 125 μm and the diode size 19 μm × 110 μm), and CMOS electronics is implemented inside the electrode. Good properties are fast charge collection by drift, high radiation tolerance (compared to other CMOS sensors), the use of a standard CMOS process, the possibility to produce thin sensors. A pixel detector based on HV-CMOS sensor structure is proposed for Mu3e experiment. Similar detector will be used for the Panda luminosity monitor. We are also evaluating the use of the high-voltage detectors implemented in 180 nm HV-CMOS technology for the high-luminosity ATLAS upgrade. We have designed and tested two HV-CMOS detector prototypes for ATLAS. The sensors can be readout using standard ATLAS pixel readout chip FE-I4 and using strip readout ASICs. In the case of pixel readout, no bump bonding is needed, the signals can be transmitted capacitively from the detector chip to the readout chip. The HV-CMOS sensor prototypes perform well with a signal to noise ratio sufficient for good minimum ionising particle detection efficiency. Signal to noise ratio after irradiation to 10^{15} n_{eq}/cm^2 is about 20. We have also demonstrated the capacitive signal transmission to FE-I4, as well as the possibility to encode the pixel position as signal amplitude, which allows construction of the detector with 2D spatial resolution that is readout with strip readout chip – the segmented strip detector. Next steps will include the evaluation of the hit detection efficiency in a test beam. We are also planning to design a reticle size sensor. The reticle size of HV-CMOS sensors matches well to the size of the FE-I4 ASIC, which can allow construction of large area detectors. One possible sensor arrangement is shown in Fig. 8. The HV-CMOS sensor could be made slightly larger in *z*-direction to allow tile-like structure without insensitive regions. No bump bonding is required and flip-chip alignment precision of ~ 10 μm would be sufficient to make a functional detector.

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