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A high precision radiation-tolerant LVDT conditioning module

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ABSTRACT

Linear variable differential transformer (LVDT) position sensors are widely used in particle accelerators and nuclear plants, thanks to their properties of contact-less sensing, radiation tolerance, infinite resolution, good linearity and cost efficiency. Many applications require high reading accuracy, even in environments with high radiation levels, where the conditioning electronics must be located several hundred meters away from the sensor. Sometimes even at long distances the conditioning module is still exposed to ionizing radiation. Standard off-the-shelf electronic conditioning modules offer limited performances in terms of reading accuracy and long term stability already with short cables. A radiation tolerant stand-alone LVDT conditioning module has been developed using Commercial Off-The-Shelf (COTS) components. The reading of the sensor output voltages is based on a sine-fit algorithm digitally implemented on an FPGA ensuring few micrometers reading accuracy even with low signal-to-noise ratios. The algorithm validation and board architecture are described. A full metrological characterization of the module is reported and radiation tests results are discussed.

1. Introduction

Linear variable differential transformers (LVDT) are widely used in industry, thanks to their properties of contact-less sensing, ruggedness, infinite resolution, good linearity and cost efficiency [1]. In addition they can be set up to be radiation tolerant with proper insulation techniques [2], making them well suited to harsh environments with ultra-high vacuum conditions [3] or high radiation levels, such as in high energy particle accelerators [4]. Many applications require reading uncertainty as low as a few micrometers even with reading electronics located far from the sensor because of the harsh environment [5]; this is, for instance, the case of the Large Hadron Collider (LHC) collimators position survey system [6]. Moreover there are zones, as for instance in the CERN accelerator complex, such as the Super Proton Synchrotron (SPS) or the Proton Synchrotron (PS) Booster [7], where the electronics cannot be protected in dedicated alcoves and need to be tolerant to high radiation levels. Many off-the-shelf modules guarantee the compatibility with any kind of LVDT and the interface with industrial control systems through Profibus, ModBus RTU or analog interface communication standards. There are several reading techniques implemented on these modules: for instance the simple synchronous analogic demodulation or digital signal processing techniques, such as the Goertzel algorithm [8]. Their reading uncertainty unfortunately is not below a few hundreds of micrometers. In addition these modules are not radiation tolerant, therefore in radioactive applications they should be placed in safe areas, even up to several hundred meters away from the LVDT, with a consequent reduction of the signal-to-noise ratio (SNR) at the module input and increasing of the reading uncertainty. The reading accuracy can be increased by adopting a ratiometric reading technique combined with the use of a three-parameter sine-fit algorithm for the extraction of the first harmonics of the secondary voltages [9]. In this paper a stand-alone LVDT conditioning module that has been tested with a 230 MeV proton beam up to a Total Integrated Dose (TID) of 200 Gy and a fluence of 3.9×10^{11} pp/cm^2 is presented. The module guarantees a reading accuracy of a few micrometers even with cable lengths of several hundred meters. In Section 2 the state of the art of the current off-the-shelf LVDT conditioning modules is reported, while in Section 3 the chosen solution is described, the advantages and the main features are pointed out together with the module architecture and reading algorithm. In Section 4 details on the algorithm implementation are discussed together with the results of numerical simulations carried out to validate the proposed algorithm and evaluate its performance according to the SNR value of the input signals. Furthermore in Section 5 experimental results of the module functionality are provided, giving details of a proper metrological characterization. Results of radiation tests are shown, first discussing each Commercial Off-The-Shelf (COTS) component used in the board design and then evaluating the radiation tolerance of the entire module.

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2. The problem: state of the art of LVDT conditioning modules

The LVDT is an electro-mechanical transducer where a physical movement of the core is detected as a change in magnetic coupling between the internal windings.

Fig. 1 shows the LVDT working principle: by applying an excitation sinewave $s(t)$ at a fixed frequency f_0 a voltage is induced in the secondaries, the difference between the two secondary voltages is linearly proportional to the core absolute position. Given the primary input signal $s(t)$ with amplitude A_P and frequency f_0 as

$$s(t) = A_P \cos(2\pi f_0 t) \tag{1}$$

the differential amplitude modulated secondary voltage $y(t)$ can be expressed as

$$y(t) = A(x) \cos(2\pi f_0 t + \phi) \tag{2}$$

where $A(x)$ depends on the LVDT core position.

LVDT sensors are generally manufactured in a 4-wire or 5-wire configuration: in the former the signal at the output terminals is the difference of the secondary windings, in the latter the voltage at each secondary winding can be measured with respect to their connection point, provided as an additional output wire. Traditional analog single chip solutions perform the functions of AC amplification, demodulation and low pass filtering. Such devices are available in monolithic form, but can also be built from discrete parts to tailor them to the specific application. Mixed signal conditioning modules offer different design solutions and interface options, for instance mixing an ASIC design with a microcontroller unit [10] or using fast DSP processors to realize the LVDT reading algorithm. The most common LVDT reading technique consists of a demodulation of the LVDT output obtained by multiplying a signal synchronous with the carrier $s(t)$ and low pass filtering the result:

$$\begin{aligned}[y(t)\cdot\cos(2\pi f_0 t)]_{lowpass} &= [A(x)\cdot\cos(2\pi f_0 t+\phi)\cdot\cos(2\pi f_0 t)]_{lowpass}\\ &= \left[A(x)\cdot\frac{\cos(\phi)}{2}+A(x)\cdot\frac{\cos(2\pi 2 f_0 t+\phi)}{2}\right]_{lowpass}\\ &= A(x)\cdot\frac{\cos(\phi)}{2}.\end{aligned} \tag{3}$$

Using this technique the reading output is a function of the phase difference ϕ and consequently of the cable length used to drive the sensor. For instance this approach is used in the Philips Semiconductors ™SE5521 [11], but it is not appropriate for long cable lengths, since long cables between the sensor and the electronics transform the impedance seen by the conditioner from inductive to capacitive, making phase recovery quite challenging and computationally expensive. The commercial standards AD598 and AD698 [12] use a ratiometric algorithm to calculate the core position. The AD698 divides the secondary differential voltage by the input excitation signal and therefore the output is also phase sensitive. The AD598 instead is based on the ratio of the difference between the two secondary signals and their sum. This requires that the sum of the LVDT secondary voltages remains constant with the stroke length and the noise immunity of this solution is not better than the one obtained using synchronous demodulation [13]. Applications that do not need to determine the phase of the ac signal can also use one of three basic methods to obtain a dc voltage from an ac voltage: rms-to-dc conversion [14], peak detection and AC-to-MAV (mean absolute value) conversion. Although these methods can be realized with simple circuitry, they do not compensate for possible drifts of the excitation signal and do not reach the accuracy level of ratiometric algorithms. Table 1 shows a few commercially available modules organized by reading algorithm and communication interface. Most of the standard COTS LVDT conditioning modules can be set up to generate frequencies in the range 1–20 kHz, with a Full Scale Output (FSO) linearity error of 0.05%, a maximum cable length of 30 m between the sensor and the electronics and a maximum temperature coefficient of 0.01% FSO/°C.

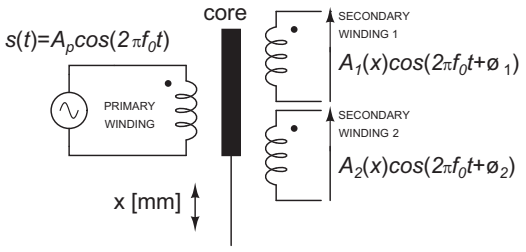

Fig. 1. Working principle of a generic linear variable differential transformer (LVDT).

Traditionally the output is a DC or an AC voltage proportional to the core position, but many modules also provide a digital output interface, for instance the Alliance Sensor™ S1A has a RS485 2-wire multidrop network and can be connected in Master/Slave mode. None of the reported devices and discussed techniques are able to provide a reading accuracy below a few hundreds of micrometers, even with only short cables.

3. The proposed solution

A three-parameter sine-fit algorithm to reconstruct the signal from the LVDT secondaries and a ratiometric formula to compute the value of the core absolute position have been chosen as the reading technique. This choice allows the local tuning of the device to compensate for phase errors between the primary and the secondary signal to be avoided, and at the same time guarantees a reading accuracy of a few micrometers even with low signal-to-noise ratios [9].

3.1. The reading algorithm

The chosen sine-fit algorithm is a three-parameter least-squares fit to a sinewave signal. Assuming that the input data from the LVDT secondaries is the sequence of M samples $y_1, y_2, \ldots, y_M$, taken at times $t_1, t_2, \ldots, t_M$, the algorithm finds the values of A_0, B_0, and C_0 that minimize the following sum of squared differences:

$$\sum_{n-1}^{M} [y_n - A_0 \cos(\omega_0 t_n) - B_0 \sin(\omega_0 t_n) - C_0]^2 \tag{4}$$

where ω_0 is the angular frequency of the input signal. The values of A_0, B_0, and C_0 are calculated first creating the matrices

$$\mathbf{D_0} = \begin{bmatrix} \cos(\omega_0 t_1) & \sin(\omega_0 t_1) & 1 \\ \cos(\omega_0 t_2) & \sin(\omega_0 t_2) & 1 \\ \vdots & \vdots & \\ \cos(\omega_0 t_M) & \sin(\omega_0 t_M) & 1 \end{bmatrix} \tag{5}$$

Table 1
Commercial Off-The-Shelf LVDT conditioning modules.

Product ID	Comm. interface	Reading algorithm
AD698	DC	Ratiometric
AD598	DC	Ratiometric
SE5521	AC or DC	Synchronous demodulation
S1A	DC or RS485	Synchronous demodulation

$$\mathbf{y_0} = \begin{bmatrix} y_1 \\ y_2 \\ \vdots \\ y_M \end{bmatrix} \tag{6}$$

$$\mathbf{x_0} = \begin{bmatrix} A_0 \\ B_0 \\ C_0 \end{bmatrix} \tag{7}$$

and then rewriting (4) as

$$(\mathbf{y} - \mathbf{D_0 x_0})^T (\mathbf{y} - \mathbf{D_0 x_0}). \tag{8}$$

It can be demonstrated [15,16] that the least-squares solution, $\mathbf{x}_0$, that minimizes (8) is given by

$$\mathbf{x_0} = \mathbf{D}^{\dagger}\mathbf{y} \tag{9}$$

where

$$\mathbf{D}^{\dagger} = (\mathbf{D_0^T D_0})^{-1} \mathbf{D_0^T}. \tag{10}$$

The fitted signal y'_n is finally given by

$$y'_n = A\ \cos(\omega_0 t_n + \theta) + C \tag{11}$$

where the amplitude A, the phase θ and offset C are calculated through the coefficients A_0, B_0 and C_0 [15]. The amplitude A of the fitted sinewave is the parameter relevant to our application and is given by (12)

$$A = \sqrt{A_0^2 + B_0^2}. \tag{12}$$

Assuming that V_A and V_B are the fitted amplitudes of the two LVDT secondary outputs, the final position P of the core inside the sensor is retrieved using the formula

$$P = k \cdot r \tag{13}$$

where r is calculated using the ratiometric relation

$$r = \frac{(V_A - V_B)}{(V_A + V_B)} \tag{14}$$

and k is a constant gain characteristic of the LVDT sensor. Eq. (13) is an approximate calculation of the core position and it has been used in all the experimental tests, although in the final application the actual core position is calculated using a linear interpolation algorithm based on r, the module output value, and a set of coefficients resulting from the calibration of the LVDT sensor [6].

3.2. Architecture of the module

The LVDT conditioning module has a DIN rail format and it can be connected to one 4-wire or 5-wire LVDT. Fig. 2 shows the top view of the module.

The module is operated by a ProASIC3E FPGA manufactured by Actel ® [17]. The secondaries input stage features a Texas Instrument INA2128UA and OPA2227UK amplifiers connected in series to provide high input impedance and filter out high frequencies. The Analog-To-Digital conversion of the input signals is performed by the MAX11046 ADC manufactured by Maxim Integrated™. The ADC has eight channels with 16 bits of resolution and its input range, dynamic performance and parallel architecture make it well suited for the conditioning module. A Resistance Temperature Detector (RTD), usually a PT100, is integrated on LVDT sensors. The board excites the RTD with a current and measures the sensor resistance variation. The excitation current is generated using an ADR434BRZ Voltage Reference and an OPA2134UA operational amplifier. The temperature of the board is measured by a surface mount LM45CIM3 Integrated Circuit directly connected to the ADC. The input signal for the primary winding of the LVDT is synthesized in the FPGA using Direct Digital Synthesis (DDS) and then sent to a

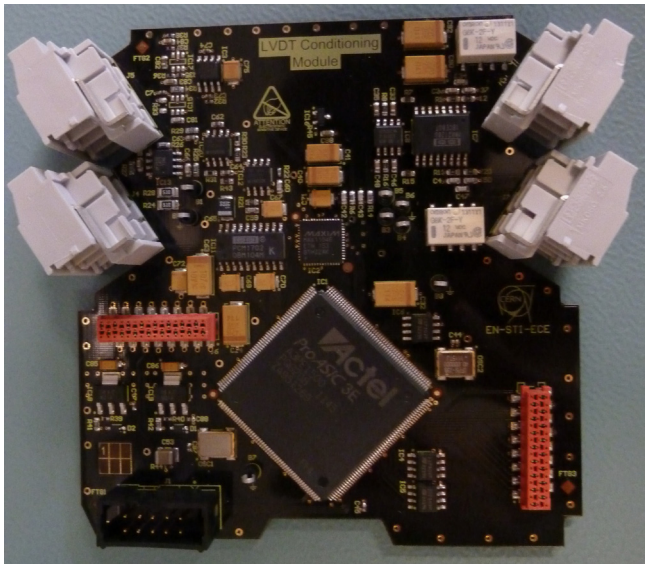

Fig. 2. Top view of the LVDT conditioning module.

PCM1702 20 bits DAC. The module allows the user to choose output frequencies in a range 1–3.875 kHz at steps of 125 Hz with precision better than 1 mHz. The signal is low-pass filtered by a OPA2134UA and amplified by a LM7372, before being fed to the LVDT primary connector. The values of the sinewave amplitude used for digital synthesis, as well as the coefficients of $\mathbf{D}^{\dagger}$, are permanently stored within three M25P05 flash memories. Flash based devices show higher tolerance to SEUs compared to SRAM based ones, but SRAM memories are faster to access, hence they are necessary in order to respect timing specifications. For this reason all data stored in the external FLASH memories is loaded at power-up within dedicated SRAM cells inside the FPGA: the SRAM blocks are constantly read, to realize the fitting algorithm and the primary signal, and rewritten with the FLASH memories contents, to mitigate the possibility of SEUs. In addition Actel SRAM blocks are designed so that two bits of the same SRAM word are never stored in nearby cells [18], whether in the horizontal or vertical direction, therefore the probability of multiple-bit upset in SRAM blocks is highly reduced. The functional block diagram of the module is shown in Fig. 3.

The conditioning module is interfaced via UART using the MODBUS over serial line communication protocol. Serial communication is realized through a MAX3491ESD transceiver mounted on a separate DIN-rail module called 'PowerCOM' and connected via Micro-MaTch connectors. This separate board provides also the necessary power supplies, ± 5 V and ± 15 V.

4. The algorithm validation

4.1. Algorithm implementation

The reading algorithm was realized using fixed point representation and optimized to reduce FPGA area allocation while meeting target timing constraints [19]. The sinefit coefficients of matrix $\mathbf{D}^{\dagger}$ are represented with 16 bits and $Q_{-9,24}$, using Q notation for fixed point arithmetic, ensuring maximum bit resolution with no overflow occurrence. The quantization of these coefficients results in a modification of the sinefit frequency response, with 10 ppm maximum error committed on the amplitude estimation. The ADC sampled input signals are represented with 16 bits and $Q_{0,15}$. The FPGA does not feature a dedicated multiply-accumulate (MAC) unit: an accumulator based on a ripple carry adder is hardwired in

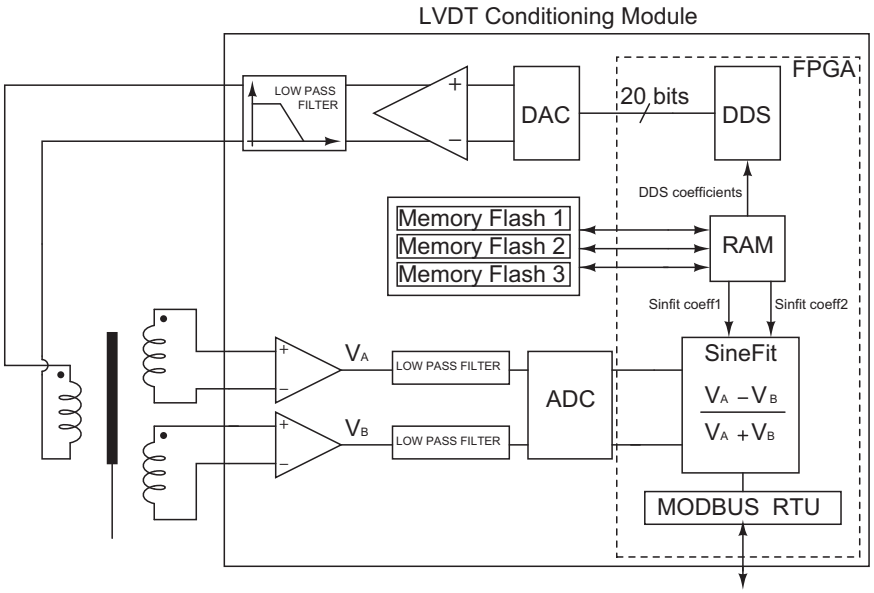

Fig. 3. Functional block diagram of the LVDT signal conditioning module.

the FPGA and performs the calculation of matrix $\mathbf{x_0}$ in (9). The final output data word of the MAC unit has 41 bits with $Q_{0,40}$, where extra bits have been added to avoid overflow errors. The square root operation in (12) is based on the CORDIC algorithm in vectoring mode [20]. The underlying equations rotate a vector with magnitude defined by cartesian coordinates (x_n, y_n) by whatever angle is necessary to align it with the x-axis. Assuming n to be the number of iterations, the final result of this calculation is represented by the following set of equations:

$$x_n = A_n\sqrt{x_0^2+y_0^2}$$
$$y_n = 0$$
$$z_n = z_0 + \tan^{-1}\left(\frac{y_0}{x_0}\right) \tag{15}$$

where z_n is the equation of the angle accumulator and x_0, y_0 and z_0 the initial values. Assigning $x_0 = A_0$ and $y_0 = B_0$ yields (12) scaled by a factor A_n, thus the value of x_n corresponds to the amplitude of the input sinusoidal signal V_A or V_B. Since the algorithm converges only if the rotation angles are in the domain $[-\pi/2, \pi/2]$, x_0 and y_0 are assigned with the absolute values of A_0 and B_0. The scaling factor A_n can be neglected since the following ratiometric operation cancels it out. The sum and difference of the two estimated amplitudes are computed and then given in input to a second CORDIC core in vectorial mode. A simple modification to the CORDIC equations [21] permits the computation of linear functions and a method for evaluating ratios, the equations for x_n, y_n and z_n then become

$$x_n = x_0$$
$$y_n = 0$$
$$z_n = z_0 - \left(\frac{y_0}{x_0}\right). \tag{16}$$

By choosing $y_0 = (V_A - V_B)$, $x_0 = (V_A + V_B)$ and $z_0 = 0$ the output z_n is the ratiometric result r of (14). Both CORDIC implementations introduce an error due to the quantized representation of the rotation angles and the finite number of iterations. Since a long data word is used in input, the best choice is to use a number of iterations equal to the number of bits used to represent the input data word, hence $n=41$ is used to get the amplitudes of the fitted sinewaves and $n=42$, one extra guard bit being added, to calculate the ratio r. Fig. 4 shows the algorithm stages with fixed point arithmetic representations. The two CORDIC cores have been

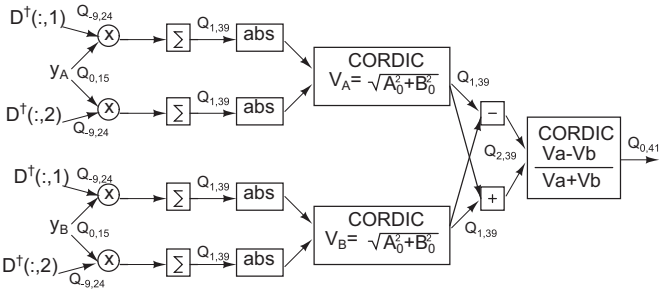

Fig. 4. Block diagram of the algorithm, showing at each stage the fixed point Q representation of the inputs and outputs [19].

realized using the Actel proprietary core [22], choosing word serial architecture for its good trade-off between speed and FPGA area occupation.

Finally the core position P is calculated using (13) assuming $k=100.0$, a standard value for commercial LVDT sensors. Since usually PLCs have 40 bits representation, when the board receives a data request via MODBUS only the 40 most significant bits of the 42 bits value of r are transmitted.

4.2. Simulation results

Simulations were carried out to study the minimum number of samples n_s required to get an uncertainty on the position $\sigma_P < 1$ μm with different values of signal-to-noise ratio of the input signal. Tests performed in the laboratory showed, in the worst case of 800 m cable length, a typical SNR value of 60 dB of the LVDT signals at the ADC input.

Fig. 5 shows σ_P as a function of different core positions in the cases of $n_s=100$, $n_s=500$, $n_s=1500$ and $n_s=2000$, with an input SNR of 60 dB. The ADC sampling frequency has been set at $f_s=250$ kS/s [9]. As a result only $n_s=2000$ ensures an uncertainty below 1 μm over the whole sensor range. With $f_s=250$ kS/s and $n_s=2000$ the acquisition time is $t_A=8$ ms. The total processing time of the sinefit algorithm is $t_p = 2.1$ μs, thus given a reading output frequency of 100 readings/s, this result is suitable for the most motion applications in particle accelerators and nuclear plants. The algorithm has been validated comparing fixed point results with results of a floating point implementation in LabView RT™

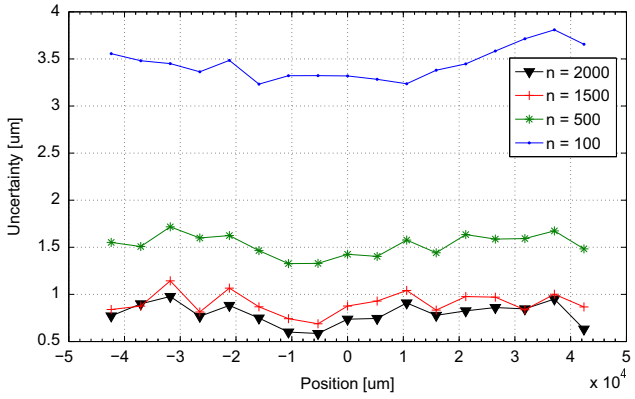

Fig. 5. Standard deviation σ_P of the final position P as a function of the number of ADC samples for SNR = 60 dB.

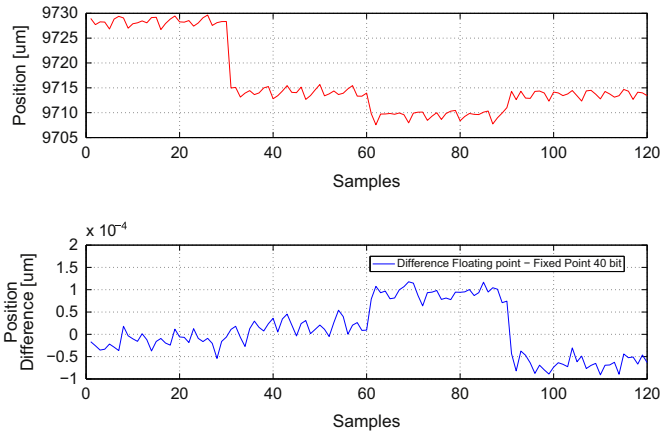

Fig. 6. Position $P \simeq 9.7$ mm (top) and difference between floating point and 40 bit resolution fixed point results (bottom).

running on a PXI system based on CPU Intel dual core 2.4 GHz and NI DAQ cards 6243. Several simulations have been run using the same input data for the two algorithms with different arithmetic representations, choosing positions over the whole sensor range. For instance Fig. 6 reports the position error calculated between the outputs of the floating point algorithm and the fixed point with 40 bit final output representation. The core position is set at $P \simeq 9.7$ mm and the position error is always below 2×10^{-4} μm [19].

5. Experimental results

5.1. Conditioning module reading uncertainty

The ADC and the DAC component have been characterized and the values of signal-to-noise and distortion ratio (SINAD) and total harmonic distortion (THD) have been evaluated [23,24]. The THD is measured in dB relative to the fundamental, such as distortion attenuation. The two ADC input channels connected to the LVDT secondaries have been fed with a sine wave generated by a Stanford Research Systems ™DS360 ultra low distortion signal generator, with frequency $f = 2.5$ kHz and amplitude $Vpp = 9.9$ V, using short BNC cables. This waveform generator has been used in all experimental tests to provide the input signals at a fixed frequency without connecting a sensor to the module. A value of SINAD = 90 dB, THD = −71 dB and an effective number of bits (ENOB) of 14 bits have been measured on both channels, the ADC sampling frequency has been set at $f_s = 250$ kS/s. The primary

Table 2
SINAD and THD of the DDS generated signals

Frequency (kHz)	SINAD (dB) No cable	THD (dB) No cable	SINAD (dB) 500 m cable	THD (dB) 500 m cable
1.000	75.98	−93.820	72.97	−85.1
1.125	78.45	−94.035	73.00	−84.6
1.250	84.22	−92.047	72.20	−84.4
1.375	79.91	−92.633	71.2	−82.9
1.500	66.04	−92.536	65.6	−81.7
1.625	65.34	−89.960	65.00	−81.5
1.750	79.76	−91.161	69.45	−80.6
1.875	83.54	−90.405	69.02	−80.3
2.000	78.05	−90.725	68.34	−79.4
2.125	77.54	−89.754	67.74	−78.7
2.250	73.42	−89.506	67.12	−79.0
2.375	79.88	−89.722	66.75	−78.1
2.500	83.10	−88.653	66.54	−77.3
2.625	79.43	−88.535	66.24	−76.9
2.750	79.76	−87.908	65.85	−76.6
2.875	75.41	−88.301	65.43	−76.3
3.000	67.02	−87.477	63.83	−76.8
3.125	70.87	−87.277	63.86	−75.4
3.250	60.36	−87.710	60.05	−74.9
3.375	80.17	−86.298	64.20	−75.4
3.500	79.91	−86.727	64.03	−75.0
3.625	80.68	−86.124	63.94	−74.5
3.750	82.14	−86.707	63.82	−73.9
3.875	75.50	−85.859	63.52	−73.6

signal, generated by the FPGA using DDS, has been measured with and without a 500 m long cable. Table 2 shows the values of THD and SINAD with and without the long cable for each available frequency. The lowest THD is $\simeq -85$ dB, while the lowest SINAD is $\simeq 60.36$ dB without the long cable. The values of the THD and SINAD at the end of the long cable are lower than the ones measured directly at the board output, the lowest THD is $\simeq -73.6$ dB and the lowest SINAD is 60.05 dB.

A dedicated software has been realized to interface the board and verify the module position uncertainty. Data requests are sent via a serial port to the module, which sends back r, V_A and V_B with 40 bit word lengths and the board and sensor temperature with 16 bit word lengths. A data request is sent every 20 ms. The module reading uncertainty has been evaluated by feeding a sinewave signal with $f = 1$ kHz and $Vpp = 8$ V to both the module secondary inputs. In all tests the core position P is calculated assuming $k = 100.0$ in (13). Results are shown in Fig. 7: since $V_A = V_B = 4$ V, the ratiometric value is close to 0. The uncertainty is calculated over each 30 position samples, therefore each 30×20 ms $= 0.6$ s. The test has been performed at constant room temperature, after 30 min from power up of the electronics, allowing the heating up of the pcb components. The position uncertainty was always below 100 nm.

5.2. Conditioning module sensitivity to temperature variations

The module reading is sensitive to the combined effect of temperature variations on the electronics and on the sensor. A full set of measurements has been performed to evaluate the module sensitivity to temperature and evaluate the position drift. The conditioning module has been placed alone inside a testbench oven, with the inputs connected to the external waveform generator and the output to the acquisition electronics setup. A signal with frequency $f = 1$ kHz and $Vpp = 8$ V is fed to both secondary inputs, while the temperature of the oven is programmed to follow a cycle. Fig. 8 shows the core position P, the oven temperature T as well as the position uncertainty σ_P vs time. The oven temperature is programmed to be initially 20 °C, then rising to 45 °C at a rate of $\simeq 0.16$ °C/min before returning to the initial

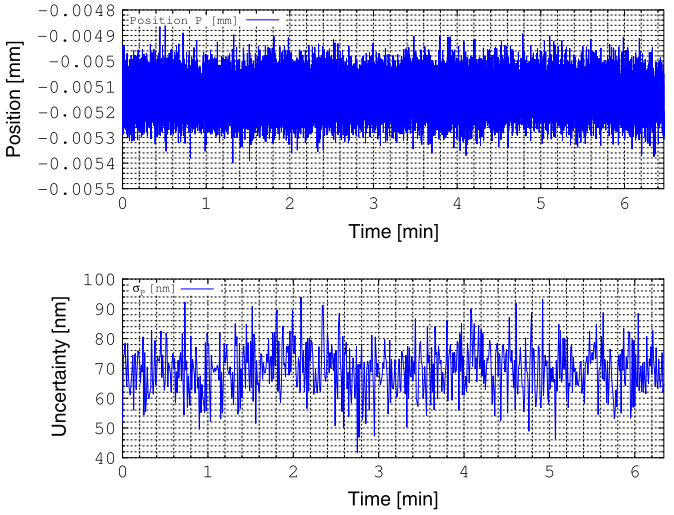

Fig. 7. Position P (top) and uncertainty σ_P (bottom) vs time. Input signal from the waveform generator has $f=1$ kHz and $Vpp=8$ V.

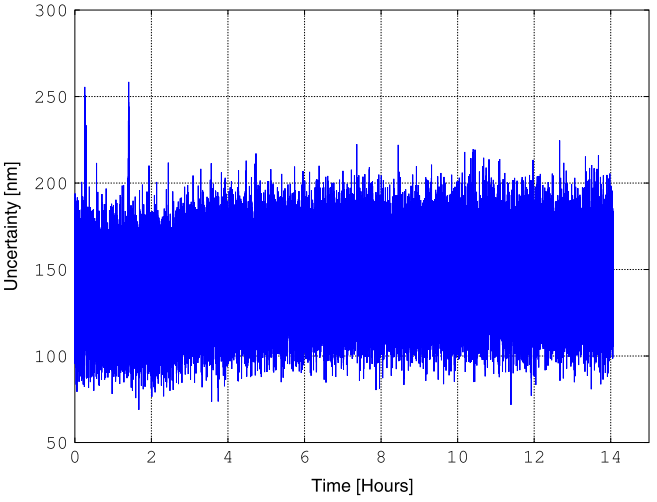

Fig. 9. Position uncertainty σ_P vs time with the LVDT connected to the conditioning module. The value of σ_P is always below 300 nm. Short cables used for the connections.

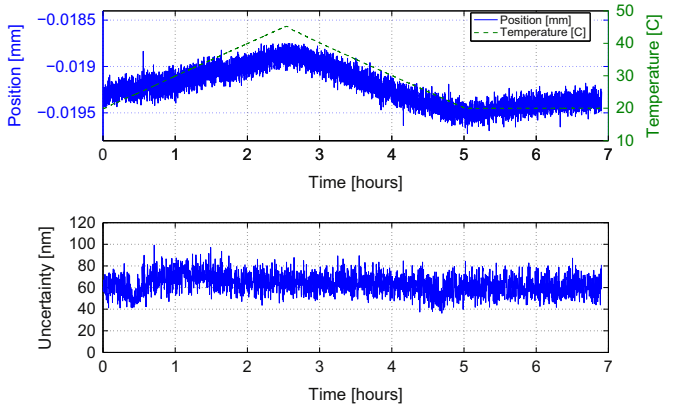

Fig. 8. Position P and temperature T vs time (top), position uncertainty σ_P vs time (bottom). The input of the secondaries is provided by a Stanford ultra low distortion waveform generator. The maximum position drift is $\simeq 48$ nm/°C. σ_P is calculated every 0.6 s (30 samples).

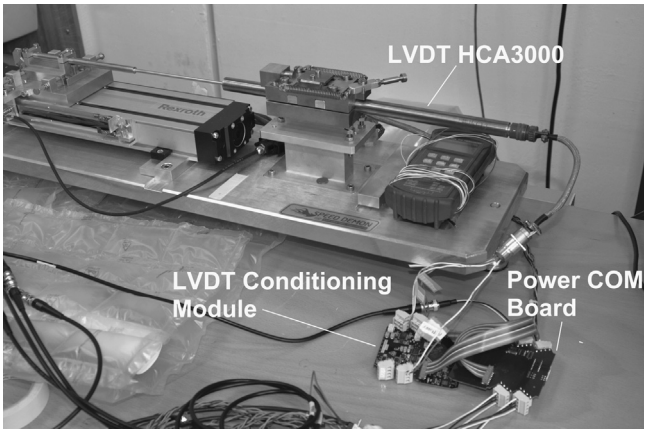

Fig. 10. Setup of experimental tests, the LVDT conditioning module is connected to an HCA3000 LVDT and to the Power-COM module. A stepper motor moves the inner core of the sensor.

temperature at the same rate. The core position experienced a drift of $\simeq 1.2$ μm over a temperature variation of 25 °C, which corresponds to a drift of $\simeq 48$ nm/°C. The position uncertainty was recorded every 0.6 s throughout the whole test and it was always below 100 nm.

5.3. Transducer reading uncertainty

A full characterization of the module performance has been carried out using a Schaevitz™ HCA3000 [25], an LVDT designed for applications in environments with high radiation levels. The position uncertainty σ_P has been monitored over 14 h with $P \simeq 36.5$ mm using a primary signal with $Vpp=9$ V, frequency $f=2.5$ kHz and short cables. Results are reported in Fig. 9. The value of σ_P has been found to be higher compared to the result in Fig. 7 and it was always below 300 nm. Similar results have been observed using a 500 m cable to connect the windings of the sensor to the conditioning module. During the whole measurement the room temperature has been monitored with a PT100 sensor, the value experienced a maximum variation of 1 °C. In conclusion the position uncertainty has been monitored in the same constant temperature conditions and with the same cable connections for both the cases, firstly with a signal generator used as an input and then with a real LVDT sensor connected. In the latter case the uncertainty was higher but it never went above a value of 300 nm.

5.4. Transducer non-linearity evaluation

The maximum non-linearity error of the transducer has been evaluated. The transducer has been connected to a testbench with a stepper motor programmed to move the inner core of the sensor, a Heidenhain™ linear optical encoder is used to have a precise measurement of the position step for the calibration of the transducer [26]. The setup with the LVDT conditioning module, Power-COM Board and the LVDT is shown in Fig. 10.

The transducer has a full stroke length of $\simeq \pm 80$ mm, a step of 2 mm is set and measured. A calibration test has been run over the half range of the transducer, -40 to 40 mm, first using the testbench to compute the core positions at each step and then using the module to return the value of P, to verify the agreement between the two results. The primary signal has $Vpp=9$ V and frequency $f=2.5$ kHz. The transducer non-linearity error has been calculated as the difference between the measured transducer characteristic and its best-fit straight line [1], divided by the half range value. Results are reported in Fig. 11: the maximum

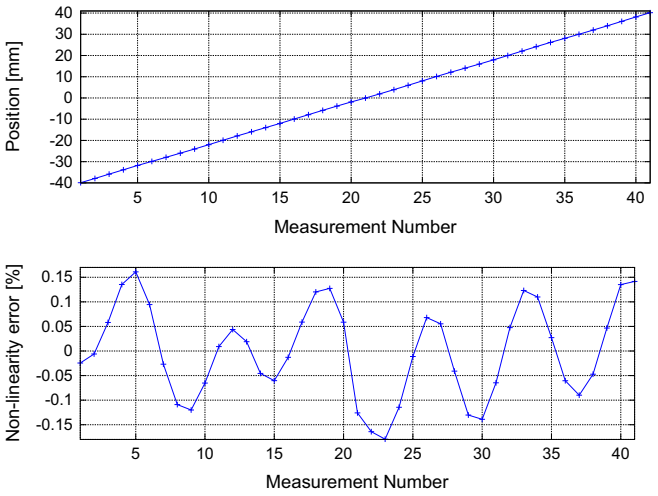

Fig. 11. Position P recorded at steps of 2 mm over the half range of the transducer using the conditioning module (top) and computed non-linearity error (bottom).

Table 3
Radiation tests results for each COTS component.

Device	Function	TID (Gy)
A3PE1500	FPGA	390
PCM1702	DAC	300
MAX11046	ADC	210
INA2128U	Instrumentation amplifier	500
OPA2227UK	Operational amplifier	220
OPA2134UA	Operational amplifier	500
LM7372	Dual operational amplifier	400
LM45CIM3	Precision temperature sensor	700
ADR434	Voltage reference	400
MAX3491	RS485 transceiver	500

non-linearity error of the tested transducer is 0.18% of the half range. This value has also been found using the testbench and it is in agreement with the value reported on the datasheet of the transducer [25].

5.5. Radiation tests results

Commercial Off-The-Shelf components are widely used for the development of instrumentation in high-radiation environments, although their behavior and tolerance to radiation needs to be carefully evaluated before using them in practical applications [27,28]. All the Integrated Circuits in the module have been separately tested to investigate the values of TID and fluence at which they start failing and showing errors related to radiation. Tests were performed at the Proton Irradiation Facility beamline of the Paul Scherrer Institute (PSI), using a proton beam with an Energy of 230 MeV and a dose rate $\simeq 10$ rad/s. The flash-based Actel A3PE1500 FPGA has been proven to be well suited to high-radiation environments [29,30], withstanding a dose up to 390 Gy with a fluence of 10^{13}pp/cm^2. The full sine-fit firmware has been loaded in the FPGA using Triple Modular Redundancy (TMR) to mitigate Single Event Effects (SEE), resulting in a 60% occupation of the FPGA resources. Table 3 reports the maximum values of TID for which each device worked within specifications without showing any SEEs or destructive events. Test results of the ADC, DAC and ADR434 are discussed below in further detail, more information on all radiation tests performed can be found online on the CERN radiation working group webpage [31–33,35–38].

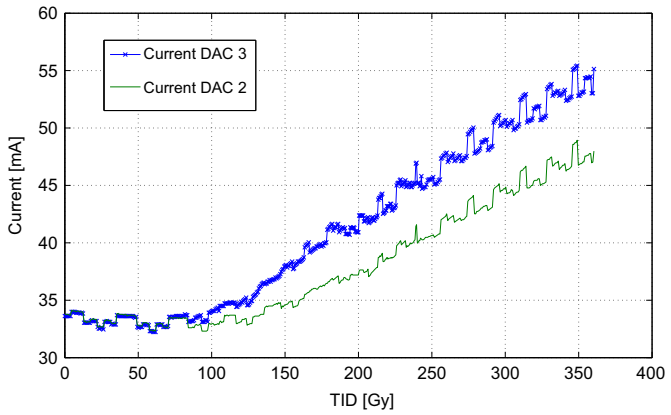

Fig. 12. Drift of the negative power supply current during PCM1702 radiation test. Curves of DAC labeled 2 and 3 are plotted.

5.5.1. PCM1702 radiation test results

The PCM1702 DAC has been tested [33,34] to verify the SEU and SEL cross-section as well as the degradation of the main parameters such as the current consumption. A total of six devices have been irradiated with a reference DAC left out of the beam during each irradiation. Each DAC is driven by the same code, hence all the outputs are the same and they are compared with the reference DAC. All the DACs tested still work at a maximum cumulated TID of 300 Gy and no single events were registered, although an increase in the current consumption appears starting from 100 Gy on the negative power supply. Fig. 12 shows a total current drift on each in-beam DAC of 11.3 mA.

5.5.2. MAX11046 radiation test results

The test of the MAX11046 [35] aimed at measuring the cross-section of the device, identifying the current consumption and measuring the voltage reference drift as a function of the TID. Three devices were tested under the same operating conditions. The test was performed feeding the ADC with a DC input voltage for each channel, the input range of the device is ± 5 V and the least significant bit is 150 μV. Measurements are divided into two parts, one is the calibration and the other the radiation test. In the calibration measurements the maximum and minimum values of the sampled input voltage are recorded for each channel, these values are used in the second phase of the radiation test as thresholds of a dead band, which is not considered for the SEU counting. If an ADC code falls out the threshold values during the irradiation, an SEU happened. The number of occurrences defines the SEUs and therefore the cross-section of the DUT by knowing the total fluence of protons provided by the facility. The values out of bound were close to the calibration range, this leads one to think that the out of range values is mostly due to variation of other parameters such as the voltage reference. The cross-section has been calculated for every channel and for each ADC tested, the cumulative cross-section including the three devices has been calculated as

$$\sigma_{cumulative} = \frac{N_{total}}{\phi_{total}} \tag{17}$$

where N_{total} is the total number of SEUs for all devices and all channels and ϕ_{total} is the total fluence cumulated by the ADCs under test. Table 4 shows the cross-section per device and per channel, together with the SEU counts and the total cumulative cross-section. Taking the cumulative cross-section as a reference it is possible to evaluate the cross-section per channel and per device, 9.5×10^{-12} cm^2 and 7.6×10^{-11} cm^2 respectively. No destructive failures were observed. Latch up events and SET were not observed up to a proton fluence 3.9×10^{11} pp/cm^2 cumulated

Table 4
Cross-section and SEU count—radiation tests MAX11046.

Channel	σ (cm^2) MAX11046_1	σ (cm^2) MAX11046_2	σ (cm^2) MAX11046_3	SEU count
Ch 0	1.52×10^{-11}	6.06×10^{-11}	1.65×10^{-11}	36
Ch 1	1.27×10^{-11}	4.04×10^{-11}	2.75×10^{-11}	31
Ch 2	1.27×10^{-11}	2.53×10^{-11}	6.06×10^{-11}	37
Ch 3	2.53×10^{-11}	2.78×10^{-11}	6.89×10^{-11}	37
Ch 4	3.04×10^{-11}	2.27×10^{-11}	1.93×10^{-11}	28
Ch 5	4.05×10^{-11}	3.54×10^{-11}	2.20×10^{-11}	31
Ch 6	3.04×10^{-11}	2.27×10^{-11}	1.65×10^{-11}	27
Ch 7	1.01×10^{-11}	4.80×10^{-11}	4.13×10^{-11}	38
Cumulative	2.3×10^{-10}			265

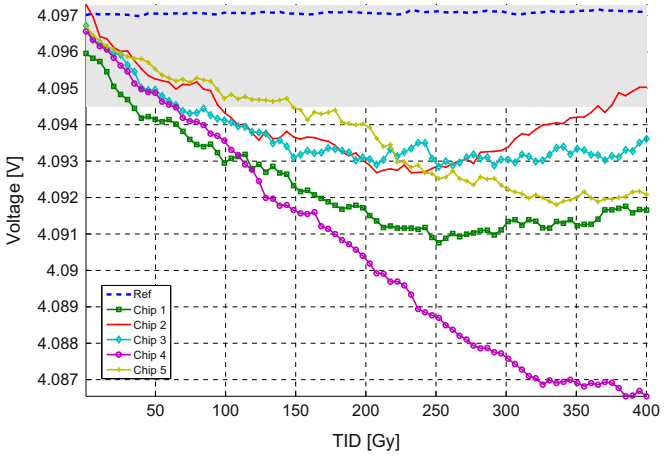

Fig. 13. The output voltage of the ADR434. Chip 6 was the reference device; Chip 4 shows the highest decrease of around -10 mV. The grey area illustrated the tolerance range according to the datasheet (± 1.5 mV with respect to V_{out}=4.096 V).

on each device. This result indicates that the ADC reaches its end-life at TID of about 210 Gy. The voltage reference had a drift between 1.8 mV and 3.2 mV, though given the small value it is hard to correlate this to a radiation effect.

5.5.3. ADR434 radiation test results

The ADR434 Voltage Reference is characterized by an ultra-low noise, low current supply and good thermal hysteresis performance. Its output voltage drift is specified to remain in a stable range of ± 1.5 mV ($\pm 0.004\%$) with respect to its initial value of 4.096 V. Five devices were tested with one kept out of the beam as a reference. The measurement [38] focused on the output voltage drift ΔV_{out} and the evaluation of Single Event Transients. Results showed that the output does not remain within the specified range of the nominal output 4.096 V, a continuous decrease of the output voltage of all irradiated devices has been observed, Fig. 13. All in-beam devices went out of specification at TIDs between 33 and 147 Gy, with the maximum achieved output drift of -0.25% after 400 Gy. The device can however operate up to 400 Gy in applications where a precision of $\pm 0.3\%$ on the output signal is acceptable. This result is within the specifications for the LVDT conditioning module and it is a good alternative to bipolar [36] and buried Zener [37,39] voltage references.

5.5.4. LVDT conditioning module radiation test results

After characterizing the tolerance of each device to radiations, a test has been performed on the whole conditioning module board

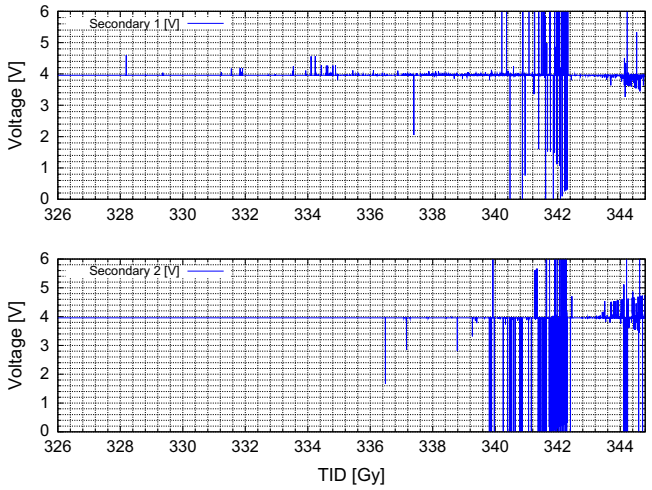

Fig. 14. Secondary 1 (top) and Secondary 2 (bottom) during irradiation of the FPGA. The fitted values are $\simeq 4$ V. The first event shows up at $\simeq 328$ Gy.

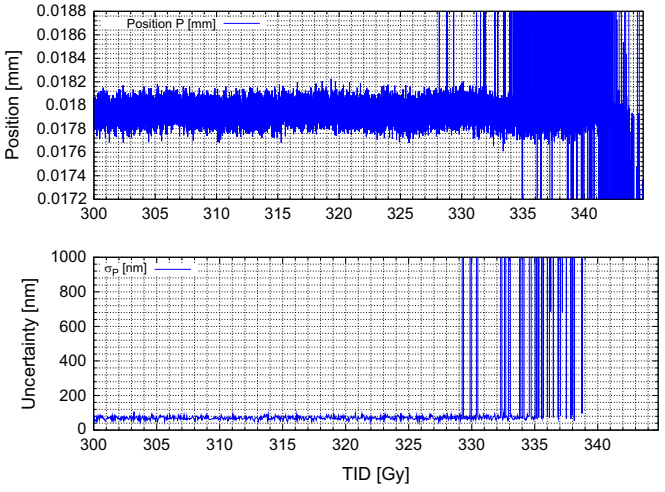

Fig. 15. Position P (top) and uncertainty σ_P (bottom) calculated during irradiation of the FPGA. $\overline{P} = 0.0179$ mm and $\sigma_P \simeq 100$ nm up to $\simeq 328$ Gy, when the first error shows up. After $\simeq 338$ Gy σ_P is always above 1 μm.

focusing the beam only on the FPGA. This test aimed at verifying the robustness of the firmware and its sensitivity to radiation. A waveform generator provides a sinusoidal signal with amplitude $Vpp = 8$ V and frequency 1 kHz to the secondary inputs, resulting in a computed average position value $\overline{P} = 0.0179$ mm, with uncertainty $\sigma_P \simeq 100$ nm. The primary signal has been monitored to detect possible SEE, while the flux has been set to $\simeq 1.41 \times 10^8$ p/cm^2 s. Fig. 14 shows the fitted amplitude of the two secondaries as returned by the module under irradiation between 326 and 346 Gy. Several spikes show up on both signals starting at $\simeq 328$ Gy, first with smaller amplitudes and then progressively increasing. The position P and sigma σ_P follow the same pattern, with P falling off by several micrometers and σ_P rapidly going significantly above 300 nm, as reported in Fig. 15.

These errors can be related to SEUs occurring on the sine-fit coefficients stored in the SRAM blocks. Since 2000 samples are acquired by the ADC, the size of matrix $\mathbf{D}^{\dagger}$ is (2×2000), thus 2000 coefficients are stored in the SRAM. The time to write 2000 addresses is 3.2 ms, if a bit flip occurs in a memory cell that has already been written, an error might occur in the sine-fit algorithm, leading to a false reading of the secondary amplitude value. The values for the Direct Digital Synthesis are also stored in the SRAM and constantly rewritten, although 256 values per sinewave

period are used and only 64 values are stored in the memory, since a sinewave signal can be generated using only a quarter of a period together with its properties of symmetry. Thus the time to write the 64 memory addresses used for the DDS is $\simeq 157$ μs, resulting in a lower bit flip probability compared to the sine-fit coefficients refreshing. This might explain why the primary signal generation never showed any failure effect up to 370 Gy, very close to the limit of the FPGA, while the secondary signals experienced several errors at a lower dose level, albeit the relation between the TID and the SEU event probability on the irradiated FPGA SRAM blocks has not been investigated and it will be the object of future studies. In addition it has been noticed that the FPGA at 213 Gy could not be reprogrammed, meaning that the device was already starting to reach the end of its life. In conclusion each component used in the design of the LVDT conditioning module has been separately tested using a proton beam of 230 MeV and radiation effects related to the level of TID have been analyzed. The module showed correct output results up to 318 Gy and the primary signal never failed up to 370 Gy. Given these results the maximum allowable TID and fluence that guarantee the proper functioning of the module are the ones imposed by the ADC: TID = 200 Gy and fluence 3.9×10^{11} pp/cm^2.

6. Conclusions and outlooks

A high precision radiation tolerant LVDT conditioning module has been developed using standard Commercial Off-The-Shelf components. The reading of the sensor output voltages is based on a ratiometric technique combined with a three parameter sine-fit algorithm that is digitally implemented on an FPGA. The module ensures a few micrometers of reading accuracy with an uncertainty below 1 μm, allowing operation with long cables between the sensor and the conditioning electronics which is not available in standard commercial LVDT conditioning modules. The module is interfaced via UART using the MODBUS over serial line protocol. A full metrological characterization of the board has been performed using an HCA3000 LVDT sensor. The position uncertainty σ_P with the LVDT core at the end of the stroke has always been below 300 nm. The module sensitivity to temperature has been evaluated, results showed a position drift $\simeq 48$ nm/°C over 25 °C of temperature variation. Radiation tests have been carried out at the Proton Irradiation Facility of the Paul Scherrer Institute using a proton beam with 230 MeV energy. The LVDT conditioning module maximum allowed TID and fluence have been found to be 210 Gy and 3.9×10^{11} pp/cm^2 respectively. Future improvements will focus on increasing the THD and SINAD values of the primary signal and decreasing the board sensitivity to temperature variations.

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