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SPADs for Vertex Tracker Detectors in Future Colliders

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Physics aims at the future linear colliders impose such stringent requirements on detector systems that exceed those met by any previous technology. Amongst other novel technologies, SPADs (Single Photon Avalanche Diodes) detectors are being developed to track high energy particles at ILC (International Linear Collider) and CLIC (Compact LInear Collider). These sensors offer outstanding qualities, such as an extraordinary high sensitivity, ultra-fast response time and virtually infinite gain, in addition to compatibility with standard CMOS technologies. As a result, SPAD detectors enable the direct conversion of a single particle event onto a CMOS digital signal in the sub-nanosecond time scale, which leads to the possibility of single BX (bunch crossing) resolution at some particle colliders. However, SPAD detectors suffer from two main problems, namely the noise pulses generated by the sensor and the low fill-factor. The noise pulses worsen the detector occupancy, while the low fill-factor reduces the detection efficiency.

This work presents the development of an SPAD pixel detector in standard CMOS technologies as a proof of concept of such devices aimed at the vertex and tracker regions of the future linear colliders. To comply with the specifications imposed by ILC and CLIC, solutions to minimize the intrinsic noise pulses and increase the fill-factor are provided.

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1. Introduction

This work presents the development of an SPAD (Single Photon Avalanche Diode) pixel detector in standard CMOS technologies aimed at the vertex and tracker regions of the future linear colliders, namely ILC (International Linear Collider) [1] and CLIC (Compact LInear Collider) [2]. In spite of all the advantages that characterize this technology [3], such as an extraordinary high sensitivity, ultra-fast response time and virtually infinite gain, SPAD detectors suffer from two main problems. On the one side, there exist noise phenomena inherent to the sensor, which induce fake pulses that cannot be distinguished from real events and also worsen the detector occupancy to unacceptable levels. On the other side, the fill-factor is low, which results in a reduced detection efficiency. Solutions to these two problems that are compliant with the severe specifications of the next generation of particle colliders have been thoroughly investigated.

2. ILC and CLIC detector concepts

The concepts for a multi-purpose detector to be built at ILC and CLIC are addressed in two different proposals, the validated SiD (Silicon Detector) [4] and ILD (International Large Detector) [5]. Both proposals also deal about the highly demanding requirements imposed by the physics goals at the future linear colliders, which drive the design of the detector. Special care must be paid to the single point resolution, material budget, granularity, time resolution, occupancy, radiation tolerance, power consumption, EMI (ElectroMagnetic Interference) immunity and cost of the detector.

The requirements for excellent single point resolution and minimum material budget, motivated by the need for an accurate particle track reconstruction, limit the pixel size and detector thickness per layer to 17 μm and 0.15-0.30% X_0 (150-300 μm), respectively. Moreover, since no active cooling is allowed inside the acceptance region, the cooling system must rely on forced cold air. A high granularity is required for good particle separation.

The time resolution and the radiation tolerance are dictated by the running conditions at the collider. In particular, the time resolution depends on the beam time structure and the required occupancy. The occupancy, which is mainly generated by beam-induced background hits and varies with the distance of the detector to the interaction point, is set at 1%. At ILC, a new train with 2820 BXs (bunch crossings) that are 308 ns apart will be started every 199 ms [6]. These parameters are much more ambitious at CLIC, where trains with 312 BXs that are separated by only 0.5 ns will take place every 20 ms. Regarding the background hits, at ILC they range from 6.320 hits/cm^2/BX to 0.046 hits/cm^2/BX between the first layer of the VTX (Vertex Detector) and the second layer of the FTD (Forward Tracker Detector) at a nominal energy of 500 GeV [6]. The second layer of the FTD is the last one where silicon pixels are expected. In contrast, backgrounds between 10^{-1} hits/cm^2/BX to 10^{-3} hits/cm^2/BX are foreseen at CLIC [2]. To comply with the demanded occupancy, if the detector is not fast enough to be read out after each BX, time slicing or time stamping techniques can be performed to read out the detector multiple times in one train or divide the bunch train into as many time-buckets as BXs.

The required radiation tolerance follows entirely from the beam-induced backgrounds. A maximum TID (Total Ionizing Dose) of up to 1 kGy/year and a neutron fluence or NIEL (Non-Ionizing Energy Loss) of approximately 10^{11} n_{eq}/cm^2/year is expected near the ILC beam pipe [6]. In contrast, the TID and NIEL for CLIC are 200 Gy/year and 10^{10} n_{eq}/cm^2/year, respectively. These data include some safety margin.

Finally, the power consumption should be low enough to minimize the material budget of the cooling system inside the detector sensitive volume. An affordable cost should be considered as well, since large-area detectors are foreseen.

3. The occupancy issue

In SPAD detectors, the output pulses are due not only to absorbed radiation but also to dark counts, afterpulses and crosstalks, which characterize the noise performance of the sensor. The typical noise rate of CMOS SPADs ranges between 1 and 100 Hz/μm^2, although this value can be dramatically increased to 50 kHz/μm^2 in those technologies that face the presence of the STI (Shallow Trench Isolation) [7]. Solutions commonly adopted to reduce the noise pulses regard the utilization of dedicated technologies with lower doping profiles, active quenching and cooling. However, dedicated technologies are highly priced, whereas active quenching circuits tend to increase the area occupation. Another possibility consists in switching off those pixels with an intrinsic noise well above the average value of the array, at the expenses of the consequent loss of fill-factor. Nevertheless, in those applications where the expected signal arrival time can be known in advance, as it is the case of HEP (High Energy Physics) experiments, the sensor can be operated in the time-gated mode [8]. In this regime of operation, the SPAD is periodically activated and deactivated under the command of a trigger signal to reduce the probability to detect the noise pulses that interfere with radiation triggered events. In this work, the time-gated operation has been chosen as an effective solution to reduce the occupancy of the detector. Further improved results are obtained with the reduction of the working temperature. The design and characterization of an SPAD pixel array operated in the conditions commented is described next.

3.1 Design of an SPAD array in a HV-CMOS process

A prototype SPAD detector has been designed and fabricated in the HV-AMS (High-Voltage AustriaMicroSystems) 0.35 μm standard CMOS technology. CMOS technologies offer the possibility to integrate on the same chip the sensor and the readout electronics, which results in a better dynamic response. Moreover, standard technologies ensure a reasonable cost. The particular HV-AMS 0.35 μm technology was chosen for the good trade-off between noise and fill-factor that it provides. Regarding the architecture, the detector consists of an array of SPAD pixels that are arranged in 10 rows per 43 columns. It has a total sensitive area of approximately 1 mm^2, which was set to increase the probability to observe events during the beam-test of the detector. Each pixel includes one SPAD sensor and one monolithically integrated readout circuit. The junction of the photodiodes is implemented by means of a p^+ diffusion in a deep n-tub. The junction is surrounded by a low doped p-tub implantation to avoid the premature edge

breakdown. Each photodiode has a sensitive area of 20 μm (width) x 100 μm (height). This geometry was chosen so as to satisfy the requirement on the single point resolution. The sensor width of 20 μm is more or less compliant with the demanded size of 17 μm, while the radial direction is relaxed to a sensor height of 100 μm to keep the local confusion small. The readout circuits are placed on top of each pixel, between two consecutive rows of sensors. With the purpose of maximizing the fill-factor of the array, all the SPADs within a row share a common deep n-tub, generating a macro-pixel of 43 SPADs. Nevertheless, the introduction of the p-tub implantation generates a minimum separation between two neighboring SPADs of 1.7 μm (width). The detector features an optical fill-factor of 67%. Although this value is superior to the usual SPAD fill-factors, it must be further incremented.

Each readout circuit is composed of 2 MOS switches to activate and deactivate the SPAD detector according to the time-gated operation, one voltage discriminator to sense the avalanches, a 1-bit memory cell to store the information generated by the SPAD during the gated-on periods and one pass-gate to extract the content of the pixel during the gated-off periods. The detector is read out sequentially by rows, although each pixel can be read out in 1.65 ns. Because the prototype SPAD detector is a proof of concept of such sensors for HEP experiments, neither techniques to mitigate the radiation effects nor on-chip data processing are included at the moment. A micrograph and the schematic diagram of one SPAD pixel are shown in Fig. 1. More information about the detector design, of both the sensor and the readout electronics, is available in [7].

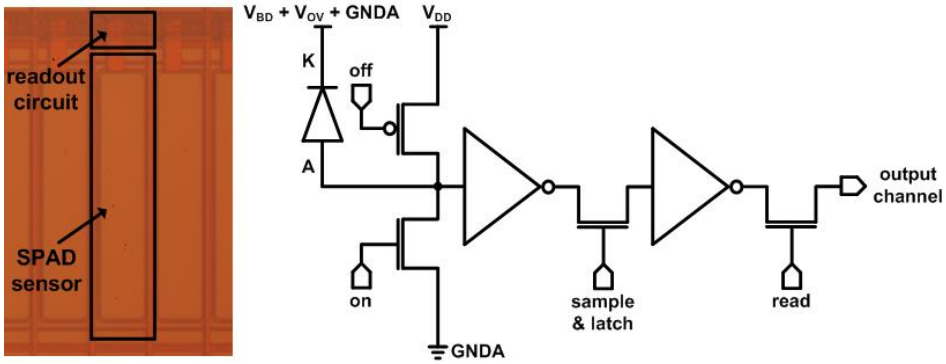

Figure 1: Micrograph (left) and schematic diagram (right) of one digital SPAD pixel.

3.2 Characterization

The prototype SPAD detector is mounted on a PCB and connected to a development board (terasIC DE0-Nano with an ALTERA Cyclone IV FPGA), which is used to generate the control signals to operate the detector in the time-gated mode, count off-chip the avalanches generated during a certain integration time and manage the communication with a PC via a USB. The PC runs a dedicated software developed in C++ that allows to select the duration of the gated-on (t_{obs}) and gated-off (t_{off}) periods, as well as the number of times (n_{rep}) that the sequence $t_{obs}+t_{off}$ is repeated. The integration time is given by the product of the gated-on period and the number of repetitions ($t_{obs} \cdot n_{rep}$). The PC also displays in real time the number of counts generated by the detector after the integration time.

The noise rate of the SPAD detector in darkness was characterized first at room temperature. The measurement of the NCR (Noise Count Rate), i.e. the detector noise including dark counts, afterpulses and crosstalks, as a function of the gated-off period revealed that it is possible to suppress the presence of afterpulses by using long gated-off periods starting at 200 ns. This result is independent of V_{OV}, the reverse overvoltage used to bias the detector above its V_{BD} or breakdown voltage. The DCR (Dark Count Rate), i.e. the detector noise without afterpulses, presents a mean value across all the pixels of the array of 67 kHz at 1 V and 139 kHz at 2 V of overvoltage. Although the DCR is high, the probability per pixel to produce one dark count during one repetition of the measurement or frame can be lessened by using short gated-on periods. Thus, the DCP (Dark Count Probability), the name given to this phenomenon, is set at 10^{-4} dark counts per frame with a gated-on period of 10 ns (1 V of V_{OV}). It can be further decreased to 10^{-5} dark counts per frame with a gated-on period of 1 ns. The experimental characterization also demonstrated that the SPAD detector is free of optical crosstalks effects. Nevertheless, as a consequence of having several SPADs in the same deep n-tub, the electrical crosstalk is nonzero. Minority charge carriers generated during an avalanche, and diffusing in the deep n-tub, can reach a neighboring SPAD and eventually trigger a new avalanche ascribable to electrical crosstalk. The electrical crosstalk was characterized by studying the noise pulse coincidences generated in neighboring pixels during the same gated-on period. It was found out that the electrical crosstalk presents a maximum probability of 2.6% with gated-on periods of 7 ns or longer. However, this probability can be reduced to almost zero by using short gated-on periods around 3-4 ns, as a result of deactivating the detector before the minority charges can reach a neighboring SPAD.

The reduction of the detector noise, and thus of the occupancy, by means of the time-gated operation results in an improved detector performance. Good proof of this is the extension of the DR (Dynamic Range) from 9.21 to 12.84 bits when the gated-on period is shortened from 1274 to 14 ns (being the gated-off period longer than 200 ns in both cases), which allows to sense weaker light intensities. In another experiment, the imaging capabilities of the SPAD detector to reproduce a model image were tested. The model image was illuminated by means of a pulsed light source with an active window of 22 ns within the gated-on period. The images were generated by the SPAD detector after the repetition of 10^7 frames. The experiment showed not only that blinding pixels can be avoided with short gated-on periods, but also that the contrast of the generated images is enhanced as the gated-on period is decreased. This phenomena is explained by the lower number of noise pulses that mask the reproduction of the model image with short gated-on periods. The images generated with two different gated-on periods can be seen in Fig. 2.

The thermal effects on the NCR and the DCR were studied in a climatic chamber in the temperature range of -20 ºC to 60 ºC, also in darkness. The NCR was obtained by operating the detector in continuous mode or free running, while in the case of the DCR a gated-off period longer than 200 ns was used. At 1 V of V_{OV}, the mean NCR ranges from 132 kHz at -20 ºC to 630 kHz at 60 ºC. A noticeable increase is observed at 2 V, where the mean NCR ranges from 636 kHz to 1.66 MHz between the same temperatures. Nevertheless, the suppression of the afterpulses with a long enough gated-off period allows to achieve more acceptable noise rates. Thus, at 1 V of V_{OV}, the mean DCR ranges from 9.8 kHz at -20 ºC to 350 kHz at 60 ºC. At 2 V,

these figures are increased to 23.9 kHz and 819 kHz, respectively. A comparison between the mean NCR and the mean DCR throughout all the measured temperature range is plotted in Fig. 2. It can be observed that the NCR shows a weak dependence on the temperature, especially below 0 ºC. The change in the slope of the NCR at 0 ºC suggests that thermally generated carriers are the main contributors to the NCR at high temperatures, while afterpulses dominate at low temperatures. In contrast, the DCR presents a reduction by a factor of approximately 2 every 10 ºC, which matches well with theory. In free running, 1 noise pulse will be generated every 7 µs at 1 V and -20 ºC. In contrast, if the detector is operated in the time-gated mode with an active period of 10 ns, the DCP will be 10^{-5} dark counts per frame under the same bias and temperature. Alternatively, with an active period of 1 ns, the DCP will be 10^{-6} dark counts per frame. The difference in the DCP measured at -20 ºC and 60 ºC is 2 orders of magnitude. This behavior enforces the utilization of the time-gated operation with long enough gated-off periods and gated-on periods in the nanosecond time scale, as well as low working temperatures.

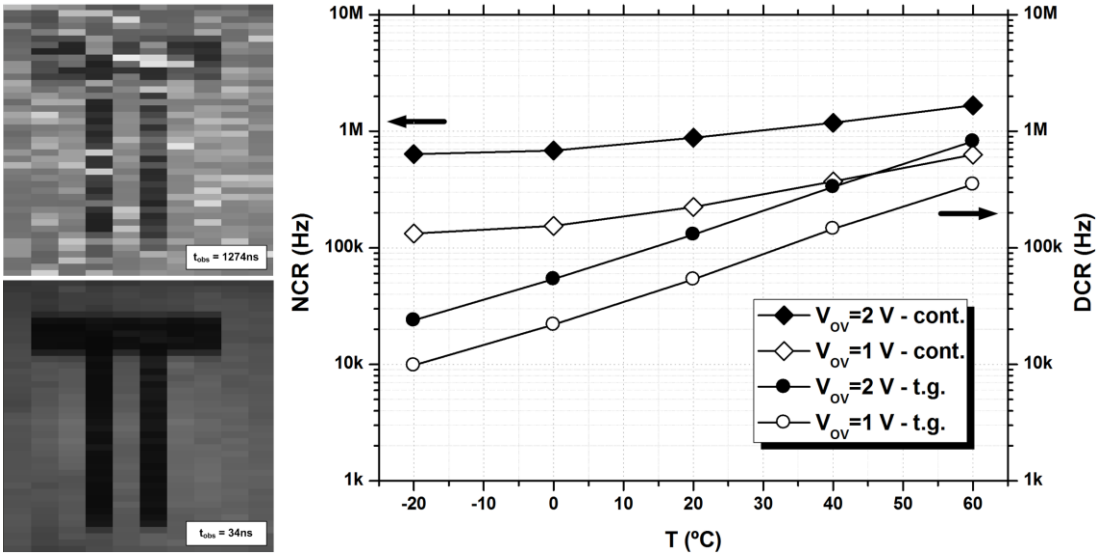

Figure 2: Image of a model at two different t_{obs} (left). NCR (in continuous mode) and DCR (in time-gated mode) as a function of the temperature at 1 V and 2 V of V_{OV} (right).

SPAD detectors are inherently susceptible to radiation damage. The predominant effects of the radiation expected at ILC and CLIC (e^+e^- pairs, photons and neutrons) are the increase of the sensor noise and the misfunction of the readout electronics. An SPAD detector array with radiation tolerant readout circuits and fabricated in the HV-AMS 0.35 µm standard CMOS technology has been irradiated with γ rays, as reported in [9]. According to to this reference, the DCR is increased by a factor 3-4 with a γ ray irradiation dose of 10 kGy, which is the dose expected at ILC after 10 years of operation. Thus, the DCR of 9.8 kHz, measured at 1 V and -20 ºC, would be risen to 36.45 kHz at the end of the ILC lifespan. At CLIC, in contrast, a softer radiation dose of 2 kGy is foreseen after 10 years of operation. In this case, the sensor noise would be risen by a factor 2. Although the prototype SPAD detector described in this article was not irradiated, an irradiation campaign should be performed to have first hand results.

The power consumption of the SPAD detector at 1 V of V_{OV} is measured to be 130 mW, which is higher than the maximum value accepted at the future linear colliders. Nevertheless, the power consumption is mostly due to the output pads that extract the information generated by the sensors and not due to the readout circuits. The dissipation of the sensors is measured to be null. This issue could be solved by using an LVDS (Low-Voltage Differential Signaling) pad, which would ensure large arrays with reasonable dissipations.

Finally, the suitability of the prototype SPAD detector for high energetic particle detection was tested in a series of beam-tests conducted at the SPS (Super Proton Synchrotron) area of CERN (European Organization for Nuclear Research). The set-up used in the beam-tests, together with the results obtained, is shown in Fig. 3. A complete description of the set-up can be found in [10]. During the beam-tests, the SPAD detector was operated with a short gated-on period of 30 ns and a low overvoltage of 1.2 V. The results obtained show a correlation between the SPAD detector and the telescope used for the calibration, which suggests that the SPAD technology can sense MIPs (Minimum Ionizing Particle). However, due to technical problems during the experiment, it was not possible to obtain high statistics or measure the detection efficiency. Further beam-tests are planned, but they are outside the scope of this work.

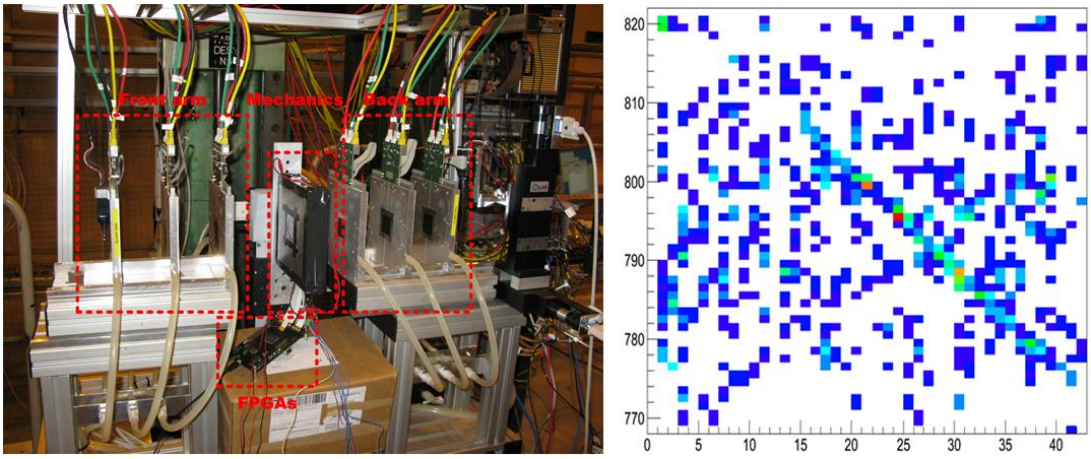

Figure 3: Set-up used at the CERN beam-test (left). Correlation between the SPAD detector array and the telescope used for the calibration (right) [11]. The axes indicate the position of the pixels.

4. The fill-factor issue

Amongst other severe specifications, a 100% fill-factor is demanded by future linear colliders on detector systems. In the particular case of SPAD detectors, the presence of non-sensitive areas due to the guard ring to prevent the premature edge breakdown and the monolithically integrated readout circuit to improve the detector response induce low fill-factors which rarely exceed the 10%. Additionally, in those technologies that are below the 0.25 μm feature, the masks that the designers introduce in the layout to block the STI, and thus avoid a dramatic increase of the DCR, worsen the situation. In this work, 3D technologies are explored as a solution to overcome the fill-factor limitation of standard SPADs.

4.1 Design of an SPAD array in a 3D process

A prototype SPAD detector has been designed in a 130 nm standard CMOS process fabricated by Global Foundries and vertically integrated by Tezzaron. The 3D SPAD detector is composed of a two-layer stack of logic dies, which are bonded together in a face-to-face orientation. The connection for relaying signals between tiers is made through Metal 6, the highest metal of the technology. Moreover, via-first TSVs (Through-Silicon-Vias) are used for connection between the logic circuitry and the I/O bond pads, which are placed on the back of the top tier. Because TSVs are also used to control the thinning of the dies after the fabrication, it is necessary to maintain a minimum TSV density throughout both tiers. This forces the utilization of dummy TSVs at a recommended pitch of 100 µm. The total thickness of the two-layer logic stack is typically 765 µm.

The 3D SPAD detector consists of an array of 48 rows per 48 columns of pixels. The junction of the photodiodes is implemented by means of a p^+ diffusion in an n-well, which is also surrounded by a low-doped p-well guard ring to avoid the premature edge breakdown. Nevertheless, the Global Foundries 130 nm technology features the presence of the STI. To avoid contact between this layer and the multiplication region of the SPAD, and thus obtain an acceptable DCR, a polysilicon gate is drawn around the p^+ diffusion. The introduction of the p-well guard ring, together with the polysilicon gate for an STI-free SPAD, generates a minimum separation between two neighboring SPADs of 2.24 µm. The readout circuits, which are monolithically integrated with the sensors, allow to operate the detector in a time-gated mode. The detector is sequentially read out by rows during the gated-off periods. Further details concerning the design of the detector can be found in [12].

Prior to the final layout of the 3D SPAD detector, several array architectures were considered. It was concluded that the maximum fill-factor is achieved when the sensitive areas of one tier are used to overlap the non-sensitive areas of the other tier, and vice versa. Amongst all the proposed architectures, two of them were selected for implementation. Thus, the 3D SPAD detector is composed of two sub-arrays of 48 rows per 24 columns each. The first approach implements 18 µm x 18 µm sensors on one tier and the readout electronics on the other one, which allows to achieve a 66% fill-factor. In contrast, the second scheme relies on clusters of four pixels, in which two sensor areas of 18 µm x 18 µm and 30 µm x 30 µm are used to maximize the overlap between tiers. Three 18 µm x 18 µm sensors together with the readout electronics of the four sensors are placed on one tier, whereas the 30 µm x 30 µm SPADs are placed strategically on the other tier to overlap the readout electronics and most of the non-sensitive areas of the 18 µm x 18 µm sensors. This approach generates a 92% fill-factor. The first structure was chosen for its simplicity and the second one because it provides the maximum fill-factor with the lowest risks. The architectures of the 3D SPAD detector are shown in Fig. 4. Although the design of the detector is finished, it has not been submitted for fabrication due to the continuous delays in the MPW (Multi-Project Wafer) runs of the Global Foundries 130 nm/Tezzaron 3D process. Nevertheless, the 3D SPAD detector demonstrates that the low fill-factor typical of SPAD technologies can be increased up to values close to 100%, as demanded by future linear colliders on detector systems.

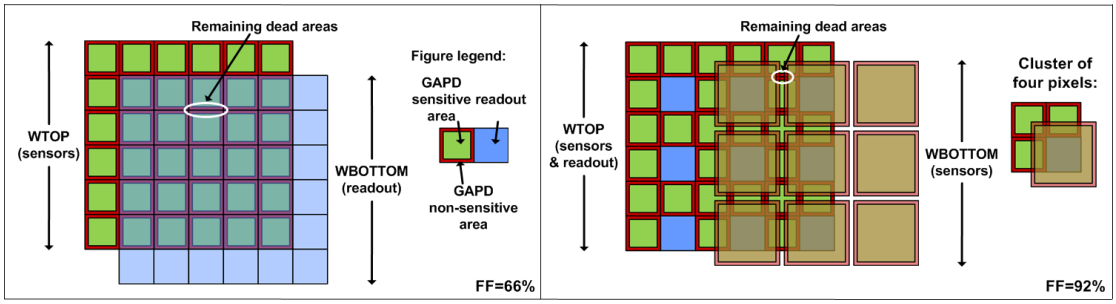

Figure 5: Schematic diagram of the two array architectures implemented in the 3D SPAD detector. The sensors and the readout electronics are not to scale.

5. Discussion

The suitability of any sensor technology for particle tracking at future linear colliders is given by the capability to fulfill the highly demanding requirements of ILC and CLIC. However, the prototype SPAD detectors presented here are proof of concepts and therefore they are not optimized for performance. Next, the extent of fulfillment of the mentioned requirements by the SPAD technology is reviewed.

Regarding the timing resolution, SPAD detectors are the only sensor technology proposed so far that can be read out after each BX at some future linear colliders. Although SPAD sensors are characterized by rise times of a few hundred picoseconds, the timing resolution of the detector is also determined by the readout electronics. In the case of the SPAD detector in the HV-AMS technology, the pixels can be read out in 1.65 ns. Thus, the present detector could be used at ILC as it is, but the prototype is not suited for CLIC. A possible solution would go through the utilization of time stamping techniques.

In order not to affect the pattern recognition, the occupancy of the detector including the beam-induced background hits must be below 1%. Moreover, in the case of SPAD technologies, the noise counts intrinsically generated by the sensor must also be taken into account, since they can be even higher than the background hits. Nevertheless, the experimental characterization of the 10 x 43 SPAD array has shown that the DCP can be deeply reduced by means of the time-gated operation, combined with low reverse overvoltages and low working temperatures. Thus, on the one side, the expected backgrounds at ILC range from $1.264 \cdot 10^{-4}$ hits/SPAD/BX to $9.2 \cdot 10^{-7}$ hits/SPAD/BX between the first layer of the VTX and the second layer of the FTD, provided that an SPAD size of 20 µm x 100 µm is used. The measured DCP of the detector is 10^{-6} noise counts/SPAD/BX, with a t_{off} of 336 ns, t_{obs} of 1 ns, V_{OV} of 1 V and temperature of -20 ºC. Because at the future linear colliders the expected event rate will be below the level of backgrounds, it seems reasonable to compare the background hits and the noise counts to study in first approximation the feasibility of the detector. According to this, the appropriate performance of the SPAD technology is ensured at the second layer of the FTD, where the background hits and the noise counts present approximately the same value. However, this is not true for the first layer of the VTX, where the expected background hits are too high. To solve this issue, the logic AND between the output values of two overlapped pixels from two different layers could be done. On the other side, the short inter-BX spacing of 0.5 ns planned

for CLIC is too short to allow for the readout of the detector. Nevertheless, the detector can still be operated in the time-gated mode, with a long gated-off period equal to the inter-train period (20 ms) and a short gated-on period equal to the BX train length (156 ns). Considering that the detector is read out during the inter-train period, the expected background hits range between $6.2 \cdot 10^{-4}$ hits/SPAD/train and $6.2 \cdot 10^{-6}$ hits/SPAD/train. Under the same timing conditions, a V_{OV} of 1 V and temperature of -20 ºC, the DCP is $1.53 \cdot 10^{-3}$ noise counts/SPAD/train. Therefore, the SPAD detector at present time is unfitted for CLIC, yet the logic AND between two layers could be done to improve this situation. A summary of the extent of fulfillment by SPADs of this and all the other requirements demanded by ILC and CLIC is presented in Table 1.

Category	Required	Achieved by SPADs	Improvement
Pixel size	17 µm	20 µm	–
Material budget	0.15% X_0 (ILD) 0.30% X_0 (SiD)	0.25% X_0	–
Granularity	High	20 µm x 100 µm	–
Timing	Single BX resolution	Single BX resolution (ILC) Time integration (CLIC)	– Time stamping (CLIC)
Occupancy	< 1%	$9.2 \cdot 10^{-7}$ bh/SPAD/BX, 10^{-6} nc/SPAD/BX (ILC) $6.2 \cdot 10^{-6}$ bh/SPAD/train, $1.53 \cdot 10^{-3}$ nc/SPAD/train (CLIC)	– 2 input logic AND
Radiation tolerance	1 kGy/year, 10^{11} n_{eq}/cm^2/year (ILC) 200 Gy/year, 10^{10} n_{eq}/cm^2/year (CLIC)	$9.2 \cdot 10^{-7}$ bh/SPAD/BX, $4 \cdot 10^{-6}$ nc/SPAD/BX (ILC) $6.2 \cdot 10^{-6}$ bh/SPAD/train, $3.06 \cdot 10^{-3}$ nc/SPAD/train (CLIC)	– 2 input logic AND
Power	< a few mW/cm^2	High	LVDS pad
Fill-factor	100%	67%	3D technologies (to ≈100%)
EMI	Immunity	Yes	–
Cost	Affordable	Yes	–

Table 1: Summary of the extent of fulfillment by SPADs of the requirements demanded by ILC and CLIC. The numerical results presented refer to the SPAD detector in the HV-AMS technology.

6. Conclusion

The development of a tracker detector capable to meet all the specifications demanded by ILC and CLIC is a defiant field. In the case of SPAD detectors, the two most ambitious aspects make reference to the occupancy and the fill-factor. Despite the single BX resolution of SPADs, the high frequency of the pattern noise generated by the sensor increases the occupancy to unacceptable values. In an attempt to minimize this problem, the operation of the detector in the

time-gated mode, at low reverse overvoltages and low temperatures has been proved as an effective solution. 3D technologies appear to be a solution to address the requirement on the 100% fill-factor. Nevertheless, although the performance of the prototypes developed is encouraging, further studies concerning radiation effects and the sensor efficiency in the detection of high energy particles are needed.

7. Acknowledgement

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