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# The Shunt-LDO regulator to power the upgraded ATLAS pixel detector

Gonella, L (UBONN) *et al*

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## The shunt-LDO regulator to power the upgraded ATLAS pixel detector

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**L. Gonella,<sup>1</sup> M. Barbero, F. Hügging, H. Krüger and N. Wermes**

*Physikalisches Institut, Universität Bonn,  
Nussallee 12, D-53115 Bonn, Germany*

*E-mail:* [gonella@physik.uni-bonn.de](mailto:gonella@physik.uni-bonn.de)

**ABSTRACT:** The shunt-LDO regulator is a new regulator concept which combines a shunt and a Low Drop-Out (LDO) regulator. Designed as an improved shunt regulator to match the needs of serially powered detector systems, it can also be used as a pure LDO regulator for general application in powering schemes requiring linear regulation. The flexibility of the design makes the shunt-LDO regulator a good candidate for use in the powering schemes envisaged for the upgrades of the ATLAS pixel detector. Two shunt-LDO regulators integrated in the prototype of the next ATLAS pixel front-end chip, the FE-I4A, are used to demonstrate the feasibility of the proposed powering solutions.

**KEYWORDS:** Voltage distributions; Particle tracking detectors

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<sup>1</sup>Corresponding author.

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## Contents

<b>1</b>	<b>Introduction</b>	<b>1</b>
<b>2</b>	<b>The shunt-LDO regulator</b>	<b>1</b>
<b>3</b>	<b>Shunt-LDO characterization</b>	<b>2</b>
3.1	Shunt mode	3
3.2	LDO mode	5
3.3	Partial shunt mode	5
<b>4</b>	<b>FE-I4A performance vs. powering mode</b>	<b>7</b>
4.1	IBL powering scheme	8
<b>5</b>	<b>Conclusions</b>	<b>8</b>

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## 1 Introduction

Different powering schemes are investigated for the upgrades of the ATLAS pixel detector to provide high efficiency with a low material burden. In particular, for the first upgrade, the Insertable B-Layer (IBL) project [1], a direct powering scheme with on-chip linear regulators will be implemented, whilst for future upgrades (Phase-1 [2] and High Luminosity (HL-)LHC), DC-DC conversion and serial powering [3] are under investigation.

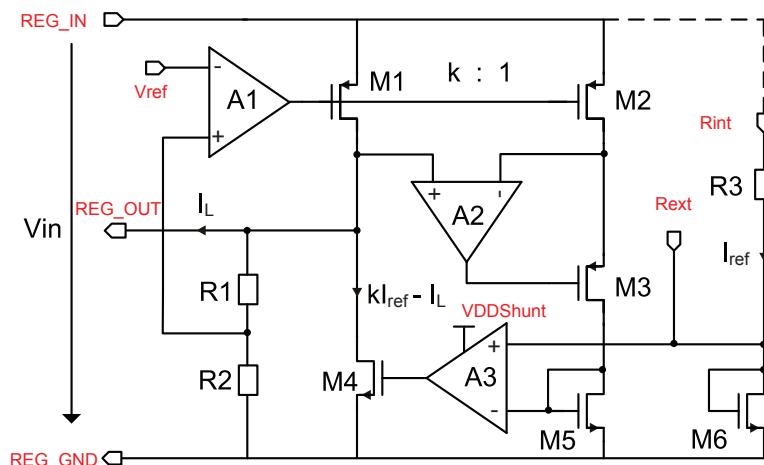
To evaluate the different powering options, the first full scale prototype of the next generation pixel Front-End (FE) chip, FE-I4A [4], integrates one switched capacitor DC-DC converter [5] and two shunt-LDO regulators. The latter offer a versatile design that can meet the needs of powering schemes requiring either linear or shunt regulation. The shunt-LDO regulator will thus be used for the IBL upgrade, and is as well the regulator proposed for a serially powered pixel detector upgrade.

This paper describes the characterization of the shunt-LDO regulator in FE-I4A and compares the chip performance when powered with and without the regulator.

## 2 The shunt-LDO regulator

The shunt-LDO regulator (figure 1) is a combination of a Low-Dropout (LDO) regulator and a shunt regulator, and it is thus composed of two regulation loops. The voltage regulation loop is enforced by the LDO regulator formed by the error amplifier A1, the PMOS power transistor M1, and the resistive divider formed by R1 and R2. It is responsible for generating a constant output voltage equal to twice the reference voltage ( $V_{\text{out}} = 2V_{\text{ref}}$ ).

The current regulation loop is enforced by the shunt transistor M4, the current mirror M2 (the amplifier A2 and the cascode M3 are added to improve the mirroring accuracy), and the differential



**Figure 1.** Simplified schematics of the shunt-LDO regulator in FE-I4A.

**Table 1.** Working modes of the shunt-LDO regulator.

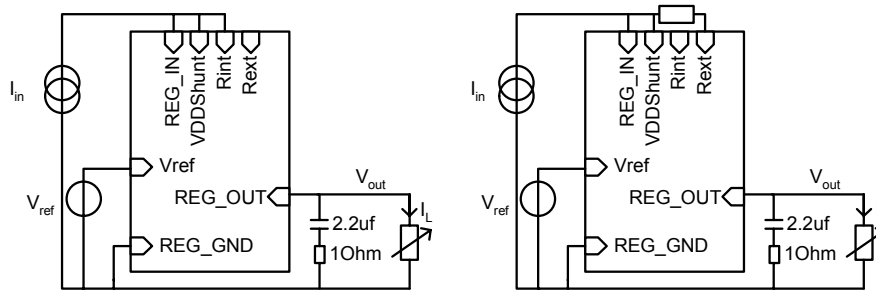
	Shunt mode	LDO mode	Partial shunt mode
I regulation loop	enabled	disabled	enabled
REG_IN	I	V	V

amplifier A3. It can be enabled in combination with the voltage regulation loop to either keep the current through the regulator constant, independently of the load, or to set a minimum current under which the current flowing through the regulator cannot drop. These features can be selected by setting the appropriate value of the shunt current via the reference resistor R3. In this way, different working modes can be selected, as summarized in table 1. In particular, the device can be configured in shunt mode for application in serially powered systems (current based), or in LDO and partial shunt mode for use in conventional voltage based supply schemes. The three working modes are illustrated in sections 3.1, 3.2, and 3.3, together with the results of the characterization. A complete description of the shunt-LDO working principle can be found in [6].

The shunt-LDO regulator in FE-I4A can withstand spikes at the input up to 2.5V, as every branch of the design is cascoded. The nominal operating input voltage is 1.6V. The input current can be as high as 600mA. The generated output voltage is in a range of 1.2–1.5V. The reference resistor R3, used to define the shunt current, can either be internal (Rint), with a fixed value of 2k $\Omega$  in FE-I4A, or be placed externally (Rext) to choose a different value. The regulator version in FE-I4A requires the voltage reference  $V_{ref}$  to be provided externally.

### 3 Shunt-LDO characterization

The shunt-LDO regulators in FE-I4A have been first characterized without connection to the core of the chip. An external load was used in the measurements (figure 2, 5, and 7) to mimic the typical



**Figure 2.** Connection of the shunt-LDO regulator in shunt mode with internal (left) or external (right) reference resistor.

FE-I4A power consumption (analog and digital supplies of resp. 1.5V and 1.2V, analog and digital current of resp. 350–380mA and 140–180mA). The two regulators were characterized in all three working modes both stand-alone, and in parallel, i.e. sharing input and ground connection.

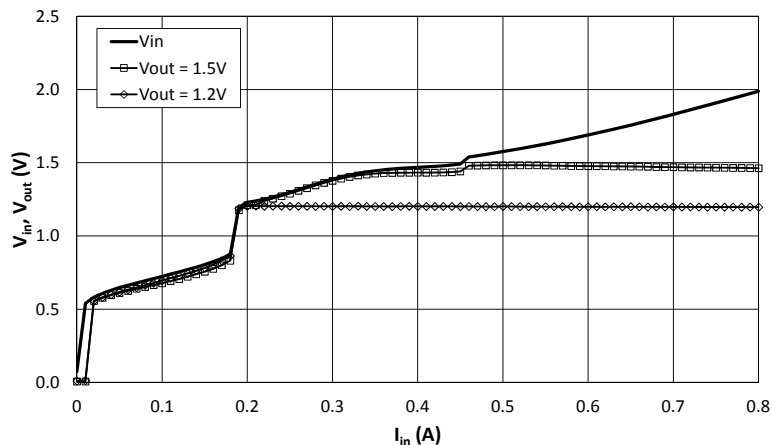
### 3.1 Shunt mode

The shunt mode is the dedicated serial powering mode. In this configuration, the current regulation loop is enabled ( $VDDShunt = REG\_IN$ ) and the shunt-LDO regulator is supplied by a constant input current  $I_{in}$  (figure 2). The current regulation loop is configured in order to keep  $I_{in}$  constant, independently of changes of the load current  $I_L$ . Variations of  $I_L$  are compensated by shunting different amounts of current.

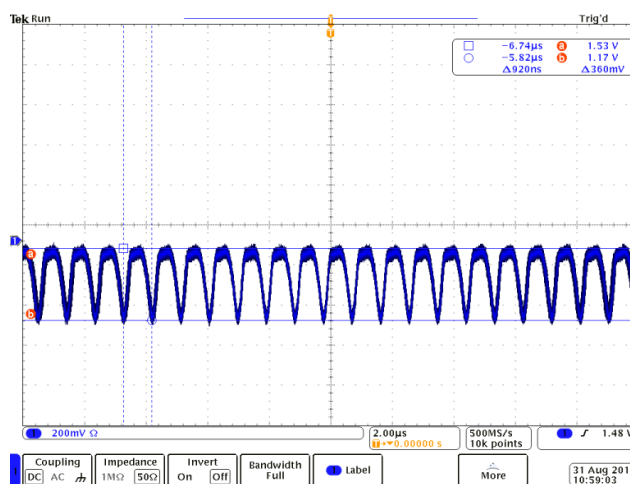
To perform this operation, a fraction of the input current flowing in transistor M1 is mirrored in M2 and drained into M5. A reference current  $I_{ref}$  that depends on the input potential  $V_{in}$  is defined by the reference resistor R3.  $I_{ref}$  is then compared to the fraction of current flowing through transistor M1 by use of the differential amplifier A3. If the current drained to transistor M5 is smaller than the reference current, the shunt transistor M4 is steered to draw more current and vice versa. In this way, the current that is not drawn by the load is shunted through the transistor M4, where  $I_{shunt} = kI_{ref} - I_L$ . The value of  $I_{shunt}$  is set in order to be able to shunt a current up to  $I_{in}$ . The minimum required  $I_{shunt}$  for regulator operation is of 5mA.

Figure 3 shows the voltage generation as a function of the input current for the two shunt-LDO regulators connected in parallel, generating  $V_{out} = 1.2V$  and  $1.5V$ . Starting from  $I_{in} = 460mA$ , both outputs are regulated. The slope of the  $V_{in} - I_{in}$  characteristics is defined by the reference resistor. R3 is here chosen in order to have a  $V_{in} = 1.6V$  for a  $I_{in} = 600mA$ , where 400mA flow in the regulator generating  $V_{out} = 1.5V$ , and 200mA in the regulator generating  $V_{out} = 1.2V$ .

Before regulation is achieved, unexpected oscillations are observed, starting at  $I_{in} = 190mA$ . Figure 4 shows the measured oscillations for a  $I_{in}$  of 280mA, with an amplitude of 360mV and a frequency of about 1MHz. Once regulation is achieved, the regulator can be operated in a stable way. However, the effect of the oscillations is to move the regulation point at higher  $I_{in}$ . This can indeed decrease the power efficiency of the device if the required input current for stable operation is much higher than the load current. The cause of these oscillations has been identified in the compensation of the current loop. This behavior is in fact not observed in LDO mode where



**Figure 3.** Voltage generation as a function of  $I_{in}$  for two shunt-LDO regulators connected in parallel.

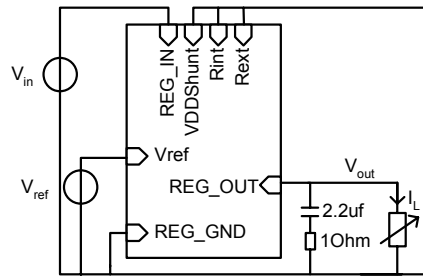


**Figure 4.** Oscillation at the output of the regulator for an input current of 280mA ( $V_{out} = 1.5V$ ).

the current regulation loop is disabled. The compensation scheme will be improved in the next submission run for serial powering applications.

The load regulation ( $\Delta V_{out}/\Delta I_L$ ) is about  $150m\Omega$ . This result is in disagreement with the simulated value, which is approx.  $30m\Omega$ . The discrepancy is being investigated with further simulations and measurements.

For a single regulator in shunt mode, two sources of inefficiency have to be considered: the  $V_{dropout}$  of the LDO and the  $I_{shunt}$ . Choosing the proper value of  $R3$  allows to achieve a  $V_{dropout}$  of  $100mV$  and an  $I_{shunt}$  of  $5mA$ . In this way efficiencies as high as  $90\%$  can be reached. For two devices connected in parallel generating different output voltages, a third source of inefficiency has to be considered, which is the  $\Delta V$  between the two output voltages. For  $\Delta V = 300mV$  and over the typical FE-I4A current range, the power efficiency is between  $68\%$  and  $77\%$  with  $V_{in} = 1.6V$  at  $I_{in} = 600mA$ .



**Figure 5.** Connection of the shunt-LDO regulator in LDO mode.

**Table 2.** Minimum  $V_{\text{dropout}}$  as a function of  $V_{\text{out}}$  and  $I_L$ .

	$I_L = 200\text{mA}$	$I_L = 600\text{mA}$
$V_{\text{out}} = 1.2\text{V}$	150mV	270mV
$V_{\text{out}} = 1.5\text{V}$	50mV	150mV

### 3.2 LDO mode

In LDO mode, the current regulation loop is disabled ( $V_{\text{DDShunt}} = \text{REG\_GND}$ ) and the regulator works as a standard Low-Dropout regulator (figure 5).

The minimum  $V_{\text{dropout}}$  required for regulation is shown in table 2 as a function of  $V_{\text{out}}$  and  $I_L$ . The measured values are higher than the design value (100mV), especially for  $V_{\text{out}} = 1.2\text{V}$  at  $I_L > 200\text{mA}$ . This is however not a concern for the specific application in FE-I4A as the digital current is below 200mA. In addition to this, the regulators share the same input to power the FE-I4A (figure 9). A  $V_{\text{in}}$  of about 1.7V has to be used to provide enough  $V_{\text{dropout}}$  for the regulator generating  $V_{\text{out}} = 1.5\text{V}$ . Thus, the regulator generating  $V_{\text{out}} = 1.2\text{V}$  sees a  $V_{\text{dropout}}$  of 400–500mV.

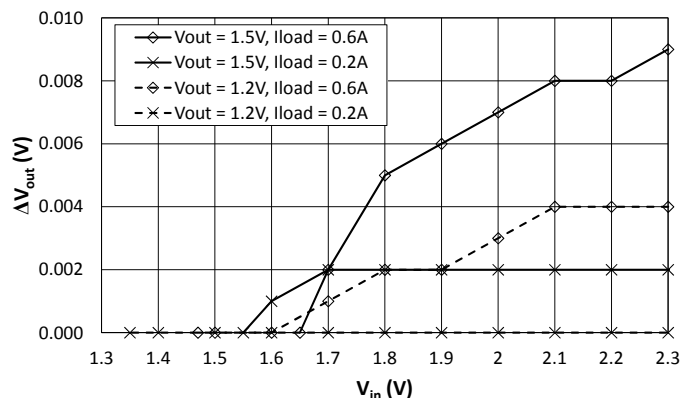
After regulation  $V_{\text{out}}$  is stable. The line regulation ( $\Delta V_{\text{out}}/\Delta V_{\text{in}}$ ) is shown in figure 6. The maximum  $\Delta V_{\text{out}}$  is of only 9mV over a  $V_{\text{in}}$  range from 1.65V to 2.3V. Also in this mode a load regulation of 150mΩ has been measured for  $I_L$  up to 600mA. The quiescent current, i.e. the difference between input and load current, is of 1mA.

The power efficiency for single device operation is between 75% and 95%, at minimum  $V_{\text{dropout}}$  and over the entire current range. When connected in parallel for  $V_{\text{in}} = 1.7\text{V}$ , with  $I_L = 180\text{mA}$  for  $V_{\text{out}} = 1.2\text{V}$  and  $I_L = 380\text{mA}$  for  $V_{\text{out}} = 1.5\text{V}$ , the power efficiency is 79%.

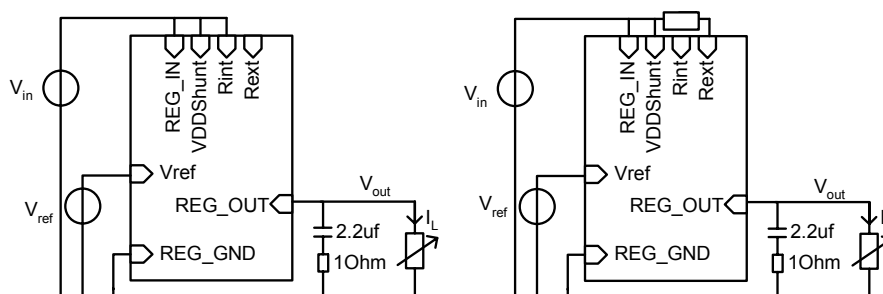
### 3.3 Partial shunt mode

In partial shunt mode, the regulator is operated as in LDO mode, but with enabled current regulation loop (figure 7). In this working mode the  $I_{\text{shunt}}$  is set in order to prevent the input current from falling under a preset value  $I_{\text{min}}$  higher than the minimum  $I_L$ . Thus  $I_{\text{in}} = I_{\text{min}}$  for  $I_L \leq I_{\text{min}}$ , and  $I_{\text{in}} = I_L$  for  $I_L > I_{\text{min}}$ . This configuration can be used to reduce transients in voltage based powering schemes where the load current is not constant.





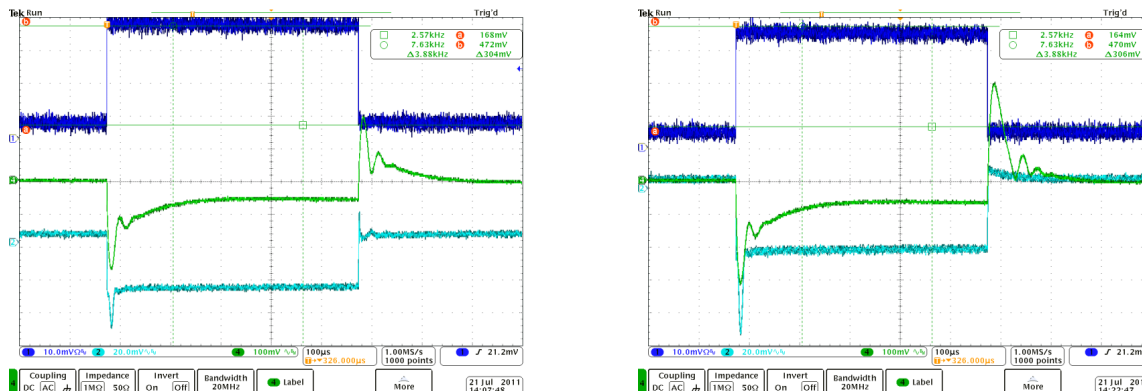
**Figure 6.** Line regulation in LDO mode.



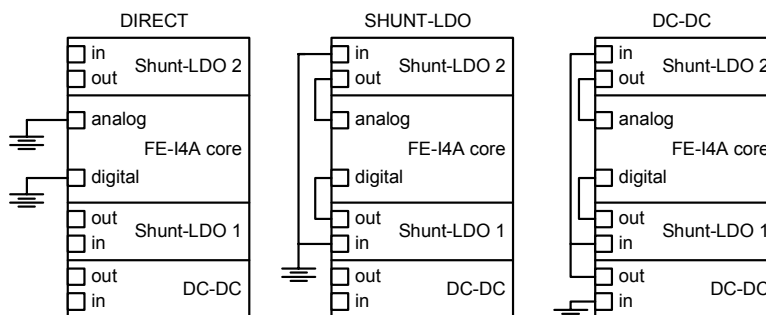
**Figure 7.** Connection of the shunt-LDO regulator in partial shunt mode with internal (left) or external (right) reference resistor.

To demonstrate this operation mode, the two shunt-LDO regulators are connected in parallel with  $V_{in} = 1.8V$ , and operated in partial shunt mode and LDO mode. The minimum current in partial shunt mode is set to 130mA for the regulator generating  $V_{out} = 1.5V$ , and 80mA for the regulator generating  $V_{out} = 1.2V$ . A load current pulse from 40mA to 340mA is applied externally to the regulator generating a  $V_{out} = 1.5V$ . When in LDO mode, the regulator sees the entire current transient, whilst in partial shunt mode this transient is reduced to 210mA because the  $I_{in}$  cannot be lower than 130mA. As shown in figure 8, the transients are lower in partial shunt mode. This is particularly evident at the input of the regulator, where transients of 200mV are observed in partial shunt mode, and up to 300mV in LDO mode. The transients at the output of the regulator are mostly due to the fact that  $V_{in}$  falls under the minimum required  $V_{dropout}$ , thus the output is no longer regulated and follows the input voltage. Increasing the  $V_{in}$ , reduces the transients on the  $V_{out}$ . The amplitude of the transients observed at the output is of max. 20mV in partial shunt mode, whilst it reaches 50mV in LDO mode.

The performance of the regulator in this mode is the same as in LDO mode for  $I_L > I_{min}$ . For smaller  $I_L$ , a certain inefficiency is added, which depends on the difference between  $I_{min}$  and the minimum  $I_L$ .



**Figure 8.** Transients in partial shunt mode (left) and LDO mode (right). Top: current pulse at the regulator output measured across a  $100\text{m}\Omega$  resistor; scale  $10\text{mV}/\text{div}$ . Middle: transient at the regulator input; scale  $100\text{mV}/\text{div}$ . Bottom: transient at the regulator output; scale  $20\text{mV}/\text{div}$ .



**Figure 9.** FE-I4A powering options (ground connection not shown).

#### 4 FE-I4A performance vs. powering mode

The FE-I4A chip integrates multiple powering options, none of which is hard wired inside the chip. Different powering schemes can be selected by means of external wire bonds. The analog and digital voltages can be provided on the respective pads either directly, using the shunt-LDO regulators or the DC-DC converter, as illustrated in figure 9. To power the FE-I4A, the shunt-LDO regulators are operated in parallel. The shunt-LDO regulators are used also to power the chip with the DC-DC converter. In this case they are operated in LDO mode to generate the required analog and digital voltages out of the converter output.

The performance of the FE-I4A chip in terms of noise was compared for different powering schemes. The FE-I4A was operated with the regulators in all three modes, and for reference with a standard direct powering mode. The chip could be powered and configured without problems using the regulator. Results of threshold scans performed with the chip powered using the shunt-LDO in the three different modes show no significant noise increase with respect to the direct powering mode (table 3).

**Table 3.** Comparison of FE-I4A performance in different powering modes.

	Direct	Shunt mode	LDO mode	Partial shunt mode
Threshold (e)	4611	4470	4489	4475
Threshold dispersion (e)	652.1	570.6	619.1	614.7
Noise (e)	150.2	159.6	155.2	156
Noise dispersion (e)	16.01	13.13	16.67	16.01

**Table 4.** Comparison of FE-I4A performance in different powering modes using a dedicated test-up for the IBL upgrade.

	Direct	LDO mode	Partial shunt mode
Threshold (e)	4824	4426	4429
Threshold dispersion (e)	650.1	613	613.5
Noise (e)	155.6	154	155.2
Noise dispersion (e)	17.08	16.43	16.8

#### 4.1 IBL powering scheme

For the IBL powering scheme, direct powering with on-chip linear regulators is chosen. The shunt-LDO will here be used either in LDO or partial shunt mode. A dedicated test setup was prepared to test this powering scheme, including voltage regulators (so called PP2 regulators) and power cables used in the experiment. The PP2 regulator was used to provide the input voltage to the shunt-LDO regulator. Also in this case, the noise figures were compared to assess the performance of the powering chain. The compatibility of the two regulators was demonstrated. As shown in table 4, the chip performance stays unchanged when power is provided via the shunt-LDO regulator.

## 5 Conclusions

A shunt-LDO regulator is proposed as the power regulation element for the upgrades of the ATLAS pixel detector. The design of the regulator allows to use it in powering schemes requiring either linear or shunt regulation. Three working modes can in fact be selected to fit the needs of different powering schemes: shunt mode, LDO mode, and partial shunt mode.

The first regulator version dedicated to power the next generation ATLAS pixel FE chip was integrated in the FE-I4A. The performance of the regulator stand-alone are satisfactory, although a few problems need to be solved in future submissions to achieve better performance, especially in terms of efficiency. In all working modes, the output resistance of the regulator has to be decreased. In shunt mode, the compensation of the current regulation loop has to be modified to achieve stability over the entire range of input current. In combination with FE-I4A, the regulator has shown good performance in all modes. No noise increase was observed with respect to the direct powering configuration. The first application of the shunt-LDO regulator will be the IBL project, where the regulator will be used in either partial shunt mode or LDO mode.

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