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SEU tolerant memory design for the ATLAS pixel readout chip

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ABSTRACT: The FE-I4 chip for the B-layer upgrade is designed in a 130 nm CMOS process. For this design, configuration memories are based on the DICE latches where layout considerations are followed to improve the tolerance to SEU. Tests have shown that DICE latches for which layout approaches are adopted are 30 times more tolerant to SEU than the standard DICE latches. To prepare for the new pixel readout chip planned for the future upgrades, a prototype chip containing 512 pixels has been designed in a 65 nm CMOS process and a new approach is adopted for SEU tolerant latches. Results in terms of SEU and TID tolerance are presented.

KEYWORDS: Radiation-hard electronics; Front-end electronics for detector readout; Analogue electronic circuits; Radiation damage to electronic components

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1 Introduction

The Insertable B-Layer (IBL) will be installed in the ATLAS experiment during the LHC shutdown in 2013–14 [1, 2]. The FE-I4 chip has been developed with a pixel size of $250 \times 50\,\mu m^2$ in a 130 nm feature size bulk CMOS process to respect IBL requirements in terms of radiation tolerance and the occupancy.

Local and global memories are implemented to retain respectively the local pixel configuration and the global chip configuration. SEU tolerant memories were used to allow reliable operation at high beam intensities and to avoid reloading frequently the configuration data.

For the second upgrade expected around 2018, the FE-I4 chip will still be compatible with the outer pixel layers of the tracker requirements. However for the inner detector, pixel granularity has to be improved in order to keep the performances. In fact, better granularity reduces the occupancy and thus improves the tracking resolution.

Highly scaled CMOS process (65 nm) is now explored and tested for the pixel front end intended for the future inner pixel layers development. A first prototype chip has already been designed where a new architecture of configuration memories based on triple redundancy and error correction was implemented and the SEU tolerance was evaluated.

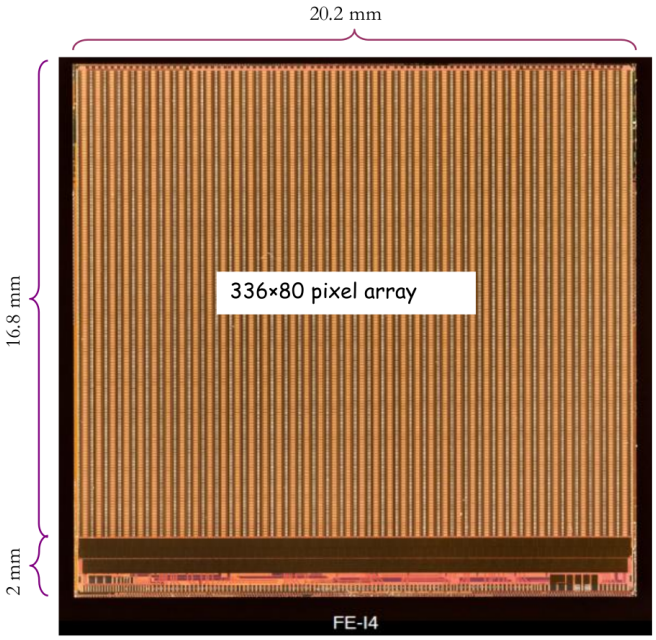

Figure 1. Picture of the FE-I4 chip.

In section 2, we describe the pixel configuration memories implemented in the FE-I4 chip where layout aspects are considered, especially spatial separation of critical nodes, isolation techniques like isolated wells, guard rings and cell interleaving. We describe the global configuration memory where particular attention has been paid to the control logic associated to each block of the configuration latches and where a relatively complex scheme is adopted to prevent some transient glitches to be propagated to the latches. Finally, we will give SEU results obtained with a 24 GeV protons beam.

In section 3, we describe the chip prototype designed to explore and to test the 65 nm CMOS process considered now as one of the best candidate for the future upgrades. In this design, the pixel configuration memories are based on the triple redundancy of standard latches with additional logic for error correction. Irradiation tests are currently being conducted and initial results show that the triple redundancy reduces hugely the number of errors and the details of these measurements will be presented and discussed.

2 The present design for the insertion of B-layer

2.1 FE-I4 chip overview

Figure 1 shows a photograph of the FE-I4 integrated circuit designed for the IBL [3]. It contains 26 880 hybrid pixels arranged in 80 columns with 250 μm pitch by 336 rows with 50 μm pitch. The FE-I4 chip is designed in a 130 nm CMOS process which shows an increased radiation tolerance with respect to previous larger feature size processes. Following a few guidelines where minimal size transistors are avoided and guard rings for analog and sensitive digital circuitry are implemented, a radiation-hardness of more than 200 MRad is achievable.

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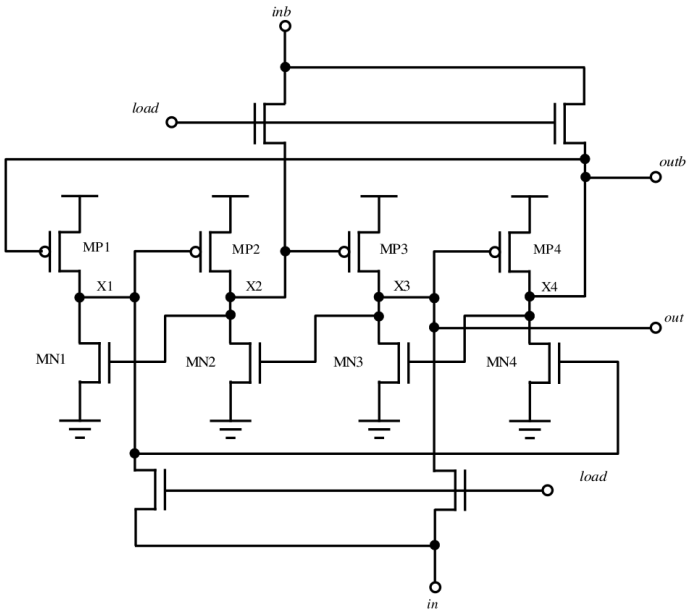

Figure 2. DICE latch structure.

However, it is noted that processes with smaller feature sizes are not intrinsically more Single Event Effect (SEE) hard, and the resistance of the design in particular to Single Event Upset (SEU) needs to be evaluated. In fact, on the one hand, a smaller device gives a smaller sensitive volume that contributes to a smaller cross-section and the design could be more tolerant to SEU. But on the other hand, in the smaller device the capacitance of storage nodes becomes smaller and the used supply voltage becomes lower. This makes the critical charge needed to provoke an upset lower than in older processes and digital designs could be less tolerant against SEU.

Because traditional flip-flops/latches are not suitable to be used in the IBL environment, configuration memories based on the Dual Interlocked CElls (DICE) has been studied, evaluated and implemented in the FE-I4 chip as SEU tolerant memories [4].

2.2 DICE latch description

DICE latches have redundant storage nodes and restore the cell original state when an SEU error is introduced in a single node [5]. The probability of multiple critical nodes to be affected is low making the DICE latch less sensitive to SEU.

Figure 2 shows the DICE latch structure. It is based on the conventional cross coupled inverter latch structure where the 4 nodes X1 to X4 store data as 2 pairs of complementary values. For example, when the stored data are 0 then X1-X2-X3-X4 = 0101 and in particular X1 is low and X4 is high. If we assume a positive upset pulse on the node X1, the transistor MP2 is blocked avoiding the propagation of this perturbation to the node X2. At the same time the transistor MN4 will propagate a negative pulse to the node X4 blocking MN3 and avoiding X3 level corruption. The perturbation is then removed after the upset transient since the nodes X2 and X3 have conserved the true information. However, if 2 sensitive nodes of the cell storing the same logic state (X1-X3)

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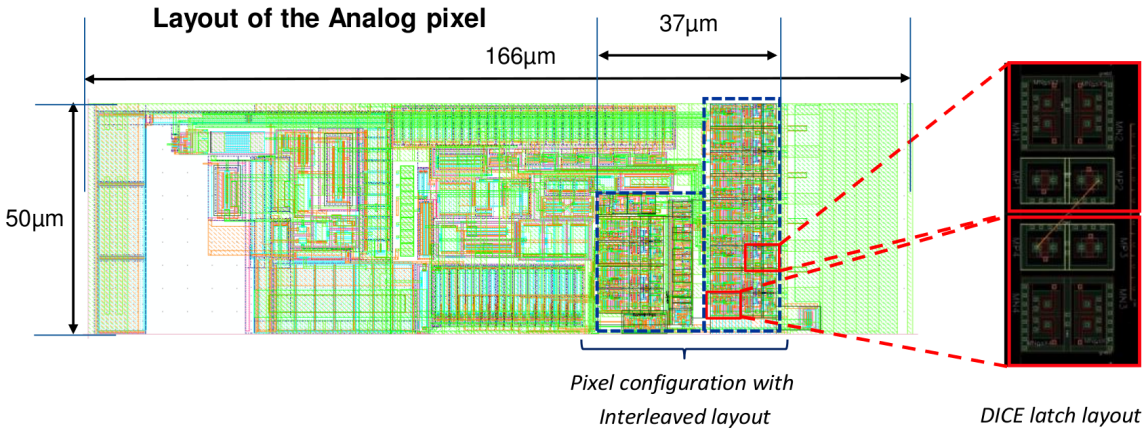

Figure 3. Interleaved layout for pixel configuration DICE latches.

or (X2-X4) change the state level due to the effect of a single particle impact, the immunity is lost and the DICE latch is upset, which is an issue.

For highly scaled processes, the device size shrinks and the space between critical nodes is reduced. The redundancy becomes less efficient because the perturbing charge becomes more often shared between sensitive nodes in the DICE latch. For this reason, some Hardened By Design (HBD) approaches are used to reduce the effect of charge sharing. Layout considerations based on spatial separation of critical nodes, isolation techniques like isolated wells and guard rings and cell interleaving are followed in the configuration memories design to increase the tolerance to SEU.

2.3 Pixel configuration memory

The analog pixel is configured with about 20 bits for global settings and 13 configuration bits for local adjustment (threshold local tuning, pre-amplifier feedback local tuning, charge injection circuitry...). Each pixel has 13 SEU-hard transparent latches. These can be set to either latched or transparent for a whole double-column at once. The only two possible operations on the pixel latches are load and read and there is no command to reset latches to zero. In fact such functionality would make the latches vulnerable to SEUs. Each of the 40 double-columns shelters its own shift register. A pixel strobe bit controls which latches can be written from the shift register when the pixels are in load mode and which ones can be read back when the pixels are in the read mode.

2.3.1 Implementation

In the FE-I4 pixel, to improve the SEU tolerance, interleaved layout is followed for each latch in the pixel to make the sensitive pair nodes of each DICE latch separated as much as possible (figure 3). However, it complicates the interconnection between elementary cells and increases the dedicate area of about 25%.

2.3.2 SEU results

Irradiation tests were carried out using the IRRAD3 beam line of the Proton Synchrotron (PS) facility at CERN. The IRRAD3 provides a beam of 24 GeV protons and the structure of the beam is defined by the operation cycle of the PS accelerator. The machine super-cycle period depends

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Table 1. Measured SEU cross sections for latch versions implemented in the FE-I4A chip.

	Rate/spill	Cross-section
Version 1	3.0	$31 \cdot 10^{-15}$ cm^2
Version 2	0.1	$1.1 \cdot 10^{-15}$ cm^2

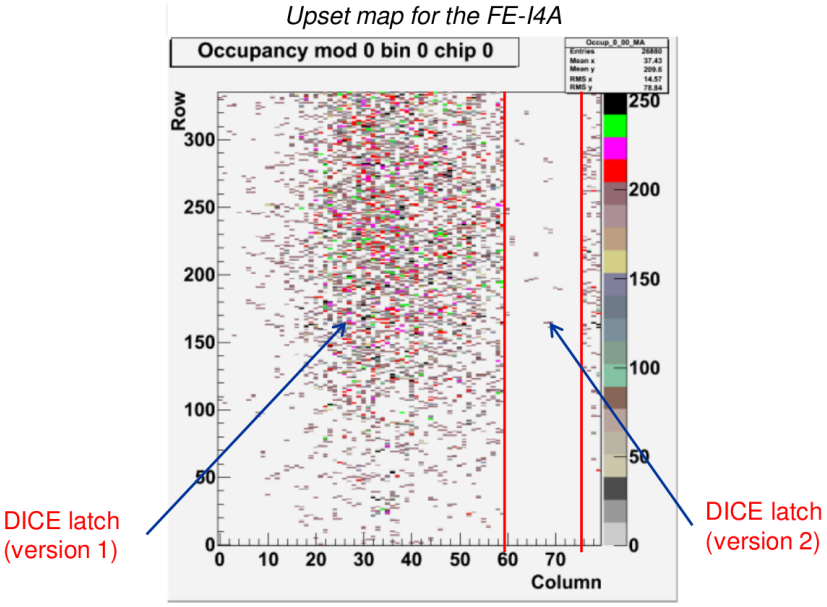

Figure 4. Latch upset map for the two latch versions implemented in the FE-I4A chip.

on the operation mode. It contains several spills of particles and it is distributed to the experiments sharing the beam. The IRRAD3 beam line, used for the chip irradiations receives 1 to 4 spills per super-cycle.

The duration of each spill is 400 ms and the intensity can be tuned typically from $5 \cdot 10^{10}$ to $1.5 \cdot 10^{11}$ protons/spill. A secondary emission chamber (SEC) monitors the proton beam intensity. During all the irradiation testing, devices are held perpendicularly to the radiation beam corresponding to a beam incidence angle of 90 degrees.

SEU measurements were carried out on the FE-I4A chip in which 2 versions of the DICE were implemented. Table 1 shows that the version 2, where the interleaved layout is adopted and where the diffusion area of sensitive nodes is minimized, is 30 times more resistant to SEU than the other version using a similar schema but where no layout approaches has been followed.

Figure 4 shows a latch upset map from a recent PS exposure. This map was produced by disabling all pixels and then periodically injecting test charge during exposure. An upset from 0 to 1 of the pixel enable bit (one latch per pixel) will cause a pixel to respond to charge injection and show up in the plot. In this configuration, we can directly see lower SEU rate for the column flavor where the second, optimized layout of the latches was used. The version 2 of the pixel latch configuration is adopted in the whole FE-I4B chip considered now as the IBL production chip.

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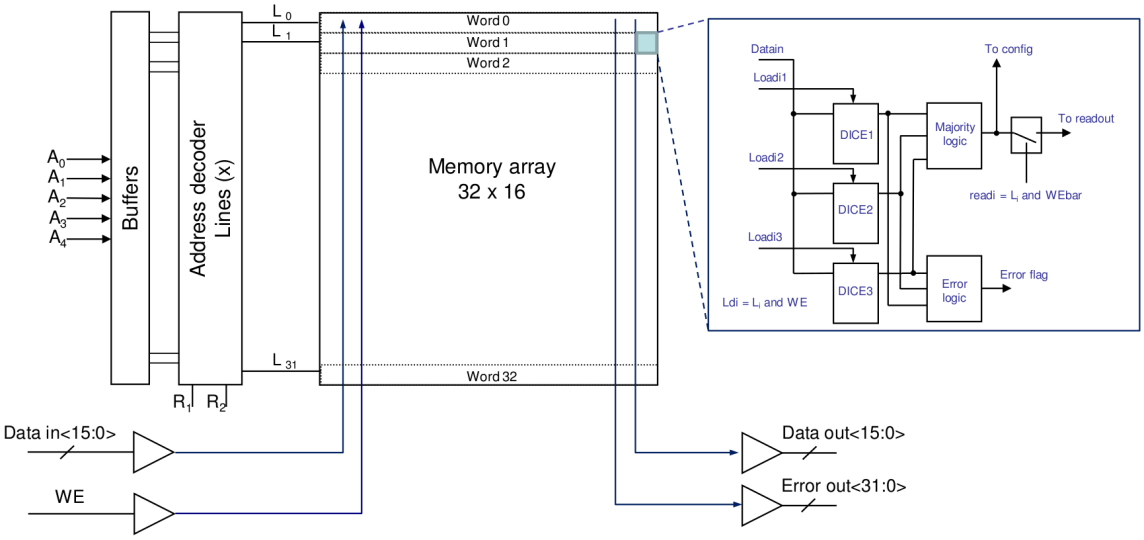

Figure 5. The FE-I4 global memory architecture.

2.4 Global configuration memory

The FE-I4 functionality is configurable by programming a master memory bank. This global configuration memory chip is implemented as a memory block of 32 words of 16 bits (512 bits in total). The main requirement is the high level of tolerance to Single Event Upsets (SEU). In fact any bit error in this memory block can highly affect the operation of the chip.

The design used for this global memory is based on the triplication of the DICE latch, presented in the first section, with the addition of simple majority logic. No automatic error correction is used, but single bit flips are monitored by an error counter and can be read back through the standard chip data output.

2.4.1 Architecture and implementation

Figure 5 shows the block diagram of the global memory. It is based on an array of 32×16 data bits addressed through a 5 bit address bus. Because of the triplication of the basic cell, the memory array has two independent ports. The first is used to write data coming from the command decoder and the second to read the majority logic output. The two ports use the same bus address line. The Write Enable (WE) is distributed into the whole memory block and is associated to the decoded address line in order to load the cell memory or to read the majority logic bit information. The 16 bits of each data word are available as parallel static output bits for use as configuration bits throughout the chip.

This memory can also be read back through the common data bus in order to read the contents via the output data stream. 32 error out flags are also generated, one flag per 16 bits data word. This error out signal is asserted if there is a mismatch in any of the three storing bit. These 32 outputs are ORed together to make a single error flag for monitoring by one Error Counter.

The R1 and R2 inputs are two negative logic resets. When they are asserted together, all bits of the configuration memory are pushed to a stable state, which is important at power-up. This reset can also take place automatically if a high enough radiation dose rate triggers the Prompt

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Table 2. Upset errors classification for the global memory of the FE-I4A.

	TRL SEU	PRD error	Command decoder glitches	Memory internal glitches
Errors number	2	79	11	10
Rate	0.1%	5.3%	0.7%	0.7%

Radiation Detectors (PRD) built into the chip. The user cannot disable or alter this feature, which is implemented for legal reasons.

A majority logic voting circuit is implemented in each cell to determine the effective output data. This data bit is corrupted only when more than one latch is upset.

2.4.2 Global memory SEU results

As for the pixel memory, the global configuration memory block was irradiated with the 24 GeV protons beam. In this case, the typical rate of errors is 6.8% (102/1480 spills) which is much higher than predicted. In fact, most of the observed errors are not related to the DICE latches themselves, but to the propagation of a Single Event Transient (SET) in the combinatory logic implemented to control this global memory.

Service Record Data (SR) implemented on the End of Chip Logic was checked during SEU tests to determine the main cause of the error [3]. This allowed dressing an error classification as shown in table 2. For example the error can be considered as propagated from glitches inside the memory block when:

- The mismatch between data written inside the memory and the data read back after the spill concerns a set of bits.
- The SR indicates that the memory error out flag is not asserted.
- The SR indicates that no error happens in the command decoder stage.

It can be noted from the table 2 that the reset caused by the PRD activation represents the largest source of errors in the FE-I4A.

Changes have been done in the FE-I4B chip to reduce PRD and glitches effects:

- The PRD threshold is increased.
- A third detector is added in the chip and the location of the 3 PRD detectors is separated.
- The load path is triplicated inside the memory block to reduce the sensitivity to glitches.

Data taken during the FE-I4B irradiation tests are still under analysis. However, this test shows clearly that the PRD-like errors and glitch errors decrease drastically.

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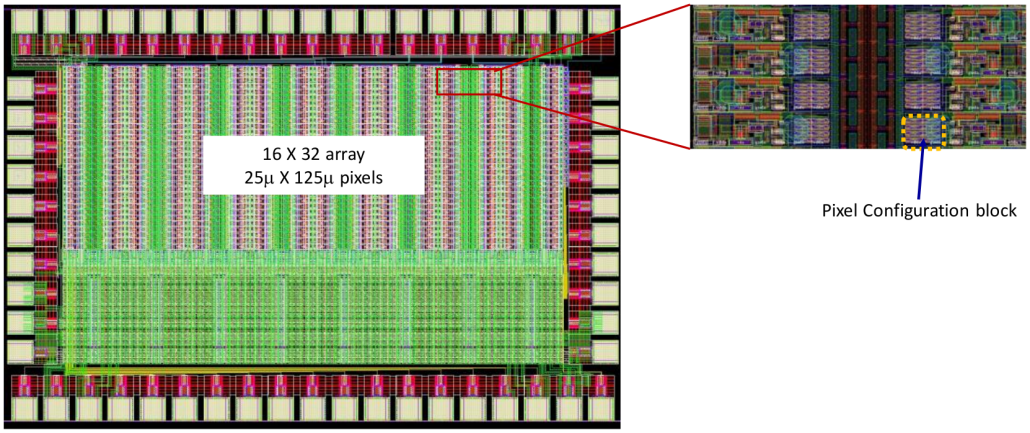

Figure 6. ATPIX65 chip prototype.

3 65 nm prototype for future inner pixel layers

3.1 Prototype chip description

Figure 6 shows the ATPIX65 prototype chip designed in Berkeley in a 65 nm CMOS process to explore the capabilities of advanced CMOS processes for analog front end design and to evaluate radiation hardness particularly for the future ATLAS pixel chip to be designed for the inner layers in the future upgrades [7].

The prototype chip is organized as an array of 32 rows by 16 columns where only one column is validated at the same time. The column selection is done using a 16 to 1 multiplexer at the output and a 1 to 16 demultiplexer at the input. Each analog pixel is configured with 8 configuration bits for local adjustment. All bits are stored in SEU tolerant latches based on the triple redundancy of standard latches with an additional logic for error correction.

As shown in figure 7, all the 4096 configuration bits can be accessed using shift registers based on DFF cell of the standard library. Shifting the patterns and loading the bits into latches is performed using a simple protocol which requires three chip pins: data input (SRIN), clock (CK), load (LD). The read back pin (RDBACK) allows the loading of data from the TRL cells on to the shift register prior to the reading back of this information through the shift out (SROUT) data.

3.2 SEU test results

As for the FE-I4 chip, irradiation tests were carried out at the 24 GeV protons beam at CERN (PS) and the chip was set perpendicularly to the beam. A data acquisition system based on FPGA has been designed to compute the number of errors occurring during each Super Cycle of the PS (CPS). The input data alternates “all 1” and “all 0” patterns at each CPS. Errors are computed simultaneously for the TRL latches and for the DFF cells of the shift registers. So, measuring the cross section for the two cells allows estimating the effect of the triple redundancy and of the error correction circuit on the tolerance to single event upset.

The cross section is determined as the total number of errors obtained for the whole memory N_{errors} over the total proton fluence Φ achieved during the test and divided by the number of the

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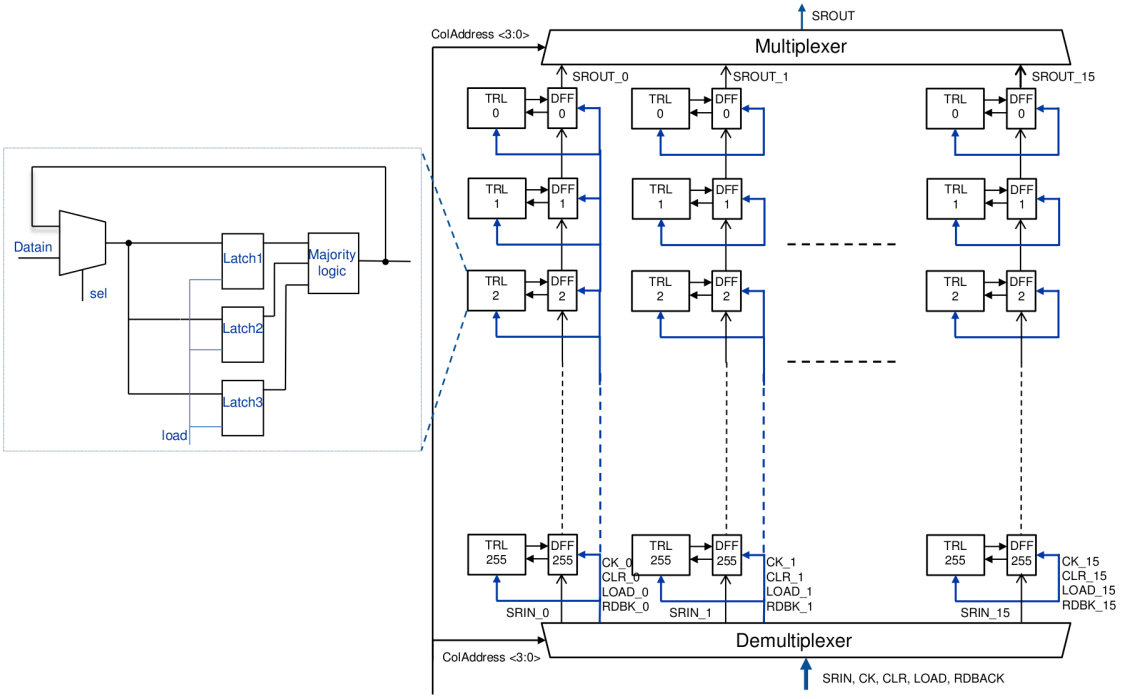

Figure 7. Organization of the prototype chip configuration memory.

Table 3. Measured cross section for single DFF cell and for the TRL cell.

			Cross section (cm^2/bit)		
	Size	Area	All	0 to 1	1 to 0
TRL for configuration	$12.5\,\mu m \times 4.3\,\mu m$	$54\,\mu m^2$	$2.6 \cdot 10^{-16}$	$2.64 \cdot 10^{-16}$	$2.55 \cdot 10^{-16}$
DFF for shift register	$6\,\mu m \times 2.4\,\mu m$	$14.4\,\mu m^2$	$4.5 \cdot 10^{-14}$	$5.9 \cdot 10^{-14}$	$3.0 \cdot 10^{-14}$

latches memories N_{latches} implemented in the chip.

$$\sigma = \frac{N_{\text{errors}}}{\Phi \times N_{\text{latches}}}$$

Table 3 shows the measured cross section for the single DFF cell and for the TRL cell. The redundancy and the error correction logic implemented in each TRL cell allow improving the tolerance to SEU by a factor 170 and reaching a cross section of $2.6 \cdot 10^{-16}$ cm^2/bit. Using this value, and taking 13 configuration bits per pixel as is the case for the FE-I4, the mean time between 2 errors for 1 front end chip containing 100 k pixels and placed in B-layer can be estimated to 20 s. This error rate would still be manageable since only a fraction of the configuration bits are critical for the pixel (in FE-I4 case, 2 of 13). It should be underlined, that those pixels having a critical configuration bit flipped could be easily detected as having too much activity or too little activity, and hence could be reprogrammed on the fly as soon as possible. A more SEU-tolerant design is now under development in order to be used for these critical configuration latches in the future front end chip design.

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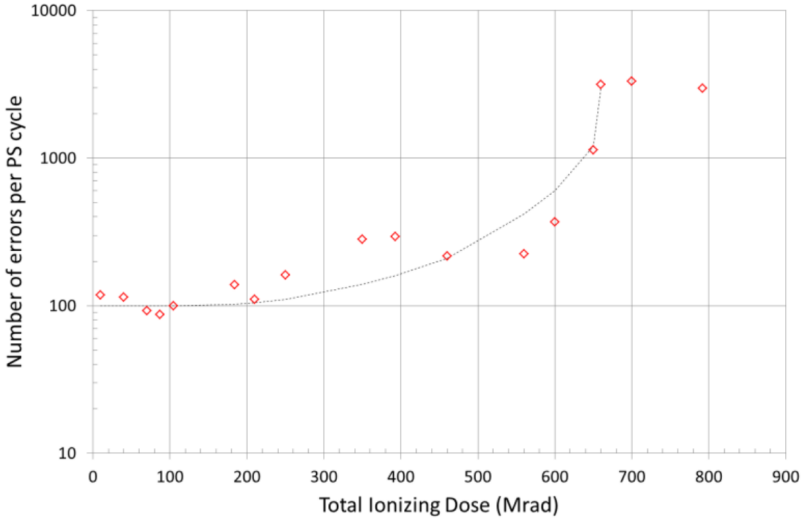

Figure 8. Evolution of the error rate per cycle with the total dose ("all 1" pattern).

Despite the use of error correction, the approach used in the design does not allow a complete mitigation of SEU. The TRL cell shown in figure 7 avoids the accumulation of upsets in the latches by the use of majority logic and feedback but the combinatorial logic should be also rightfully protected, in order to avoid the propagation of transient upsets from the logic to the latches. More tolerance to SEU requires for example the use of time redundancy with applying sufficient delays between the three load signals of the three single latches. Another possibility is to triplicate all the combinatorial logic inside the TRL cell. Both solutions require increasing the area of the configuration cell and this might not be compatible with pixel size reduction.

3.3 Dose effects

At the IRRAD3 beam line of the Proton Synchrotron (PS), the dose rate is estimated to 6 kRad(Si)/spill. During the SEU tests, the level of dose was monitored to estimate the dose effect on individual MOSFET transistors and the effect on the memory cells used for configuration.

Figure 8 shows the evolution of the error rate of the DFF cells used in the shift register design. Starting at a dose level of 250 MRad, we observe a higher rate of errors for the "all 1" pattern and a lower rate for the "all 0" pattern. In addition, we observed for the "all 1" pattern an increase in the number of multiple bit upset for which the errors occur simultaneously in consecutive DFF cells. This behavior can be attributed to transistor threshold voltage shifts and mobility degradation reducing the critical charge needed to provoke an upset.

From a dose level of 400 MRad, failures in the DFF cells are observed for the "all 1" pattern and are particularly visible for a higher levels of dose as shown in figure 9 (bottom plots). After this dose, there are 2 contributions to the total error count: a first contribution comes from "random errors" located within the matrix and changing location from cycle to cycle, and a second contribution comes from "fix errors", always located for each cycle at the very top of the pixel matrix. In fact, bits located at the top are always and for each CPS cycle in the "0 state" while they should be set to 1.

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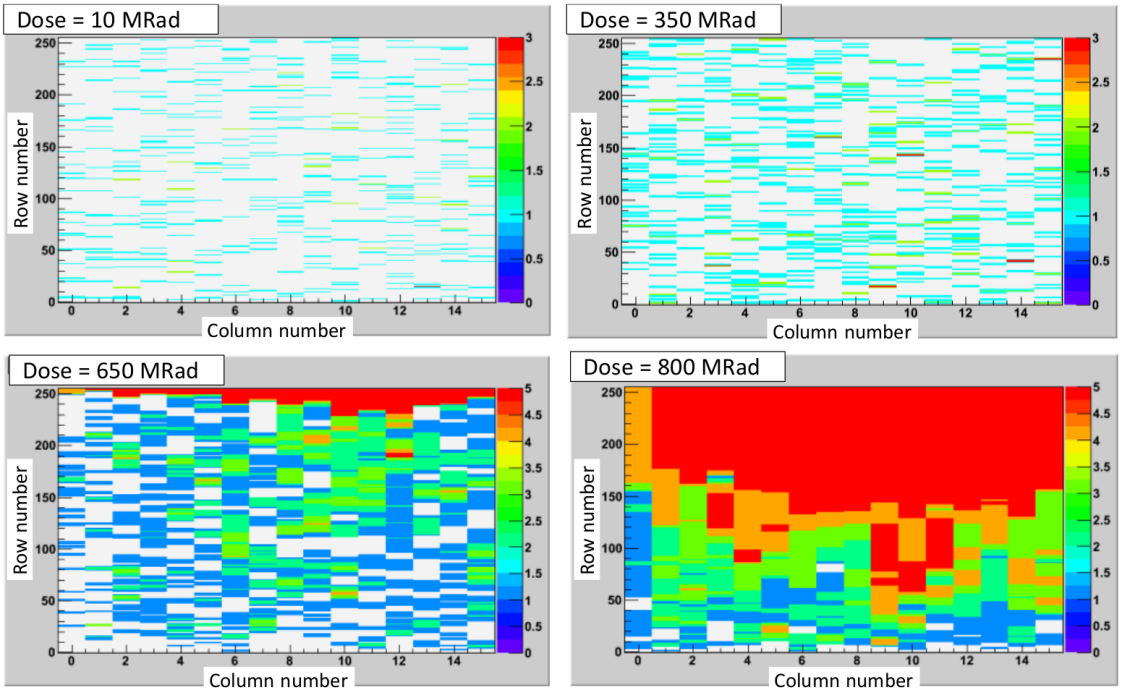

Figure 9. Shift registers SEU map plot for 5 CPS cycle ("all 1" pattern).

It should be noted that the corrupted cells correspond to the DFFs situated in the first locations of the shift register chain and that at the end of the configuration, the serial input of the shift register is set to 0 during the "all 1" pattern test. The hypothesis is that this "0" is propagated to the first DFF output without clock validation. This could be due to the fact that DFF switches assumed to be in the off state start to be less resistive. With increasing the dose, the resistance of the switches decreases and the input state is propagated to more DFF cells. We observed that this effect concerns about the half of the cells at a dose level of 800 MRad. This assumption is corroborated by the fact that SEU errors occurring in DFF cells not situated at the top and for which the state is changed from 1 to 0 are also propagated to the next cells as shown in figure 9.

The effect persists even when the chip is placed outside the beam but the number of errors decreases after annealing and most columns in the chip seems return to normal behavior after 420 hours of annealing.

4 Conclusion and perspectives

The FE-I4B chip copes with the challenging IBL requirements in terms of SEU for local and global configuration memories, by using a strategy of customized DICE layout for the local configuration cells, and customized DICE latches with TRL and majority logic in the periphery. The FE-I4B chip is now used for the IBL production. Data taken during the FE-I4B irradiation tests are still under analysis in order to understand the cause of the remaining glitches errors in the global configuration memories.

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For the future pixel design to be used for the upgrades, a prototype chip organized as a small array of pixels has been designed in a 65 nm CMOS process. In this chip, configuration memories are based on triple redundancy latches designed with standard library cells. A good result in term of tolerance to SEU has been obtained. However, we observed that from a radiation dose of 400 MRad, cell failure appears in the DFF cells located in particular at the very top of the pixel matrix. This behavior is still now under study but could be explained by the low resistance of switches in the off state after irradiation. A new chip including different structures of configuration memories is now under development.

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