AIDA-PUB-2013-016

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21 December 2013

The research leading to these results has received funding from the European Commission under the FP7 Research Infrastructures project AIDA, grant agreement no. 262025.

This work is part of AIDA Work Package **3: Microelectronics and interconnection technology**.

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Nuclear Instruments and Methods in Physics Research A 732 (2013) 506–510

Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

A 10 MS/s 8-bit charge-redistribution ADC for hybrid pixel applications in 65 m CMOS

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ARTICLE INFO

Available online 15 June 2013

Keywords:
Analog-to-digital converter
Front-end
Pixel detector

ABSTRACT

The design and measurement results of an 8-bit SAR ADC, based on a charge-redistribution DAC, are presented. This ADC is characterized by superior power efficiency and small area, realized by employing a lateral metal–metal capacitor array and a dynamic two-stage comparator. To avoid the need for a high-speed clock and its associated power consumption, an asynchronous logic was implemented in a logic control cell. A test chip has been developed in a 65 nm CMOS technology, including eight ADC channels with different layout flavors of the capacitor array, a transimpedance amplifier as a signal input structure, a serializer, and a custom-made LVDS driver for data transmission. The integral (INL) and differential (DNL) nonlinearities are measured below 0.5 LSB and 0.8 LSB, respectively, for the best channel operating at a sampling frequency of 10 MS/s. The area occupies 40 μm × 70 μm for one ADC channel. The power consumption is estimated as 4 μW at 1 MS/s and 38 μW at 10 MS/s with a supply rail of 1.2 V. These excellent performance features and the natural radiation hardness of the design, due to the thin gate oxide thickness of transistors, are very interesting for front-end electronics ICs of future hybrid-pixel detector systems.

1. Introduction

Modern deep-submicron CMOS technology plays an important role in current collider experiments because the huge number of channels in finely segmented sensor (pixel) systems can only be addressed with highly integrated custom-designed electronics circuits, e.g., more than 8×10^7 channels for ATLAS silicon pixel detectors [1]. The gate length of 65 nm CMOS is currently the minimum feature size which is applied to front-end electronics in a future collider experiment, i.e., the data handling processor (DHP) for the pixel detector of Belle-II experiment at KEK [2].

With shrinking a technological feature size, more complicated functions can be integrated into pixels with significantly smaller area. Besides that, a smaller feature size has a merit in terms of its intrinsic radiation hardness due to thinner gate oxide. However, these general trends are mainly beneficial for digital circuits, and not necessarily for analog circuits because of the reduced voltage headroom and larger gate leakage current due to the thinner gate oxide. One solution to overcome the discrepancy is to combine wafers processed with different technologies by vertically penetrating silicon-vias of 3D vertical integration technology [3,4]. In this technology, two or more layers of thinned semiconductor devices, called “tiers”, can be theoretically made in different technologies, e.g., BiCMOS, SiGe, CMOS, and interconnected by vias to form a “monolithic” circuit. Although such technology enables us to integrate circuits in much higher densities, the design of electronics becomes more challenging. For instance, the power dissipation allowed per pixel decreases because the cooling of electronics and sensor becomes difficult in the low-mass support structures required in particle physics. Also the digital readout architectures had to process much higher data volumes at the same time. In such fully functional front-end electronics, a power- and area-efficient ADC becomes one of the crucial circuit components for bridging analog and digital signals.

In this article, we present the recent development of an 8-bit SAR (successive approximation register) ADC, based on a charge-redistribution DAC. Although the circuit topology is originally proposed for wireless communication receivers [5–7], its power-efficient design is also suitable for front-end electronics for future collider experiments. The power- and area-efficient ADC with promising performance will exploit its application in the field of hybrid pixel or 3D integrated detectors for physics experiments and X-ray imaging detectors [4,13].

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http://dx.doi.org/10.1016/j.nima.2013.05.192

2. Design of the ADC circuit

2.1. Overview of the ASIC

Fig. 1 shows the block diagram of the ADC circuit. The overall circuit consists of a transimpedance amplifier (TIA) as a signal input structure, eight ADC channels with different layout flavors of a capacitor array, a serializer, and a custom-made LVDS driver for data transmission. Four channels were implemented with asynchronous and the other four with synchronous control logic. The test chip was fabricated in TSMC 65 nm standard CMOS technology.

2.2. Architecture of SAR-ADC

Fig. 2 shows the block diagram of the ADC core. The ADC uses the successive approximation register (SAR) architecture. The overall ADC circuit consists of a comparator, control logic, and a charge-redistribution DAC implemented by binary-scaled capacitors C0 (LSB) up to C7 (MSB) and corresponding drivers. The principle of a charge-redistribution DAC and its application in a SAR-ADC are well known in the literature [8].

The conversion process starts with the sampling of the input signal (V_{DAC}). In this stage, all DAC bits (D0–D7) are reset to a state where the MSB is high and all other bits are low. After the sampling, the comparator is activated by a clock signal to determine the MSB, and according to its result, the control logic decides if the MSB should remain high or set low, i.e., a charge k is equal to half of the input range is added to or subtracted from V_{DAC}. The next bits are determined in a similar operation: the comparator determines the sign of the charge for each iteration, and the procedure is repeated until 8 comparisons have been done for 8 bit resolution. The binary-scaled capacitors are switched one by one to make the total charge converge to a reference voltage V_{ref}. To avoid the need for a high-speed clock and its associated power consumption in the digital logic, an asynchronous logic controller was implemented to operate on a single sampling clock [7]. A synchronous logic controller was also implemented into four ADC channels for testing, however, we focus on the asynchronous ADCs in this paper. As for the comparator design, we employed a dynamic two-stage comparator scheme [6]. The comparator consists of an input PMOS differential pair feeding a current into a regenerative cross-coupled pair and following inverter stage to obtain the rail-to-rail digital output. Using this topology, the comparator does not consume any power when it is inactive and thus the power consumption of the ADC scales almost linearly with the sampling frequency [6].

Fig. 3 shows a layout example of one channel ADC. In order to achieve a high power efficiency the implementation of capacitors with small values is required for the capacitor array. Since the minimum capacitance value of a standard MIM structure is above 10 fF in the chosen 65 nm technology, we employed a custom-made metal–metal parasitic capacitor with lateral and stacked structures. The intended parasitic capacitance was optimized by the help of standard parasitic extraction tools. These structures aided to reduce the capacitance and layout area while preserving the required matching criteria since the accuracy of metal etching generally becomes better in smaller feature-size technologies. The structure uses metal layers 2 and 3 stacked together with minimum metal width and minimum metal spacing, while metal layers 6 and 7 are used for the differential input branch. The metal layers 1 and 4 are used for routing and shielding. Since the accuracy of the DAC is dependent on the matching and noise in the capacitor array, we prepared four different layouts (labeled as C2–5 in Fig. 3) for comparison. The minimum LSB capacitance is approximately 1 fF in the layouts C2 and C3. To prevent systematic mismatch errors in the DAC, a common-centroid technique was used.

2.3. Peripheral circuits: TIA and LVDS driver

The transimpedance amplifier consists of a common-source stage and a source follower. The open-loop gain and bandwidth can be adjusted with two independent current sources and adjustable feedback capacitance. Although the parameters are not optimized for a specific detector, the input current range was designed for 10 μA, assuming the current signals generated by the in-pixel transistors of a DEPFET sensor matrix as a detector [9].

A design of the custom-made LVDS driver was inherited from that of the pixel front-end chip (FE-I4) that is used for the upgraded ATLAS experiment [10]. The driver implementation is based on a common four transistor switch scheme arranged in a

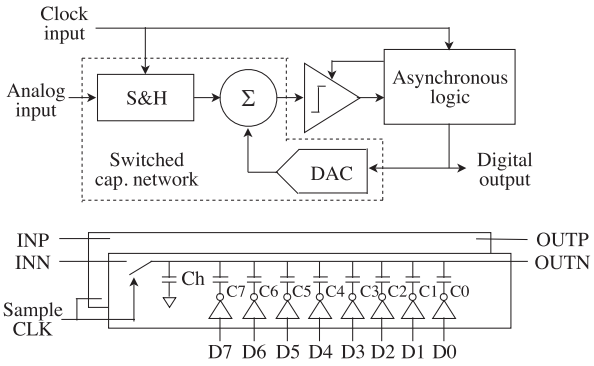

Fig. 2. Block diagram of the SAR-ADC with a differential charge-redistribution DAC [7].

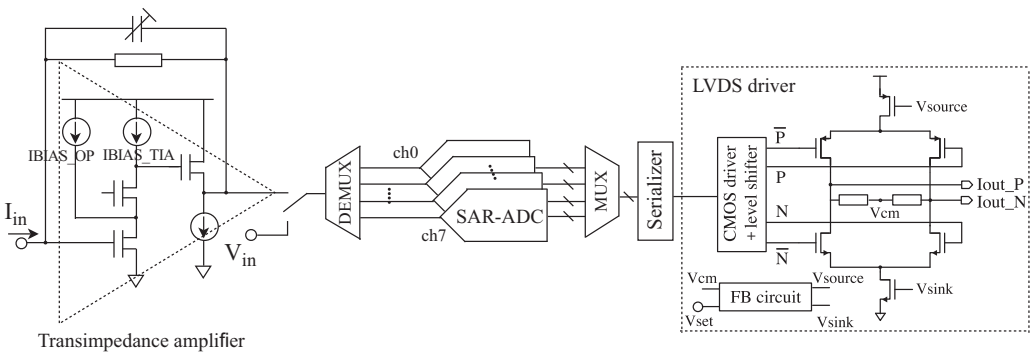

Fig. 1. Block diagram of the ADC chip.

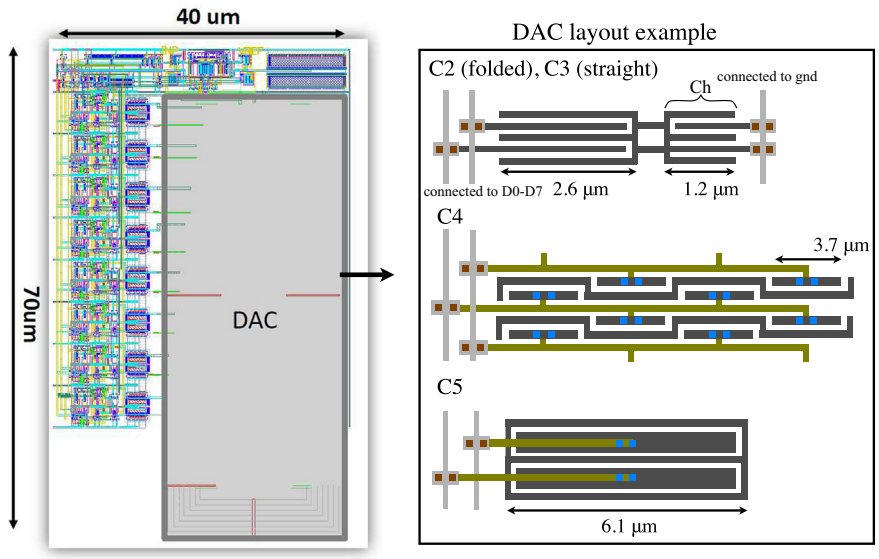

Fig. 3. Layout of a typical ADC channel.

bridge configuration including the functionality to adjust the signal current magnitude and the common-mode output voltage. To operate the driver with dual supply lines, i.e., 1.2 V for core transistors and 1.8 V for *I/O* pads, a level shifter was inserted for driving the switching transistors with the *I/O* voltage.

3. Measurement results

3.1. Performance of the ADC

To compare noise properties of different ADC flavors, we first operated each ADC channel in a single-ended mode and at a moderate sampling frequency of 1 MS/s with external voltage input. The transfer characteristics and corresponding INL and DNL results are shown in Figs. 4 and 5. We can see that input voltage ranges are slightly different from each other. This comes from variations of the pre-charged hold capacitance C_h (Fig. 2). The maximum input range was obtained with the layout C4, in which no C_h component was implemented except parasitics, and its range almost equals the core supply rail. In Fig. 3, C_h is shown in the right side of the DAC layout C2 (C3). The room for optimizing the ADC input range is practically favorable because the voltage headroom for signal amplification in analog circuits decreases in modern deep-submicron technologies. In Fig. 5, the layout C2 shows periodic spikes in the DNL, we found that those come from a faulty connection leading to a floating node C_h. Small DNL spikes appearing in each binary-scaled bit are due to the unavoidable parasitic effects for routing between the capacitor array. From the INL and DNL results of Fig. 5, we conclude that the layout C3 performs best.

Consequently, we focused on the layout C3 and increased the sampling frequency. The integral (INL) and differential (DNL) nonlinearities were measured below 0.5 LSB and 0.6 LSB at a sampling frequency of 10 MS/s, and measured below 0.6 LSB up to a sampling frequency of 12.5 MS/s (Fig. 6). This result reveals that the matching of the lateral metal capacitors is sufficient for 8 bit accuracy. The power consumption is simulated as 4 μW at a sampling frequency of 1 MS/s, and 38 μW with 10 MS/s. It is quite difficult to extract the power consumption of the ADC from measurements, hence no measured values can be given. Table 1 summarizes the ADC properties.

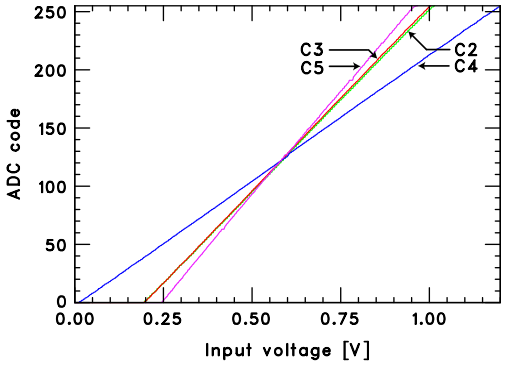

Fig. 4. Transfer characteristics of the ADCs with different layout flavors.

3.2. Performance of the TIA and LVDS driver

The LVDS driver has been prototyped independently, and characterized by measurements in parallel with the ADC circuit. Fig. 7 shows the eye-diagram of the LVDS transmitter at a data rate of 320 Mbps. The measurement was performed without transmission line and with an active differential probe across a 100Ω termination register. The output voltage swing could be adjusted at a range of 50–400 mV. The LVDS driver works at a frequency of up to 640 MHz without cables, while it works up to 100 MHz with an eye opening of about 110 mV when it is connected to a 20 m twisted pair cable.

The combined noise level of the TIA and ADC (layout C3) was measured as below 0.8 LSB (rms, Fig. 8). To reduce the noise of the ADC, we operated the ADC at 1 MS/s in the measurement, and the noise of the ADC was about 0.4 LSB. On the other hand, the TIA noise level is simulated as 2 mV. This value corresponds to 0.64 LSB in the ADC output if we account for the input voltage range of the layout C3, i.e., 0.8 V (peak-to-peak). Thus the simulated noise level is consistent with the measurement value deduced by $\sigma^2_{\mathrm{TIA+ADC}} = \sigma^2_{\mathrm{TIA}} + \sigma^2_{\mathrm{ADC}}$.

4. Summary and future prospects

A low-power and area-efficient ADC has been developed in TSMC 65 nm standard CMOS technology. The ADC is based on

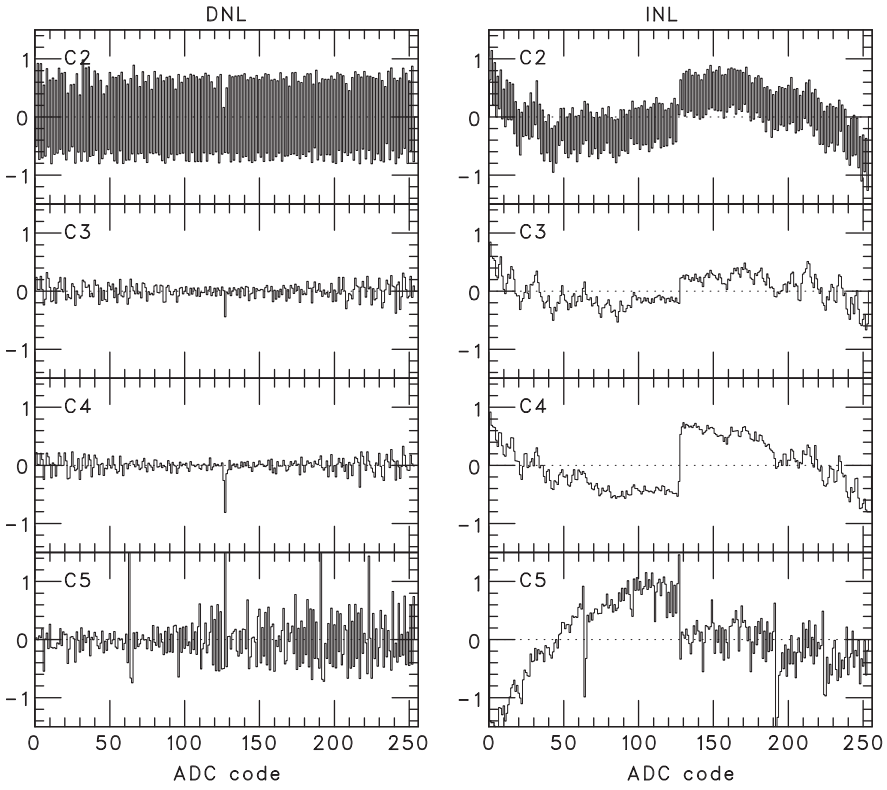

Fig. 5. INL and DNL of each ADC channel, operating in a single-ended mode and at a sampling frequency of 1 MS/s.

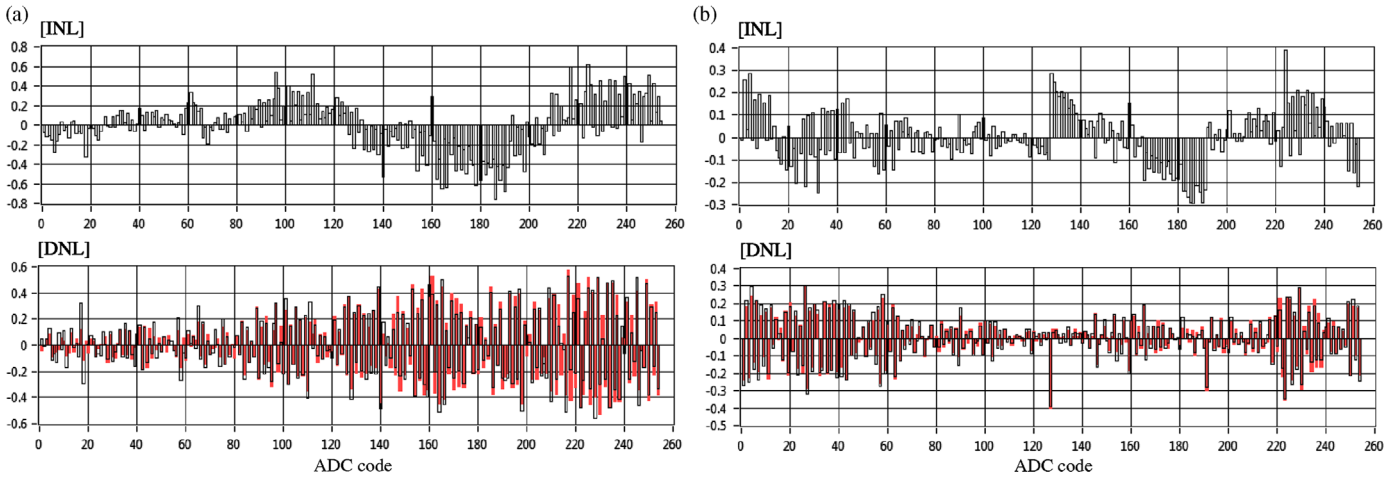

Fig. 6. INL and DNL of the best channel (layout C3), operating in (a) the single-ended mode and (b) differential input mode at a sampling frequency of 12.5 MS/s.

Table 1
Summary of the performance features of the ADC.

Technology	TSMC 65 nm CMOS, 9 metals
Supply rails	1.2 V for core & 1.8 V for *I/O*
Input range, resolutions	0–1.2 V/0.3–0.9 V with 8 bits
INL (C3 in diff. mode)	0.2 LSB @ 1 MS/s, 0.6 LSB @ 10 MS/s
DNL	0.3 LSB @ 1 MS/s, 0.5 LSB @ 10 MS/s
Area for one channel	40 μm × 70 μm
Power consumption	4 μW @ 1MS/s, 38 μW @ 10 MS/s

the SAR-architecture with a charge-redistribution DAC. To reduce power and area, a custom designed low capacitance array has been employed based on a parasitic capacitance of metal–metal lateral and stacked structures with a common-centroid layout technique. The typical area of one channel ADC occupies 40 μm × 70 μm. Test results confirmed that the matching of the lateral metal capacitors was sufficient for 8 bit accuracy. The power consumption is estimated as 4 μW with a sampling frequency of 1 MS/s, and 38 μW with 10 MS/s. These encouraging results with natural radiation hardness of transistors due to the thin gate oxide are attractive features for future front-end electronics in physics experiments and X-ray imaging detectors based on hybrid-pixel systems. We can take the following detector systems as an application example of the ADC; the fast readout architecture of the DEPFET in XFEL [11], Fine Pixel CCD as an option of the future ILC vertex detector [12], or two-dimensional readout for CdTe/CdZnTe detectors for X-ray astronomy [13].

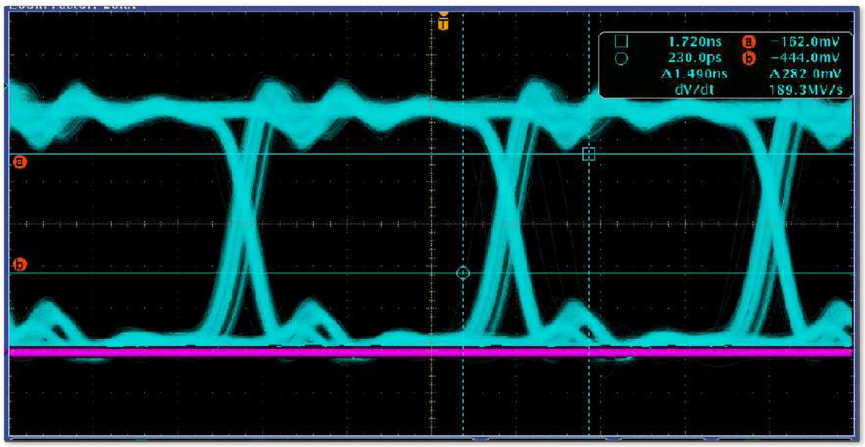

Fig. 7. Eye diagram of the LVDS measured at 320 Mbps without transmission line.

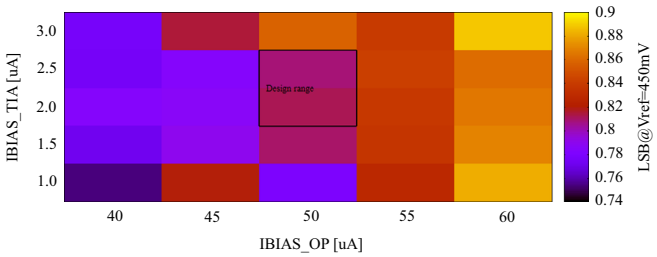

Fig. 8. Combined noise map (rms) of the TIA and ADC (C3) with different bias settings.

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