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KLauS – A charge readout and fast discrimination chip for silicon photomultipliers

Dorn, M (UHEI) *et al*

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KLauS – A charge readout and fast discrimination chip for silicon photomultipliers

M. Dorn, T. Harion,¹ W. Shen, G. Sidlauskas and H.C. Schultz-Coulon

*Kirchhoff-Institut,
Im Neuenheimer Feld 227, Heidelberg, Germany*

E-mail: tharion@kip.uni-heidelberg.de

ABSTRACT: KLauS is an application specific integrated circuit (ASIC) for the readout of silicon photomultipliers. The chip has been designed for the application in the analog hadronic calorimeter developed by the CALICE collaboration for the next linear collider experiment. To address the severe power constraints introduced by the highly granular design of the calorimeter, the chip has been designed for low power consumption while maintaining the high dynamic range and timing precision required by the experiment. In addition, a power gating scheme has been implemented to further decrease the average power consumption. For a duty cycle of 1% a value of $25\ \mu\text{W}$ per channel is achieved without affecting the readout capabilities of the chip. The chip has been designed in the $0.35\ \mu\text{m}$ SiGe technology and provides a low power readout channel for SiPMs with low gain for the input stage of the existing readout chip SPIROC. The analog channel of KLauS will be implemented in a future version of the SPIROC chip.

KEYWORDS: Analogue electronic circuits; Front-end electronics for detector readout

¹Corresponding author.

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1 Introduction

Silicon Photomultipliers (SiPM) are novel photo detectors based on semiconductor technology. The high gain, of 10^5 to 10^6 , low operating voltage, insensitivity to magnetic fields and a small form factor make these devices an ideal candidate for the application in detectors for high energy physics experiments. Due to the insensitivity to magnetic fields and the small form factor, these sensors allow direct readout of scintillation light at its origin inside the particle detector, making the use of light guides obsolete while maintaining the possibility to build detectors with a high granularity.

The prototype of a highly granular analog hadronic calorimeter (AHCAL) using SiPMs for the readout of scintillation light was developed by the CALICE collaboration¹ [1]. The high granularity allows for advanced event reconstruction methods like the particle flow algorithm [3], promising unprecedented energy resolution in hadronic calorimetry. However, the dense structure necessary to achieve this high granularity leaves minimal space for infrastructure and readout electronics, posing many challenges to the front-end electronics. One of the major constraints is a very low power consumption of less than $40\mu\text{W}$ per channel for the electronic front-end ASIC in order to avoid active cooling.

The KLauS (Kanäle zur Ladungsaslese von SiPMs) chip has been designed to provide a low gain SiPM readout solution with a high dynamic range, precise signal timing and a tunable SiPM bias voltage while still addressing the power constraints introduced by the AHCAL design. The chip has been developed in the $0.35\mu\text{m}$ SiGe technology and is planned to be integrated in the next version of the existing readout chip SPIROC [2]. Figure 1a shows the layout of the KLauS2v0 chip. The chip consists of 12 analog channels which can be configured using a SPI interface.

¹Calorimeter for the Linear Collider Experiment.

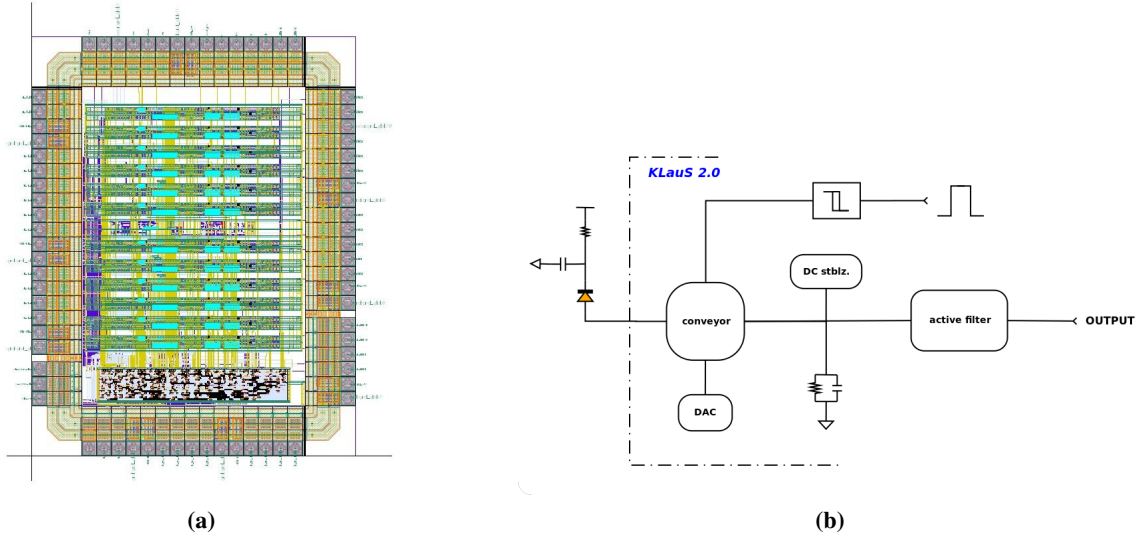


Figure 1. (a) Layout of the KLauS2v0 chip. (b) Diagram of the KLauS2v0 channel.

2 Circuit description

Aside from the severe power constraints of the system, a dynamic range of up to 200 pC for charge measurements of the SiPM signals is required. In addition, a precise trigger signal is required for the event reconstruction.

Figure 1b shows a diagram of the KLauS2v0 channel with the external SiPM sensor indicated as a diode. A low impedance at the input stage of the analog channel allows the signal charge to flow completely into the current conveyor of the channel where the signal is duplicated. The conveyor unit allows to configure the amplification for later signal processing using a multi-gain selection unit which scales down the input charge by a ratio of 1, 10 or 40. An 8 bit DAC allows to control the voltage at the input line of the channel, giving the possibility to fine tune the SiPM bias voltage. This is used to correct for temperature fluctuations and chip to chip variations in the SiPM breakdown voltages, thus allowing to stabilize the sensor gain. In order to achieve the very low power consumption required by the calorimeter, a power gating scheme has been implemented that utilizes the bunch pattern proposed by the International Linear Collider [4], to reduce the average power consumption. The design of the conveyor unit ensures that the effect of the power gating on the input bias of the sensor is negligible. The two signal copies generated by the current conveyor are used for the generation of a precise trigger signal and the charge measurement respectively.

2.1 Input stage

Figure 2 shows a diagram of the input stage schematic at the transistor level. The low input impedance can be determined by the transconductance of the transistors M1 and M4 and the width ratio of the transistors M2 and M3. If the channel length modulation of the current mirror is neglected, the low frequency impedance can be expressed by

$$\begin{aligned}
 R_{\text{in}} &= \frac{g_{m2}r_{ds1} \cdot g_{m4}r_{ds4} - g_{m1}r_{ds1} \cdot g_{m3}r_{ds4}}{g_{m2} \cdot g_{m1}r_{ds1} \cdot g_{m4}r_{ds4}} \\
 &= \frac{1}{g_{m1}} - \frac{1}{g_{m4}} \cdot \frac{g_{m3}}{g_{m2}}
 \end{aligned} \tag{2.1}$$

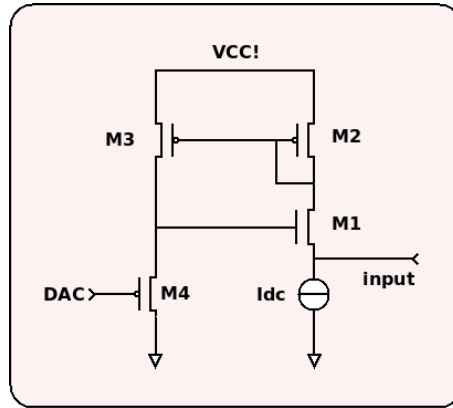


Figure 2. input stage diagram of KLauS chip.

The advantage of this input stage scheme is that the voltage from the digital to analogue converter can be directly applied onto the gate terminal of M4. In this case, the low gate leakage current will not disturb the performance of the low power DAC despite the large switching current in both M2-M3 mirror branches. This scheme also gives the possibility to maintain the input terminal bias voltage constant during variations in the bias current. A drawback of this scheme is the relative large noise, which has to be handled by the later processing stages to achieve a low noise design.

2.2 Signal processing

For energy measurements, the signal current is integrated on a passive integration unit and DC coupled into a shaping stage. The shaping is performed by an active filter, which adds two complex poles to the integration pulse so as to provide an output waveform without undershoot. If the real parts of the complex poles are the same as the exponential constant of the passive integration, the output waveform can be expressed as

$$U_{\text{out}}(t) = \frac{4R}{\tau} \cdot Q \cdot \sin^2\left(\frac{t}{2\tau}\right) \cdot \exp\left(-\frac{t}{\tau}\right) \quad (2.2)$$

where τ is the shaping time constant, Q is the input charge and R is the integration resistor. The shaping time of this unit can be configured to 25 ns, 50 ns and 100 ns. Due to the fast recovery time, the channel is capable of handling sensors with dark rates up to several MHz.

In order to have a tunable pedestal voltage, a pedestal stabilization unit with a response frequency of the order of kHz has been implemented inside the channel. All transistors inside this unit are biased in the sub threshold region to get a very low power consumption and keep the circuit active during all power gating stages. The signal discrimination is performed by a fast Schmitt trigger with pulse length calibration. The trigger thresholds can be selected in a range from single to multiple detected photons.

3 Characterization measurements

Figure 1a shows the layout of the KLauS2v0 chip. The chip consists of 12 analog channels which can be configured using a SPI interface.

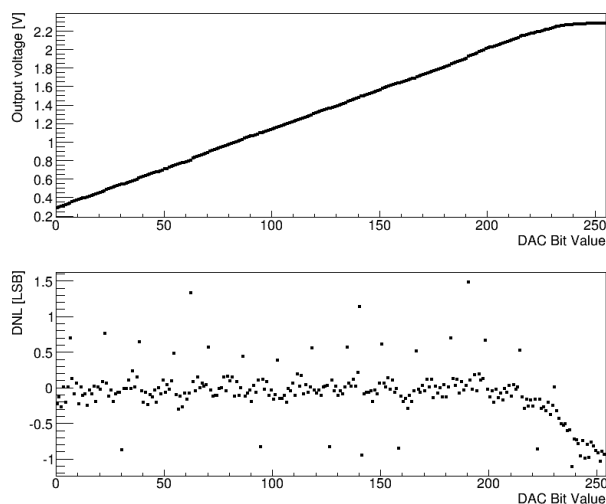


Figure 3. Voltage DAC scan for input bias voltage tuning.

3.1 Bias DAC linearity

For the tuning of the SiPM bias the linearity and range of the 8 bit DAC have been determined. For each programmed DAC value the corresponding output voltage at the input terminal has been measured.

The scan of the input bias voltage for one channel is shown in figure 3. A total range of 2 V has been observed with perfect monotonicity. The periodic deviations evident in the differential non linearity of the scan are due to a mismatch in a current mirror of the DAC. The overall linearity is not influenced by this behaviour and was measured to be larger than 1.8 V for all channels.

3.2 Dynamic range

To characterize the performance of the chip, defined charge signals are injected into the input stages and the corresponding output signals of the channels are measured. The dynamic range of the analog channel was determined by injecting charges ranging from 40 fC to 220 pC for different configuration settings of the channel. Figure 4 shows a linearity measurement for a signal shaping time of 100 ns and a input bias DAC value of 255. The different channel configurations have only a small influence on the output linearity. For all chip configurations a total dynamic range spanning from 40 fC to 220 pC has been determined with a maximum integral non-linearity (INL) value of $\pm 2.1\%$ FSR. The lower end of the dynamic range is determined by electronic noise. For a detector capacitance of 40 pF an equivalent noise charge (ENC) of $25000e^-$ has been measured. If we consider a typical SiPM sensor with a gain of 2.75×10^5 the resulting signal to noise ratio is thus expected to be larger than 10 for single pixel signals with a charge of 44 fC.

3.3 Trigger jitter and efficiency

A high precision of the trigger is important if the timing information of events in the calorimeter is used in the reconstruction algorithms. To characterize the performance of the trigger, a signal charge of 660 fC corresponding to the signal of a minimum ionizing particle (MIP), detected with

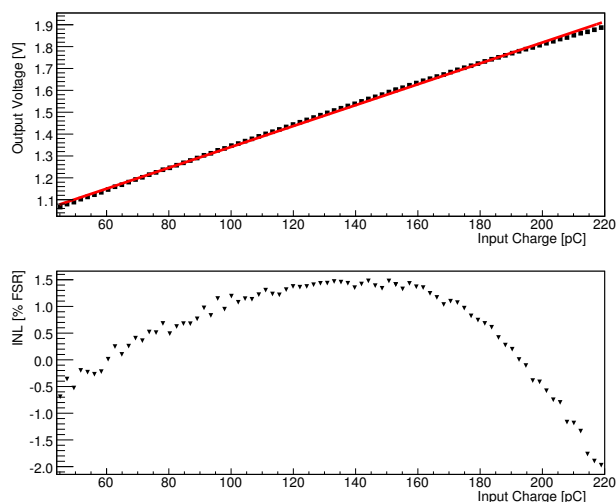


Figure 4. Signal output amplitude against signal charge for 100ns shaping time and input bias DAC value of 255.

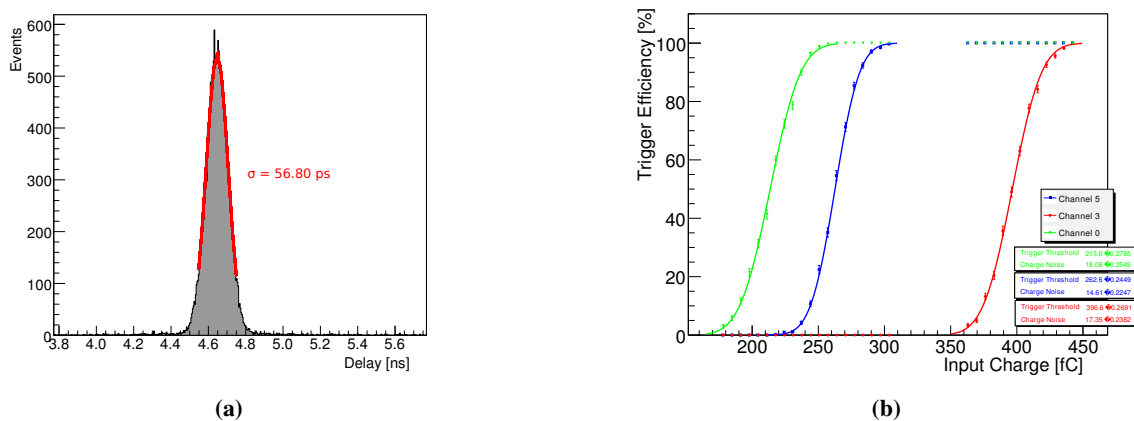


Figure 5. (a) MIP signal timing jitter measurement. (b) Trigger efficiency measurement.

the CALICE prototype described earlier, is injected into the channel using a capacitance of 33 pF. The recorded time difference between the trigger signals of the pulse generator and the KLauS chip is shown in figure 5a. The timing jitter is measured to be 57 ps. This value also includes the jitter from the pulse generator trigger signal which was measured to be 20 ps. The low trigger jitter makes the chip a good candidate for experiments requiring precise timing information.

For the characterization measurements the trigger threshold is generated globally, causing variations in the threshold levels of the individual channels due to the voltage distribution on the PCB. These variations do not occur if the threshold is individually generated for each channel. Figure 5b shows the trigger efficiency for three different channels with the trigger threshold of channel 5 set to 260 fC. The threshold level and the charge noise can be determined by fitting an error function to the measured efficiencies. For all channels a charge noise of less than 18 fC was measured.

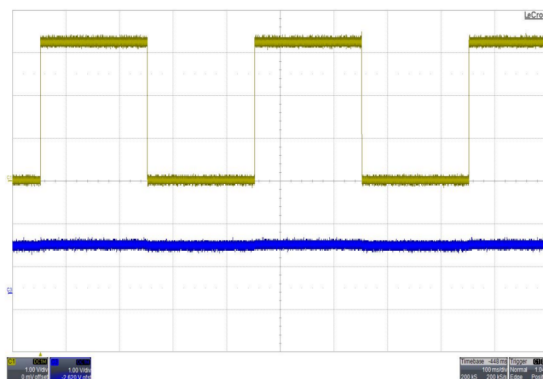


Figure 6. Waveform of the input bias voltage (blue) for a power gating period (yellow).

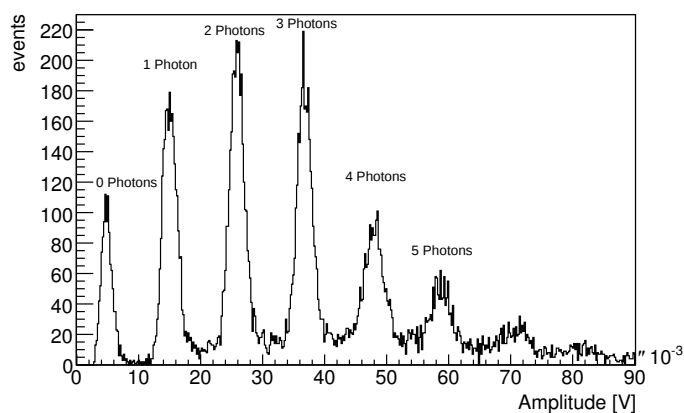


Figure 7. Single photon spectrum using a MPPC S11028-025 recorded with KLauS2v0.

3.4 Power gating

An important feature of the chip is the power gating functionality which can turn off the chip during periods where no events are expected thus reducing the average power consumption significantly. For a duty cycle of 1%, the power gating reduces the power consumption of 2.5 mW/channel to 25 μ W/channel. To ensure the stability of the photo detectors, the voltage at the input bias line has to be kept at the preset value. Figure 6 shows the waveform of the input bias voltage during a power gating cycle. The voltage difference of the input bias between the on and off period was measured to be smaller than 20 mV for all DAC settings, which corresponds to less than 2% of the SiPM bias voltage and is negligible.

3.5 SiPM measurements

Figure 7 shows a single photon spectrum recorded using a Hamamatsu MPPC S11028-025 biased at nominal over voltage. Similar results were obtained for MPPCs from Hamamatsu with larger pixel size and SiPMs produced by CPTA. The individual peaks are clearly separated, which shows that the chip works well under conditions with dark count rates up to 1 MHz.

4 Conclusion

The KLauS2v0 chip provides a low power SiPM readout solution for low gain sensors. The chip has been developed in the $0.35\mu\text{m}$ SiGe technology and has been submitted in November 2010. The characterization measurements show a dynamic range of 220pC and a signal to noise ratio larger than 10. The SiPM bias voltage can be tuned in a total range of 2 V using the bias DAC of the chip. For experiments utilizing the signal timing, a high precision trigger signal is generated with a jitter of 57ps for 660fC signals. Due to the low power design of the analog channel, the total power consumption is less than 2.5mW per channel. A power gating scheme has been implemented which further reduces the consumption to $25\mu\text{W}$ for a duty cycle of 1%.

The characterization shows that all chip parameters fulfill the severe constraints of the AHCAL detector design. The analog channel of the chip is planned to be integrated in the next version of the currently used readout chip SPIROC.

Although developed for the readout of SiPM sensors in the AHCAL detector, the measurements show that the chip is well suited for many experiments requiring low power consumption, high dynamic range and high precision signal timing.

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