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Development of the Readout System for a TPC at the Future Linear Collider

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Abstract

A high resolution TPC is the main option for a central tracking detector at the future International Linear Collider (ILC). The MPGD (Micro Pattern Gas Detector) technology is used to read out a Large Prototype TPC with electronics built for the ALICE experiment and further developed to meet the requirements of the ILC. The first step was to demonstrate that the MPGD readout provides the necessary precision, set by the physics goals of the ILC. Results from beam tests of two GEM systems are presented. The next steps in the electronics development are discussed and the status of the R&D work is given.

1 Introduction

A TPC using MPGD (Micro Pattern Gas Detector) readout with pads, which aims at the high spatial and momentum resolution required to meet the physics challenges expected at the future Linear Collider, will need many rows of pads as small as a few square millimeters. The width of the pads is mainly given by the spread of the charge cloud in the case of GEM:s and by the properties of the resistive layer in the case of MicroMegas. The influence of the pad length on the space resolution and two-track separation has to be given by measurements and simulations. Preliminary results from simulations [1] have shown that the improvement in momentum resolution in going from pads of size 1x6 mm^2 to pixel readout is only marginal. Further simulations as well as measurements at test beams are, however, necessary to determine what pad size is needed to achieve the physics goals of the future Linear Collider. This is an important issue since a large fraction of the cost for the TPC is in the electronics and the pad size has direct implications not only on the cost but also on data rate and power consumption.

This is a summary report on the development work, of the readout electronics for a TPC at the ILD-detector [2], going on in Lund

2 Demonstration phase

The aim of the first phase (EUDET) of the electronics R&D was to provide readout electronics in order to demonstrate the feasibility of the MPGD technology (GEM:s [3] and MicroMegas [4]) with respect to the requirements set by the physics challenges at the future Linear Collider. For proof of principle tests, a Large Prototype (LP) TPC was built by DESY [5], within the framework of the EUDET project. The electronics system set up for the EUDET project provides very flexible test conditions and if tests with really small pads turn out to be necessary the EUDET system should be used also in the future.

3 The ALTRO electronics

In case of the GEM modules the pad readout has been based on the readout electronics that was developed for the ALICE experiment at the CERN LHC, the ALTRO system [6]. The 16 channel ALTRO chip performs analogue to digital conversion with 10-bit resolution followed by various steps of digital signal processing, including zero suppression and storage in an event buffer. The sampling can be clocked at frequencies up to 40 MHz so in principle sampling at this frequency and frequencies lower by multiples of two is possible. However, at 40 MHz sampling the full resolution is not maintained for the standard ALTRO chip. A limited number of ALTRO chips were modified to allow sampling at 40 MHz with almost full precision [7]. Up to now the system has been operated at 20 MHz only. The ALTRO chip has an event storage memory of 1 k 10-bit words per channel, which corresponds to sampled data over a depth of 50 μs drift time at 20 MHz sampling frequency. The so called T2K gas mixture (95/3/2 % Ar/CF4/Isobutan) was used in the TPC, which gives a drift velocity of around 7 $cm/\mu s$ at a drift field of 230 V/cm. This leads to a maximum allowed drift length of 350 cm that can be accommodated on the ALTRO memory i.e. much longer than the total length of the LP-TPC of 60 cm.

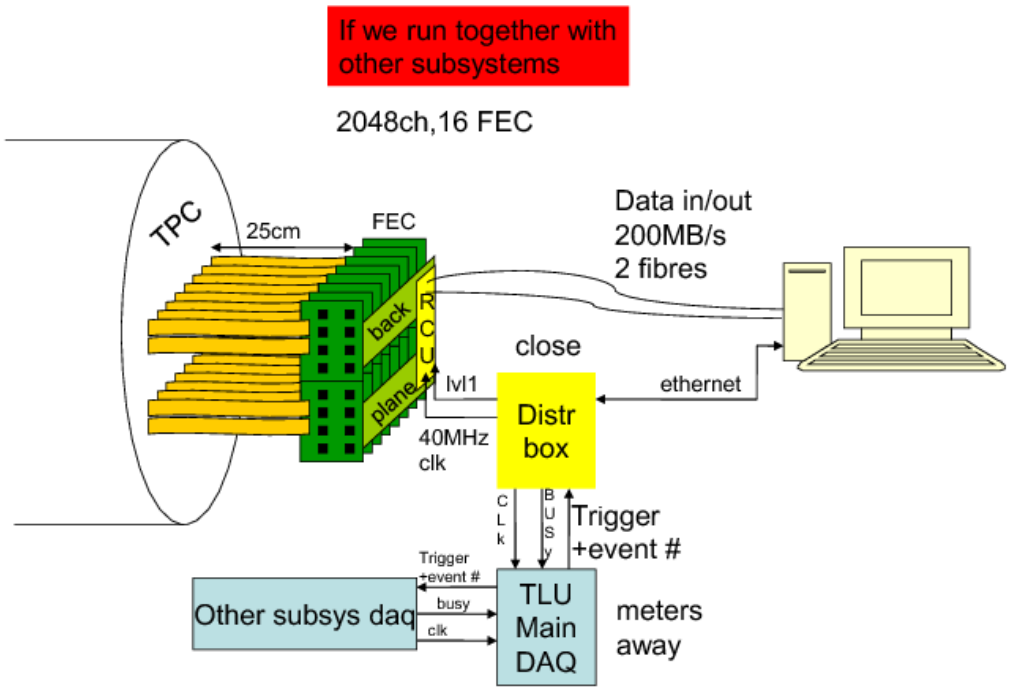

Figure 1: Schematic layout of the present readout system with the ALTRO electronics

3.1 The PCA16 charge sensitive preamplifier

In order to test recent technologies for gas amplification a new charge sensitive preamp-shaper (PCA16) has been developed [8]. The programmable PCA16 chip has, as the name indicates, 16 channels and offers different choices with respect to shaping time (30, 60, 90, 120 ns), gain (12, 15, 19, 27 mV/fC), decay time and signal polarity. The new analogue chip required modifications to the Front End Card (FEC), compared to its original design for the ALICE TPC. These are mainly related to the programmability of the PCA16 chip which is done remotely. Data for setting the parameter values are downloaded to the board controller FPGA on the FEC via the data bus on the back plane. An 8-bit shift register delivers the digital input to set the peaking time, the gain, the polarity (common to the 8 PCA16 chips on a FEC) and it also provides a possibility to bypass the shaping function. An octal Digital to Analogue Converter (DAC) controls the decay time of the preamplifier.

Each FEC contains 128 channels i.e. 8 PCA16 chips and 8 ALTRO chips are mounted on each board. They are connected to the pad board on the TPC via flexible 30 cm long Kapton cables. Fig. 1 shows a schematic view of the front end electronics and the DAQ system.

3.2 The DAQ system

The ALTRO-electronics has been designed to operate in the LHC environment where the clock is provided by LHC. In order to circumvent this, a Trigger Logic Unit (TLU) has been developed [9] to provide trigger and timing control. The TLU constitutes the central trigger unit for all sub-detectors

in a beam set-up and includes an event synchronization mechanism by a distributed event sequence number. In the case of the LP-TPC a distribution box (DBOX) [10] receives the trigger from the TLU and sends it via the RCU to the FEC's. The DBOX either takes the trigger from the Trigger Logic Unit (TLU) or from a local NIM trigger system, which is also used for operation in stand alone mode. So far the TPC has only been operated in a stand alone mode, and with a local clock generator.

A Readout Control Unit (RCU) [11] governs the readout of the data via the back plane to which a maximum of 32 FEC's can be inserted. Data are sent via an optical cable to a Detector Read-Out Receiver Card (DRORC), which is placed in the Data Acquisition (DAQ) PC. The DAQ software uses the ALICE drivers and libraries for communication between the DRORC and the front end electronics via the optical link. At the reception of the Level-1 trigger the ALTRO starts storing digitized information in the event buffer, up to a predefined number of samples. The RCU reads the ALTRO event buffer and sends the data on the optical link to the DRORC, which stores it in the memory of the readout computer. At the arrival of a trigger in the DBOX, it defines a time stamp of the event that is used to synchronize it with events from other detectors. The run control is done from a graphical user interface. A monitor program creates and updates histograms in a shared memory, which is also accessible from a presenter program.

4 Performance

The electronics pedestal and noise levels for all readout channels have been measured both initially as well as on a regular basis during data taking periods, mainly for pedestal subtraction and to check whether there are corrupt channels. The front end electronics has shown excellent noise performance. A typical measurement with the PCA16 chip programmed to provide the longest peaking time (120 ns) and the lowest gain (12 mV/fC) gives an average RMS value of around 0.5 ADC counts corresponds to the equivalent noise of 520 electrons, which includes random noise, coherent clock noise and long term variations on the scale of seconds. If the gain is increased to the highest value (27 mV/fC) the noise level increases to typically about 1 ADC count, which corresponds to the equivalent noise of 462 electrons at this gain. It should be noted that the noise limiting factor is the long Kapton cables for signal input. Without the Kapton cables connected, the ADC resolution of 1.2 mV per channel is not good enough to measure the RMS noise.

The ALTRO readout boards for a total of 10.000 channels have been produced, tested and taken into operation. For the Low Voltage (LV) supply a commercial system from Delta Elektronika has been used.

5 Test results

Measurements have been performed at the DESY test beam T24, which provides electrons of maximum 6 GeV. Two different GEM-systems have been tested, one with two GEM-layers, prepared by the Asian groups [12] and one with three, produced by the DESY group [13].

Analyses of data from test beam measurements, using the LP-TPC equipped with the two layer GEM system and pad sizes of approximately 1.1x5.26 mm^2, have been performed [14]. The analyses revealed inhomogeneities of the electric field, caused by the support structure along the long borders of the GEM module, leading to distortions of the recorded tracks. These distortions were corrected for by using the Millepede program package [15]. During the run the position of the beam was kept fixed

and thus the impact position to the TPC was the same within the beam spread. Millipede makes a least square fit of all measured tracks simultaneously. After these corrections have been applied the residuals line up around zero.

In Fig. 2 (top), the measured space resolution in the direction of the electron drift (z-direction), determined from a fit to the rising edge of the pulse, is plotted as a function of the drift distance for different shaping times. It is shown that the resolution improves with decreasing shaping time until it reaches 60 ns. For smaller shaping times (30 ns) it gets worse, the reason for which is the sampling rate of 20 MHz, which doesn't give enough samples on the rising pulse to determine the front edge accurately. Extrapolating the measurement at 60 ns shaping time to the full drift length of the final ILD-TPC (2.15 m) gives a resolution of $\sigma_z(2150) = 446 \pm 9$ μm meeting the final goal of 500 μm. Fig. 2 (bottom) shows the space resolution versus drift distance in the bend plane. A fit to the data points results in an intrinsic resolution $\sigma_y(0) = 59.1 \pm 0.4$ μm. The measurement was performed at a magnetic field of 1 T whereas the magnetic field foreseen for the ILD-TPC will be 3.5 T. Theoretical calculation have shown that the space resolution as a function of drift distance at this field is essentially flat so that the result obtained is in accordance with the goal of ≤ 100 μm.

A three layer GEM detector used a new support structure for the GEM:s consisting of ceramic frames and spacers to provide a mechanically stable and compact system. The pad plane had an active area of approximately 40x170 mm^2. This had pads of size 1.26x5.85 mm^2 organized in a central road with an approximate width of 4 cm right through the module. In the outer areas 8 pads were combined to make bigger effective pads of around 5x11 mm^2 . Fig. 3 shows the integrated pulse height distribution over the pads caused by straight tracks through the central part of the module. At the ends some distortions can be observed, which are due to a transverse electric field component close to the boarders of the module. This is caused by the gap between the pad module and the neighboring dummy modules.

6 The electronic adaption phase (consolidation phase)

The overall design goal with the next prototype step (AIDA) is to demonstrate that a system can be built so that a final system with the required performance can be constructed. It should work as a demonstrator which shall address all expected difficulties and limitations. The subsequent design phase prototype will be a full scale prototype and this will require substantial funding. The compromises relative to a final system shall be understandable and possible to describe to technical and financial evaluation committees in a convincing way.

The main goal of this prototype step is to bring the system as close as possible to a final design with regards to the electronics placed on the TPC backplane. Originally the defined goal of the AIDA phase R&D was to minimize and organize the electronics components such that their density should be compatible with a pad size of 1x6 mm^2. While the size of the newly developed SALTRO16 chip is compatible with this goal (see below), the area taken by the backframe, the HV-connectors and the cooling system also has to be taken into account. In doing this it turns out that the electronics components have to be mounted extremely tight in order to meet this space requirement. However, since already the first phase prototype demonstrated that the MPGD technologies are able to provide the required space resolutions, the focus of the second phase prototype was reconsidered to be:

- Aiming for a realistic pad size without hazarding the functionality of the electronics.

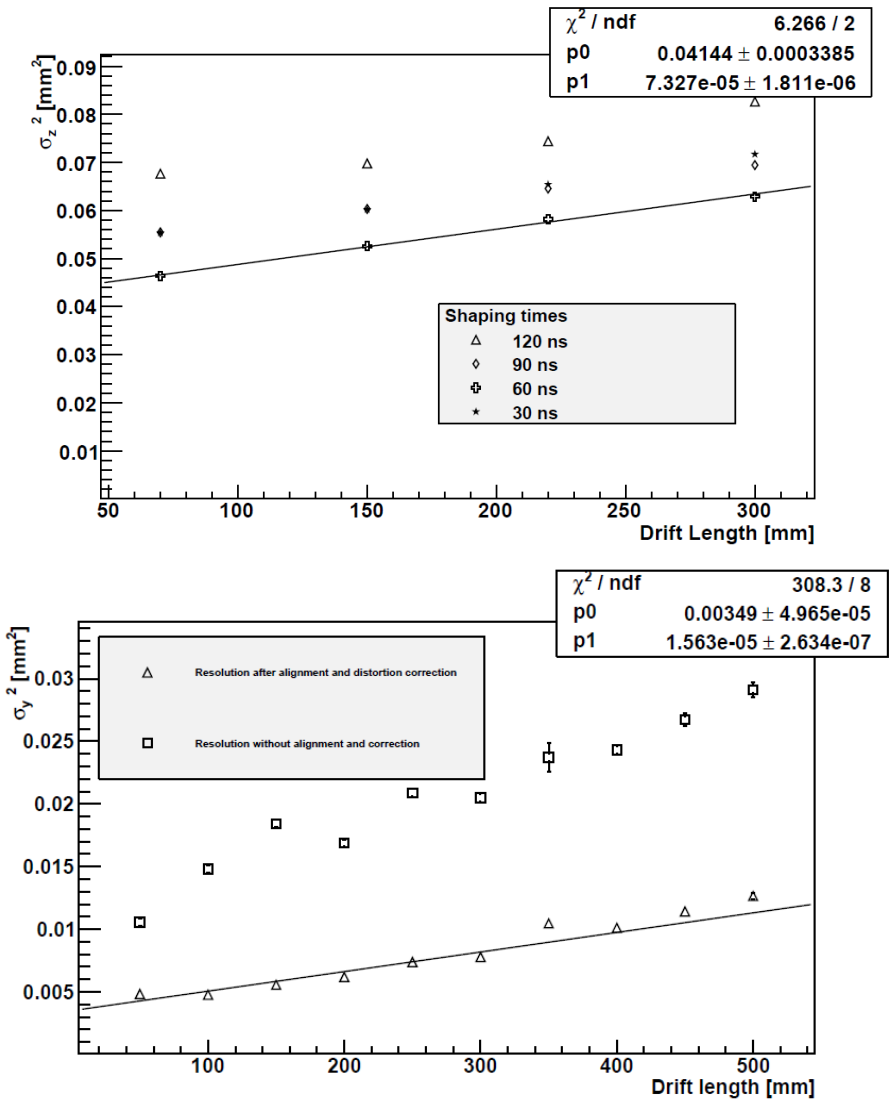

Figure 2: Squared z-resolution plotted against drift length for four different shaping times (top). Bend plane resolution squared as a function of drift length (bottom). The situation before as well as after alignment and distortion correction has been applied is shown.

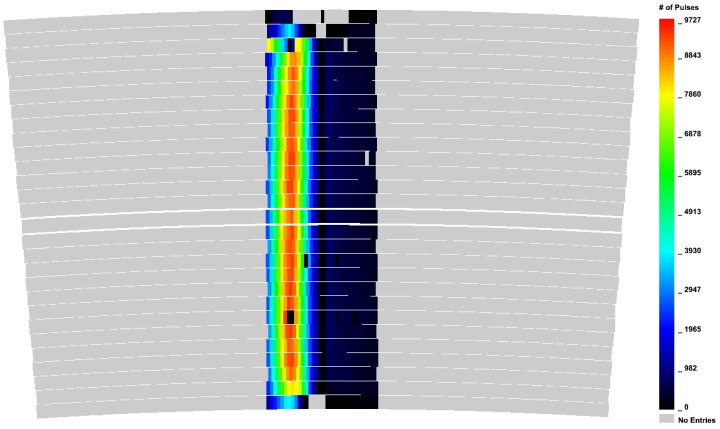

Figure 3: Integrated pulse height distributions plotted against pad row for straight tracks.

- Testing power pulsing.
- Studying cooling issues and developing a prototype for the final cooling system.
- Being as realistic as possible in terms of electronic noise.
- Providing enough experience for a safe input to the final solution.

One improvement compared to the EUDET system is that the long Kapton cables are not needed. This means a significant reduction of the input capacitance and consequently a noise reduction. The noise level in the EUDET system is very low and it is clear that the limiting factor with regards to sensitivity in the electronics system is the long cables and there are improvements to expect when the Kapton cables are not needed.

The noise level in the readout electronics may limit the performance in momentum resolution both by its effect on the amplitude resolution and the sensitivity (threshold). The amplitude resolution affects the coordinate resolution and thus the momentum resolution. This is likely to be a small problem as the pads are narrow and due to the large number of coordinates measured along a track. Instead it may turn out that the highest possible sensitivity (lowest possible number of input electrons) is most important as it relaxes the need for high avalanche gain. This in turn reduces the number of produced positive ions, which may drift back into the drift volume and distort the track images. Thus, the sensitivity of the readout electronics is likely to be more important for the ILD-TPC performance than for systems where one can compensate loss of sensitivity in the electronics, e.g. due to high noise level, by increased avalanche gain.

Thus, the sensitivity of the system remains to be demonstrated and the optimal solution in this respect is involved in this prototype step.

6.1 The SALTRO16 electronics

The development of readout electronics for the second phase is based on the, by CERN, newly developed SALTRO16 chip [16], which combines the analogue and digital signal processing of the incoming information. This essentially means that the functions of the PCA16 preamp and the ALTRO chips have been integrated into one chip, mainly to save space. The SALTRO16 silicon die itself is 8.7x6.2 mm^2 and contains 16 readout channels which equal 2.625 mm^2 per channel. There are only small differences in the functionality of the SALTRO16 compared to the EUDET version of the electronics where the PCA16 and ALTRO chips are separate. One important difference is, however, that the new chip can be turned off when no signals are expected, which reduces the power consumption and demands for cooling drastically.

The integration of the PCA16 with the ALTRO in the same chip does not, in itself, provide a large enough area saving. The main reduction is achieved by using the most modern techniques for circuit assembly. In almost all aspects it means to stretch the techniques beyond what is used in industrialised manufacturing today. Thus, the development has to be done in close cooperation with industry.

The major complication arise from the fact that the SALTRO16 dies are delivered untested. Further restrictions are due to the cost and availability of the chips, and that the yield is unknown. The alternative of using packaged chips is not a realistic choice since it requires too much space on the pad board in order to give small enough pad sizes, although testing, mounting and service would be simpler. Due to the uncertainty in the yield it is unrealistic to assemble untested dies directly on

a pad module with the requirement that all chips should work. Instead the chips will be mounted on carrier boards, only slightly bigger than the chips themselves, which simplifies the handling and enables tests of individual chips. Eight of these carrier boards will then be mounted on a so called Multi Chip Module (MCM), which essentially will correspond to a FEC in the old ALICE system.

The advantages in placing the electronics components on separate boards, compared to soldering them directly onto the pad board, are listed below.

- Trace routing from the pads to the SALTRO chip becomes simpler since translational routing will essentially only be necessary at the edges of the pad module.
- With fewer or no active electronics components on the pad board it will be easier to design.
- Changes during the electronics prototyping will be cheaper and easier to implement and test.
- The interface between the SALTRO-part and the controller/readout-part is well defined.
- The trace routing on the plug-in board will be easier compared to the trace routing in case all the electronics components are placed directly on the pad board. The pad board will need less layers.
- It moves heat away from the TPC endplate.
- It facilitates service. A malfunction in the readout chain can easily be fixed by replacing the electronics board instead of dismounting the whole pad board.

In a final production step, the dies must be tested directly on the wafer and then the assembly will be much more like a standard assembly and even smaller size is possible by either bonding the chips directly to the MCM-board without carrier boards or mounting by chip-flip technology. Together with an integration of more channels per chip (64 or 128) a further miniaturization of at least a factor 2 is expected.

6.2 The carrier board

The naked chips will be mounted on small carrier boards, which enable testing before mounting and simultaneously meet the areal constraints. The size of the carrier boards is 12.0x8.9 mm^2, which also includes space for bonding wires and some passive components. The layout of the carrier board is shown in Fig. 4. Eight of these carrier boards are mounted on so called Multi Chip Modules (MCM), which will be connected to the pad board.

The signals from pads are brought to the preamp input of the SALTRO16 chip, via 4 micro-connectors of type Panasonic P4S, which have a lead pitch of 0.4 mm and a mated height of 3 mm. These connectors are offered with either 42 or 60 leads. The connectors have to be mounted with very high precision on the pad board and on the carrier board since four such connectors have to fit simultaneously and the space between the MCM boards is very small.

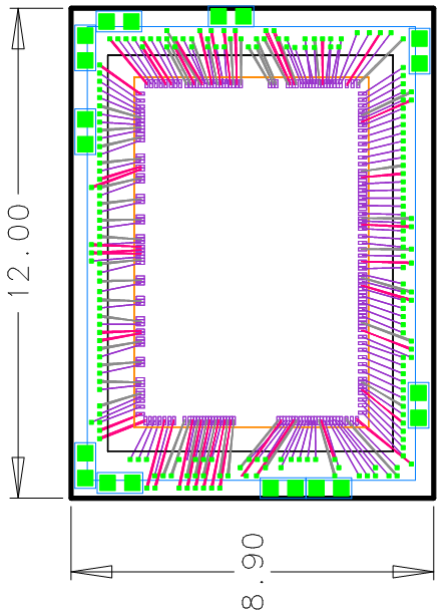

Figure 4: Layout of the carrier board with bonding wires and passive components.

6.3 The MCM-boad

The carrier boards are mounted onto the MCM-boards by soldering of small tin balls on the back side of the carrier board, organized in a so called BGA foot-print. Fig. 5 shows a schematic draft of an MCM-board. In order to meet the areal constraints, the carrier boards have to be mounted on both sides of the MCM-board. That is possible since the Panasonic connectors are elevating the MCM-board by 3 mm above the pad board, which thus leaves enough space for components on both sides of the MCM-board. In Fig. 5 the rectangles with a dot-matrix of 20x13 dots are 8 sets of BGA patterns (4 on each side) for the SALTRO carrier boards. These boards are placed in each corner of the MCM-board such that the analogue inputs are facing outwards towards the long edges of the MCM-board, the bottom side of which the four 42-pin connectors for the 32 input signals (plus grounds) also are placed. The digital signals are concentrated towards the centre of the board. In the centrally placed square of the MCM top side, the BGA footprint of a CPLD (Complex Programmable Logic Device) is seen, which has an area of only 8x8 mm^2 (for details see below). The two centrally placed 60-pin connectors on the top side are place holders for the HDMI connector and the LV connections. The LV may use many pins in such a connector. The final design of this is yet to be completed.

Proper design rules from the bonding company have been followed and the external components are of the smallest outline version. The dimensions of the MCM-board are 32.5x25 mm^2, which means a drastic reduction by about a factor 40, in physical size, of the readout electronics compared to the 17x18.5 cm^2 for the EUDET FEC readout card. Within this area the MCM-board contains the following main components in the present design:

- 8 Saltro16 chips mounted on carrier cards which are BGA bonded to the MCM-board.
- 1 CPLD LCMX02-400 csBGA132.
- TMP101 temperature sensor (I2C interface).
- ALTRO bus between SALTRO's and CPLD.

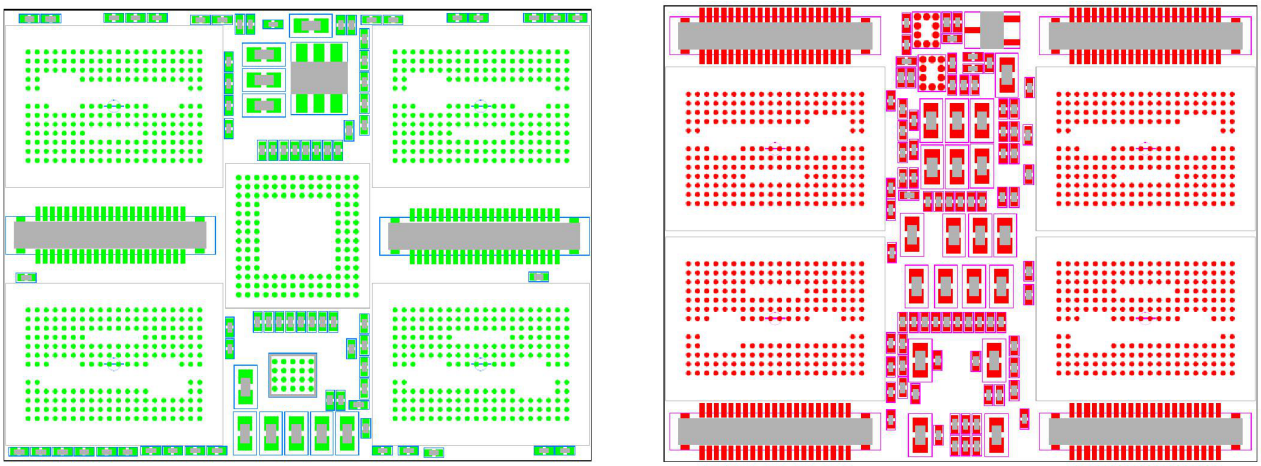

Figure 5: The MCM-board top surface (left, green) and bottom surface (right, red)

- 1 microHDMI connector.
- DAC (MAX5825 with I2C interface) for setting PCA16 decay time.
- Four multi-pin connectors to pad plane.
- LV connector for 5 voltages and one ground.
- 1 LM4040 Voltage reference.
- 3 MAX4233 Analog voltage buffer.

Fig. 6 shows a side view of the board assembly on the pad plane with the SALTRO16 chips marked in black sitting on the carrier boards, marked in dark green, which in turn are placed on the MCM board, marked in light green. The Panasonic and HDMI connectors are marked in orange, of which the higher one is the microHDMI connector. Some other major components are marked in light grey. This gives an impression how much space is left for the cooling system.

An MCM serves 128 channels and logically it corresponds to a FEC in the EUDET system architecture.

The design presented here is a challenge. It has very good features like the direct connection to the pads without cables which is very good for the noise level. The SALTRO16 chip mixes analogue and digital in the same silicon die, and the readout and control of the SALTRO's are placed close to the chips on the MCM-board. Analogue and digital signals are well separated on the MCM-board but because of the small size they are still close. Small size with good local grounding can also be a good feature in terms of noise. It is difficult to estimate at this stage which effect will be the most dominating.

6.4 The readout mode

In the EUDET ALTRO-system the readout of the FEC's is done via backplanes with a 40 bit wide parallel, bidirectional data bus, and for control signals. This follows the readout architecture of the ALTRO chip. The backplane provided readout of maximum 16 FEC's, one after the other, with 2 branches read out in parallel, controlled by an RCU, as described in section 3.2. The SALTRO16 chip

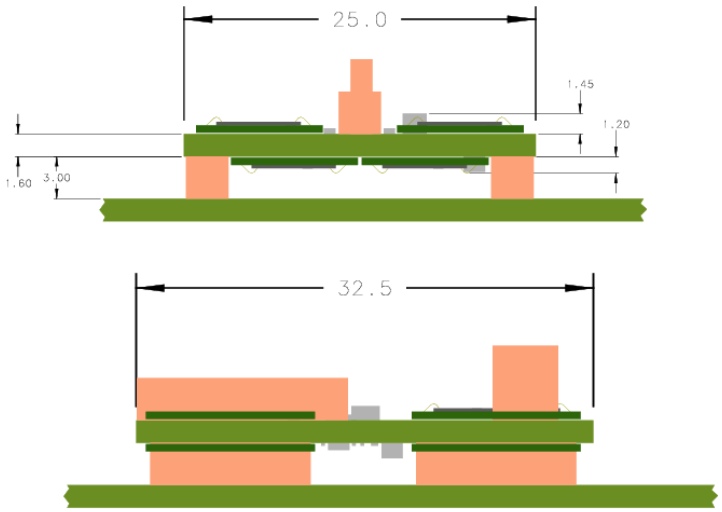

Figure 6: A schematic sideview of the board assembly.

has the same output as the ALTRO chip but a readout using the 40 bit parallel backplane architecture is more or less impossible for a number of reasons.

The main disadvantages are:

- Due to the small size of the MCMs, connectors to the backplane are excluded.
- Horisontally mounted MCMs gives difficult assembly with large backplane. The backplane would cover essentially the full area of the pad module, which would have consequences for the cooling.
- It would be very inflexible.
- The solution would be far from the final system which will have point to point readout via high speed serial transfer.

Although keeping the old readout architecture would mean less new development we find it necessary to introduce a point to point readout already at this stage. Such an alternative has been made possible by the recent development of FPGA's or CPLD's operating in the Gigabit per second range. This is the option that will be discussed below.

6.5 The CPLD

The heart of the readout system on the MCM is the CPLD chip. It takes over the role to handle the ALTRO bus in the EUDET system, which is now internal to the MCM only. In the EUDET readout system the RCU had the role of the ALTRO bus master and since this bus was shared by up to 32 frontend cards with the limitation to 8 chips on one and the same frontend card, the CPLD offers a substantial simplification.

There are only four types of communication between the DAQ and the individual channel of an SALTRO chip.

- Send a command.
- Write data to a register.
- Read data from a register.
- Read the data of an event.

Most of these operations are concurrent during data taking and the control of the operations is handled via the serial link. Other controls on the MCM don't involve the ALTRO-bus but should be controlled by the CPLD and the serial communication. These operations include:

- The 8 bits for configuring the SALTRO16 preamp/shaper.
- Serial control of the DAC to set the decay time.
- I2C communication with the temperature sensor and other sensors.
- Controlling the power pulsing of the SALTRO chip.
- Sending error and status messages to the DAQ.

This input will correspond to registers in the CPLD. The communications to/from these registers can be via a separate I2C bus or via the main serial data transfer or a mixture thereof. For a final choice further input is needed. It will in any case be necessary to have an I2C communication to the MCM for programming the CPLD chip.

7 Readout of a panel

It is very hard to make the present MCM-board smaller and if it has to be made larger it will be at the expense of the number that fits within a pad panel, which in turn directly influences the pad size if the full panel is to be equipped with readout pads. Fig. 7 shows how a pad panel with 25 MCM:s are arranged in a 5x5 matrix i.e. they contain 3200 channels in total. This leads to pad sizes of about 1x8.5 mm^2. This layout has been judged to give sufficient room for cooling and HV connections. Most likely, a final solution will have to leave about the same area of a pad panel for HV, cooling and other services. So, to fit the readout electronics inside a 17.0x13.0 cm^2 rectangle is a reasonable design goal also for the final system and to place the MCM-boards in regular rows and columns to simplify the construction of the cooling system.

8 The DAQ system

For the readout and communication to the DAQ several concepts have been under consideration. The most attractive option is to use the serial readout of the MCM. The functionality needed locally in the vicinity of the MCM-board is the serial to parallel conversion of the downloaded data and the parallel to serial conversion of the uploaded (readout) data. This can be accomplished by a CPLD chip and there are chips which seem to have enough logic gates to serve the purpose and which should fit on the MCM itself, thus making the front end electronics on a single board using only a microHDMI cable

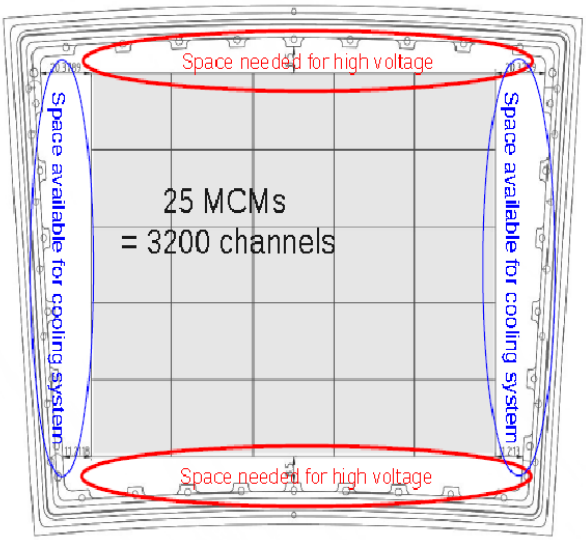

Figure 7: The layout of the MCM-boards on a pad module with spaces for HV connectors and cooling indicated.

as external communication line plus LV supply from a separate LV distribution card with the voltage regulators. This alternative would mean the most realistic step forward towards a final system. The use of an FPGA or a CPLD is not a big design issue and in a final solution either may be feasible. Here, the areal constraints favour the CPLD so that the construction can be done on a double sided circuit board, as shown in Fig. 5, which is likely to be similar to the final solution.

8.1 Serial readout

A lot of work is going on in the HEP community aiming for serial high speed readout e.g. for the LHC upgrades. Much of this has become possible with the development of a new generation of FPGA's that provide serial interfaces supporting data rates of several Gbit per second. A rather general purpose serial connection suitable for many experiments uses 4 LVDS signals (clock, trigger, data out and data in) communicated via cables like HDMI, microHDMI or Ethernet (RJ45), frequently used in consumer electronics. A general solution to this task is the Scalable Readout System (SRS) [17] developed for the purpose of detector R&D in the laboratory but scalable to be suitable also for readout of several 10 k channels. The system has been developed within the RD51 collaboration but it is intended also for a broader use where the hardware shall become available from the CERN stores. The SRS system contains the SRU (Scalable Readout Unit), the core of which is a powerful FPGA. The system includes the usual collider timing and trigger system with distribution of clocks and triggers. One of the main advantages with the SRS system is that it is very adaptable to future changes and developments of the DAQ in LCTPC and possibly the whole ILD-collaboration. In the most attractive solution, shown in Fig. 8, the MCM and the SRU communicate directly via the Data Trigger Control (DTC) link. However, this requires that the FPGA firmware on the SRU is modified to include also the customized communication to and from the MCM. This can be done and the ALICE EmCal has developed a system like this for point to point readout of the EmCal modules to the SRU.

Since the ALICE EmCal also uses the ALTRO chip one has solved the SERDES (serializer-deserializer) conversion of data as communicated via the ALTRO bus. How much one could benefit from that work is not evident as it had the constraint that the hardware of the front end card could not be changed,

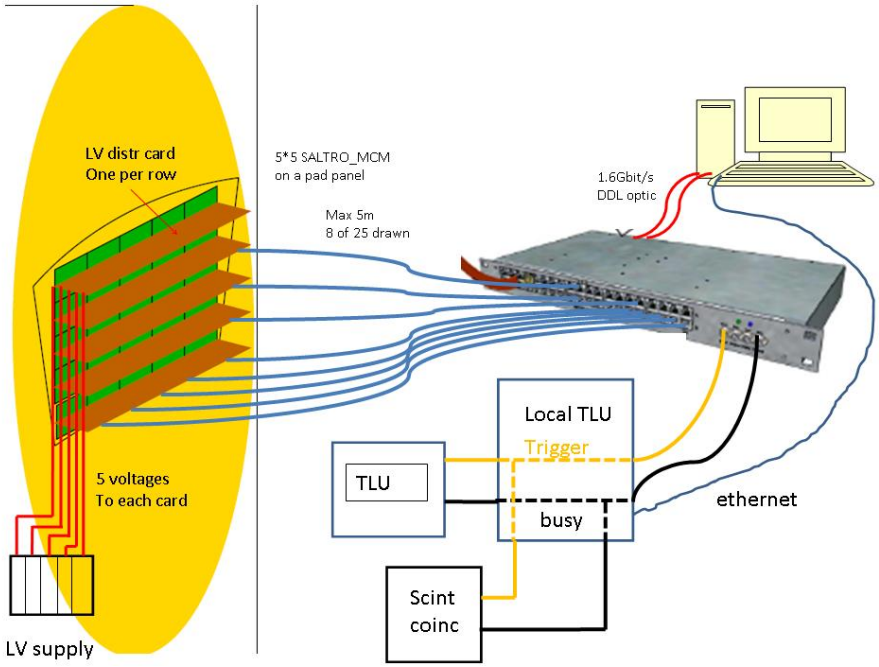

Figure 8: Schematic view of a serial readout system where an MCM-board communicates directly with the SRU via an interface card, which provides a transfer between the microHDMI and RJ45 cables.

A drawback with this solution is that the RJ45 cabling is too bulky for the small MCM-boards. One would at some point need to go from RJ45 cables to microHDMI. This is not a big problem but it has to be kept in mind. This interface card would then also be the place to mix in the I2C controls (see Fig. 8). Another drawback is that the maintenance of the user SRU specific firmware has to be done by the group itself and one thus loose the advantage of being able to use a general purpose readout.

One SRU could handle 40 MCM's. Five SRU's would be more than sufficient to handle all the channels of the seven LP-TPC modules, each having 5 MCM-boards. The DTC protocol uses the four pairs of leads in the RJ45 cable for the fast signals. Slow control data have to be coded into the high speed data and translated on the MCM or provided by a separate system.

The solution reading the MCM-boards directly to the SRU is the cheapest as it uses the least new hardware. If the system shall read only the MCM-boards on the TPC this may be the most convenient solution. The baseline solution of the SRS system is to have an intermediate module called SRS-FEC between the SRU and the user front end. The SRS-FEC can be equipped with plug-in cards which can add user functionality to the readout chain without interfering with the DAQ FPGA's. This solution is more adaptable and allows data to be collected from different detectors.

9 Communication with the SALTRO16 via the ALTRO-bus

All ALTRO-bus operations, except reading data, imply moving 20 bits of data to/from a register. Together with addresses for register number, channel number and chip number such an operation transfers a 40-bit word in parallel between the CPLD and the SALTRO16 chip. In addition to the 40 bits aimed for the SALTRO16 chip, four bits are added as an action code by which the CPLD can direct the data to different operations depending on which type of communication that is referred to. These operations are used to configure the preamp/shaper in the SALTRO.

9.1 Event data readout

The readout sequence means a local transfer of 40-bit words from the SALTRO16 chip to the CPLD via the ALTRO-bus. If the readout clock runs at 40 MHz the SALTRO16 chip would send 1.6 Gbit data per second to the CPLD. However, the upper limit at which the CPLD can send and accept data via the serial link is 400 Mbit per second. Two possible solutions are to either reduce the frequency of the readout clock or to allow sufficient buffer storage in the CPLD to contain the maximum number of bits from a readout channel i.e. about 10 kbit.

9.2 Clocks and triggers

The serial communication includes one LVDS line for clock (reference clock) provided by the SRU, and one for trigger. The reference clock is likely to run at 40 MHz. In the CPLD the reference clock frequency is divided down to the desired sampling clock frequency, likely to run at 20 MHz, and the readout clock frequency of 40 MHz. The CPLD has PLL:s (Phase-locked Loop) to maintain the phase of the clocks.

An event trigger asserts an Level-1 trigger and this is followed up by an Level-2 signal if the sampled data is supposed to be kept. These data should be sent on the trigger line in the serial transfer and they should arrive at the SALTRO16 chip within a minimal and constant delay compared to the time when the physics event occurred. Since the Level-1 and Level-2 are sent on the same line they have to be coded for recognition.

New triggers are not accepted during the time that data are read out, as the readout clock would induce coherent noise on the amplifier output.

9.3 Further signal communication between the SALTRO16 chip and the CPLD

The preamp/shaper within the SALTRO16 chip is programmable with respect to the choise of polarity, gain, shaping time and the decay time of the preamplifier. In total 8 DC signals are needed for the first three options whereas the decay time is controlled by an analogue voltage from a DAC. The CPLD can provide the appropriate DC levels as it has different power domains, where each domain can be set to individuaul analogue supply voltages. The DAC could be controlled by the built in I2C interface.

9.4 Slow control on the I2C

The MCM needs to have temperature sensors. It would also be useful to monitor the currents drawn by the circuit. This has to be done on the LV distribution board. In addition the power pulsing will be done on the LV board. These features can be controlled locally using the I2C of the CPLD and the communication with the I2C registers in the CPLD would go through the serial system like normal writing and reading to/from the SALTRO16 chip. The programming of the CPLD, however, requires an external access, which can be provided by the microHDMI cable through connection to the CPLD internal I2C. In case of malfunction of the I2C or the DAQ there should be an emergency switch off, triggered by the temperatur sensors as the chip temperatures are getting too high.

10 Summary

A possible readout system for the front end electronics, based on the SALTRO16 chip, has been proposed, with some alternative solutions, which have to be decided upon in the near future. The design of a small carrier board to house the SALTRO16 dies has been completed and the boards have been ordered. The size and component placement of the MCM-board (Multi Chip Module) have been fixed and the layout is ongoing. Two options for serial readout are being discussed and a decision on which to choose will be taken this year. First ideas on the LV (Low Voltage) supply board have been discussed but the design has not yet started. The cooling system, which is the responsibility of the Japanese groups, have been discussed and some simulations have been performed.

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