AIDA-CONF-2015-006

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Advanced European Infrastructures for Detectors at Accelerators

Conference Contribution

Front-end electronics and readout system for the ILD TPC

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25 November 2014

The research leading to these results has received funding from the European Commission under the FP7 Research Infrastructures project AIDA, grant agreement no. 262025.

This work is part of AIDA Work Package **9: Advanced infrastructures for detector R&D**.

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Front-end electronics and readout system for the ILD TPC

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ABSTRACT: A high resolution TPC is the main option for a central tracking detector at the future International Linear Collider (ILC). It is planned that the MPGD (Micro Pattern Gas Detector) technology will be used for the readout. A Large Prototype TPC at DESY has been used to test the performance of MPGDs in an electron beam of energies up to 6 GeV. The first step in the technology development was to demonstrate that the MPGDs are able to achieve the necessary performance set by the goals of ILC. For this 'proof of principle' phase, the ALTRO front-end electronics from the ALICE TPC was used, modified to adapt to MPGD readout. The proof of principle has been verified and at present further improvement of the MPGD technology is going on, using the same readout electronics. The next step is the 'feasibility phase', which aims at producing front-end electronics comparable in size (few mm^2) to the readout pads of the TPC. This development work is based on the succeeding SALTRO16 chip, which combines the analogue and digital signal processing in the same chip. This paper summarizes the status of this work and discusses how the experiences made so far can be exploited to improve the final readout electronics.

KEYWORDS: TPC; MPGD; ILC.

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1. Introduction

A Time Projection Chamber (TPC) is a candidate for the central tracker of the future International Linear Collider (ILC) detectors. TPCs have already demonstrated very good performance in past collider experiments. In order to obtain one order of magnitude improvement in momentum resolution and the highest possible track recognition efficiency, the Linear Collider TPC (LCTPC) Collaboration is pursuing R&D activities to find the best state-of-the-art technology for the TPC. The TPC will have a diameter of 3.6 m and a length of 4.3 m. It should provide 200 space points with pad readout along a particle track, with a spatial resolution of 100 μm in the Rϕ plane. To achieve these performances, a TPC equipped with Micro Pattern Gaseous Detectors (MPGD) instead of Multiwire Proportional Chambers (MWPC) is needed. Therefore the LCTPC Collaboration has built a large TPC prototype (LPTPC), with a diameter of 750 mm and a length of 600 mm, which can be equipped with Micromegas or GEMs as amplification structures. Since 2008, the LPTPC has been exposed many weeks to an electron beam of up to 6 GeV at DESY, in presence of a magnetic field of up to 1.0 Tesla [1]. The first step in the technology development was to demonstrate that the MPGDs are able to achieve the necessary performance set by the goals of ILC. For this 'proof of principle' phase, the ALTRO [2] front-end electronics from the ALICE TPC was used, modified to adapt to MPGD readout. The proof of principle has been verified and at present further improvement of the MPGD technology is going on, using the same readout electronics. The next step is the 'feasibility phase', which aims at producing front-end electronics comparable in size (few mm^2) to the readout pads of the TPC. This development work is based on the succeeding SALTRO16 chip [3], which combines the analogue and digital signal processing in the same chip. This paper summarizes the status of this work and discusses how the experiences made so far can be exploited to improve the final readout electronics.

2. The SALTRO16 LPTPC readout system

The anode endplate of the LPTPC has been designed such that amplification modules can be mounted in a pattern that corresponds to a circular subsection of a possible TPC endplate for a Linear Collider. The endplate of the large prototype allows to accommodate up to 7 GEM modules, with an accuracy better than 50 μm. The SALTRO16 readout system for the LPTPC detector is schematically shown in Figure 1 for one pad module. The pad module consists of a double or triple GEM structure mounted 2 mm above a pad plane consisting of 3200 pads of 1.0 x 8.5 mm^2. One of the goals of this prototyping phase is to achieve a significant reduction in size of the front-end electronics, to match the pad size. To achieve this goal most modern techniques for circuit assembly are used. In almost all aspects, it means to stretch the techniques beyond what is available in industrial manufacturing today. Consequently the development has been done in close cooperation with industry. The major complication arises from the fact that the SALTRO16 dies are delivered untested. Further restrictions are due to the cost and availability of the chips, and that the yield is unknown.

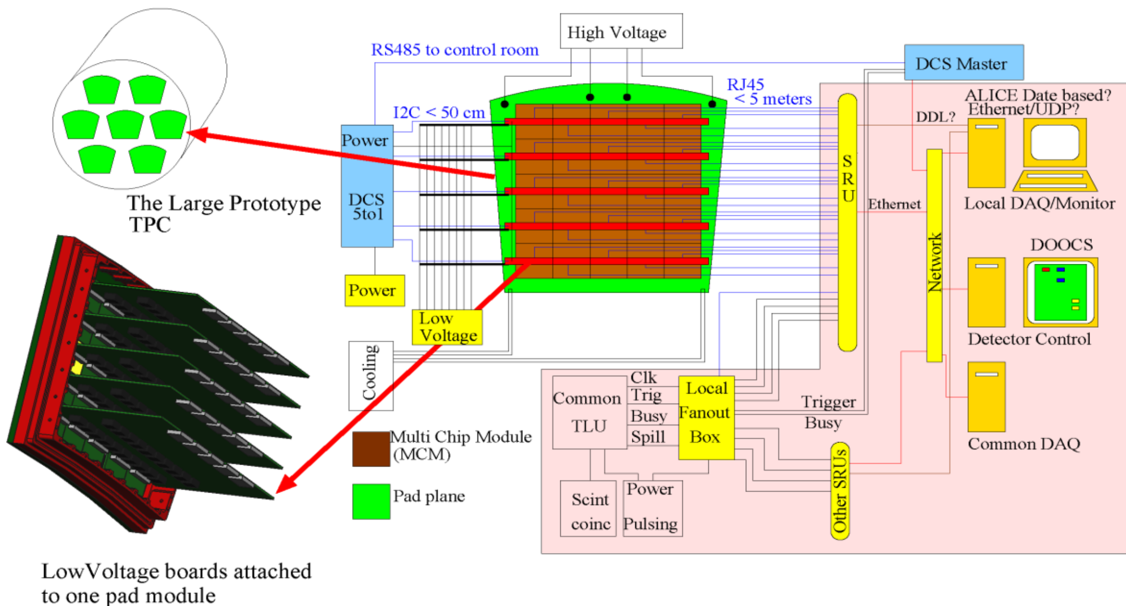

Figure 1: Schematic view of the SALTRO16 readout system for the LPTPC detector, shown for one pad module.

The readout system is a highly advanced development project, which includes several subsystems which will be described in this paper. These subsystems are not independent but have to be developed in parallel. In order to facilitate testing and debugging of the various subsystems, it has in some cases been necessary to construct prototype systems to avoid complications due to the requirements of compactness or due to other constraints.

3. The Carrier Board

The SALTRO16 chip combines the analogue and digital signal processing of the incoming TPC signals. The silicon die itself is 8.7 x 6.2 mm^2 and contains 16 readout channels which equals an occupancy of 3.37 mm^2 per channel. The new chip can be turned off when no signals are expected, which reduces the power consumption and demands for cooling drastically.

The alternative of using packaged chips is not a realistic choice since it requires too much space on the LPTPC detector pad module, although testing, mounting and service would be simpler. Due to the uncertainty in the yield it is unrealistic to assemble untested dies directly on a pad module and expect that all chips will work. Instead the dies will be mounted on Carrier Boards, only slightly bigger than the chips themselves, which simplifies the handling and allows individual chips to be tested. The size of the Carrier Boards is 12.0 x 8.9 mm^2, which also includes space for bonding wires and some passive components. Eight of these carrier boards are mounted on one so-called Multi Chip Modules (MCM) (see Section 4), using BGA soldering techniques.

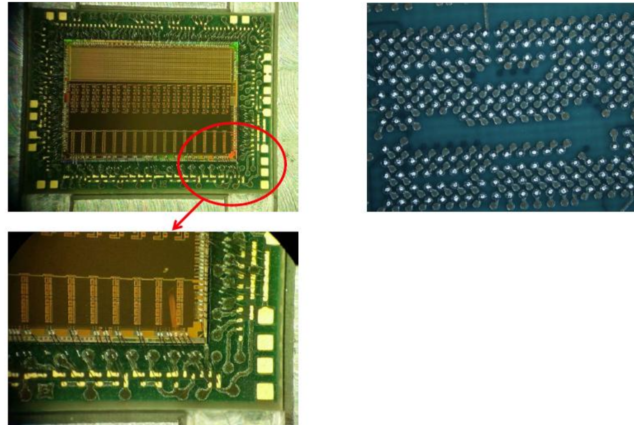

Figure 2: A Carrier Board with one bonded SALTRO16 chip (top left) and a blow up view of one corner (bottom left), where the bonding wires can be seen. On the right, bottom side of the Carrier Board with tin balls applied.

Figure 2 shows one Carrier Board holding one SALTRO16 chip. There are more than 200 bonding wires per board and the bonding procedure has to be very accurate, because of several bridge-overs, which require customized wire settings and fine tuning of the positioning due to the tightness. The application of small tin balls on the bottom side of the board has been successfully accomplished. The top side of the board will be covered by an epoxy layer. Figure2 shows the board before the application of the epoxy layer.

For the functionality tests of SALTRO16-chips mounted on Carrier Boards, a test set-up has been assembled, as shown in Figure 3. The boards are placed in a test socket into which the Carrier Board fits exactly. The test socket is a commercially available, high technology product, which had to be customized to fit our BGA pattern and chip dimension. There are spring loaded probe pins guided by small holes in the bottom of the test socket, which make contact with the tin balls on the bottom surface of the Carrier Board. In order to secure sufficient contact of the 208 probe pins, a fairly strong force has to be applied from above. The thin layer of epoxy protects the chip, bondwires and passive components on the Carrier Board.

For testing, this epoxy glob has to have a flat surface to distribute the force evenly over the whole surface. The application of the epoxy layer has caused more problems than expected. In order to reach a satisfactory result various epoxy materials have been tried out as well as different application procedures and modifications of the molding frame. The pins connect from the solder balls to the test socket board, which has a matching BGA-grid and provides an interface between the test socket and pin grid array (PGA) socket on the CERN SALTRO test

board, which was used to characterize the first packaged SALTRO16 chips. The functionality of the CERN SALTRO test board has been verified using a packaged SALTRO16 chip.

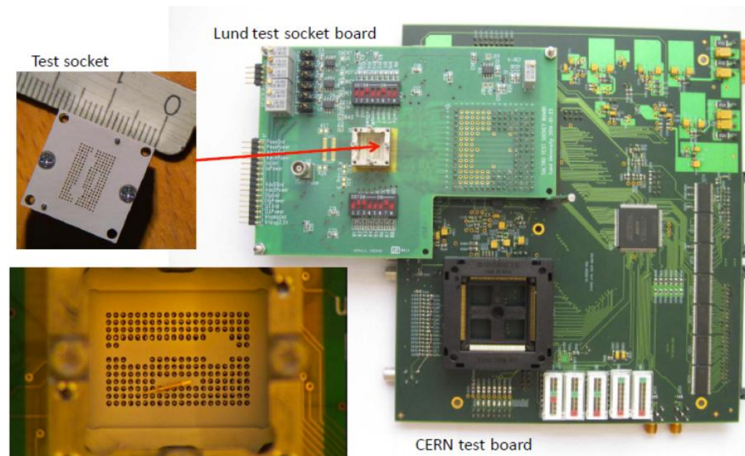

Figure 3: Test set-up to test the SALTRO16 chips mounted on Carrier Boards.

4. The Multi-Chip-Module (MCM) board

The Carrier Boards will be mounted onto the MCM boards by soldering of the small tin balls on the back side of the Carrier Board, organized in a so called BGA foot-print. Figure 4 shows the layout of the two sides of a MCM board. The advantages in placing the electronics components on separate boards, compared to soldering them directly onto the pad module, are listed below.

- Trace routing from the pads to the SALTRO chip becomes simpler since translational routing will essentially only be necessary at the edges of the pad module.
- With fewer or no active electronics components on the pad module it will be easier to design.
- Changes during the electronics prototyping will be cheaper and easier to implement and test.
- The interface between the SALTRO-part and the controller/readout-part is well defined.
- The trace routing on the plug-in board will be easier compared to the trace routing in the case all the electronics components are placed directly on the pad module. The pad module will need less layers.
- It moves heat away from the TPC endplate.
- It facilitates service. A malfunction in the readout chain can be fixed by replacing the electronics board instead of dismounting the whole pad module.

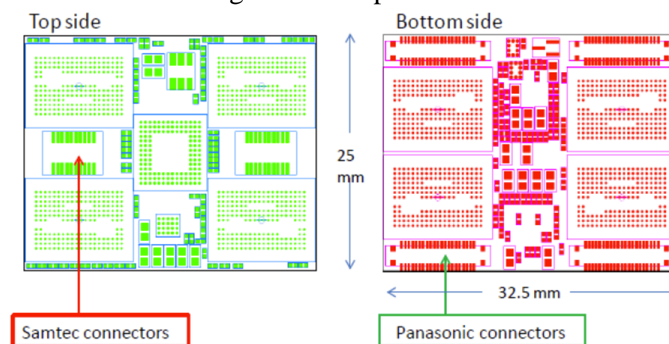

Figure 4: The MCM board top surface (left) and bottom surface (right).

The MCM boards will be attached to the pad module via 4 Panasonic micro-connectors, which have a lead pitch of 0.4 mm and a mated height of 2.5 mm, and transmit the signals from the pads to the preamplifier of the SALTRO16 chip. The connectors have to be mounted with very high precision on the pad module and on the carrier board since four such connectors have to fit simultaneously and the MCM boards are sitting very tightly. In order to meet the areal constraints, the Carrier Boards have to be mounted on both sides of the MCM board. That is possible since the Panasonic connectors are elevating the MCM board by 2.5 mm above the pad module, which thus leaves enough space for components on both sides of the MCM Board. In Figure 4 the rectangles with a dot-matrix of 20x13 dots are 8 sets of BGA patterns (4 on each side) for the Carrier Boards. These boards are placed in each corner of the MCM board such that the analogue inputs are facing outwards towards the long edges of the MCM board, the bottom side of which the four 42-pin connectors for the 32 input signals (plus grounds) also are placed. The digital signals are concentrated towards the center of the board. In the centrally placed square on the top side of the MCM board, the BGA footprint of a CPLD (Complex Programmable Logic Device) is seen, which has an area of only 8x8 mm^2. The total current drawn by the MCM electronics is about 16 A per board at 8 different voltages, corresponding to a power consumption of about 22 W per board.

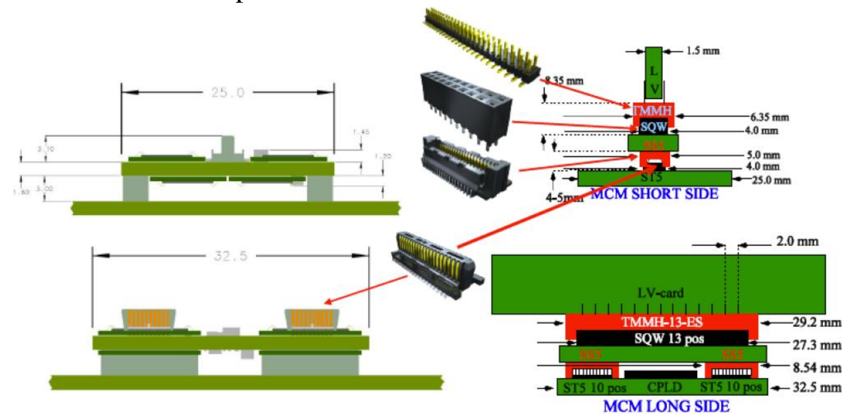

Figure 5: Side views of the MCM board assembly including an adaptor board.

On the MCM board there is also a DAC for setting the decay time in the preamplifier and reference voltages to the SALTRO16, as well as a temperature sensor. These are controlled via an I2C bus connecting to a 5to1 board(see Section 7) which plays the role as a I2C master for 25 MCM boards in total. On the upper surface of the MCM board Samtec connectors, for getting low voltage from LV-board (see Section 6) and transmission of the signals from the SALTRO16 chip, are placed. The problem with this connector is that the female partner does not allow edge mounting on the LV-board , which has forced us to introduce an adaptor board, resulting in an additional pair of connectors. The MCM board and the adaptor board is considered as one unit in the sense that it should not be needed to disconnect the two. The proposed layout of the adaptor board can be seen in Figure 5. The dimensions of the MCM board, which serves 128 channels, are 32.5x25 mm^2. This corresponds to a space occupancy per channel of about 6.4 mm^2. However, also some space is needed for HV-supply of the MPGD system and cooling of the electronics so that the available area for electronics is further reduced.

The design of the MCM board is essentially ready but it will be redesigned in so called High Density Interconnect (HDI) technology. This allows for a higher routing density, for both signals and voltage supply, compared to conventional PCB design. A reduction in the number of

layers, from the current 20 layers to maybe 10, can be envisaged. Vias can be made as small as 25-50 μm by laser drilling. This technology also offers the possibility to mount components, electrical or mechanical, into cavities in the PCB, which are covered with one or more dielectric layers. The components are, thus, embedded into the PCB and the surface is essentially left free for surface mounting of readout chips. This will be a valuable exercise for the final design. We plan to produce a mock-up system to check that the mounting of the components and connectors on the MCM board does not lead to unexpected difficulties and that the various parts fit together.

The heart of the readout system on the MCM board is the CPLD chip. There are four types of communication between the DAQ and the individual channels of an SALTRO16 chip: send a command, write data to a register, read data from a register, read the data of an event. Most of these operations are concurrent during data taking and the control of the operations is handled via a serial link. Other controls on the MCM, which are done by the CPLD, are:

- The 8 bits for configuring the SALTRO16 preamp/shaper.
- Controlling the power pulsing of the SALTRO chip.
- Sending error and status messages to the DAQ

Tasks that do not need to involve the CPLD are foreseen to be done via the I2C communication, including the control of the DAC for setting the pre-amplifier decay time and the SALTRO16 reference voltages and the reading of the temperature sensor. The CPLD will have two I2C interfaces, one for programming the CPLD, and one in the case we decide to communicate with the CPLD via the I2C as well.

5. The Readout and DAQ system

For the readout of the MCM boards and communication to the DAQ we will use serial readout. The functionality needed locally in the vicinity of the MCM board is the serial to parallel conversion of the downloaded data and the parallel to serial conversion of the uploaded (readout) data. This is accomplished by the CPLD chip. Serial high speed readout has become possible with the development of a new generation of FPGA's that provide serial interfaces supporting data rates of several Gbit per second. A rather general purpose serial connection suitable for many experiments is the SRU (Scalable Readout Unit) developed in RD51 [4]. We plan to use the SRU to directly communicate with the MCM via the Data Trigger Control (DTC) link, which contains clock, trigger/control and data. However, this requires that the FPGA firmware on the SRU is modified to include also the customized communication to and from the MCM.

One SRU can handle 40 MCM boards. The DTC protocol uses the four pairs of leads in the RJ45 cable for the fast signals. The solution reading the MCM boards directly to the SRU is the cheapest as it uses the least new hardware. There are two readout possibilities of the SRU, either the ALICE DATE with the DDL optical link or direct readout using optical ethernet. One SRU with power box and cables have been purchased and the first tests have been successfully performed. The communication between the SALTRO16 chip and the CPLD was established as well as with the SRU. Data could also be read out, using the DDL optical link. However to avoid being dependent of the ALICE DATE DDL libraries and dedicated hardware, the ethernet option is preferred.

6. The Low Voltage board

The Low Voltage board (LV-board) provides low voltage for five MCM boards. Each MCM board requires eight different voltage levels and thus the LV-board contains 8x5 = 40 voltage regulators. The communication with the CPLD and the I2C bus on the MCM is transmitted through the LV-board. There are five LV-boards per pad module. The board contains I/O registers to switch on/off the regulators, ADCs to monitor voltages and currents, and a temperature sensor.

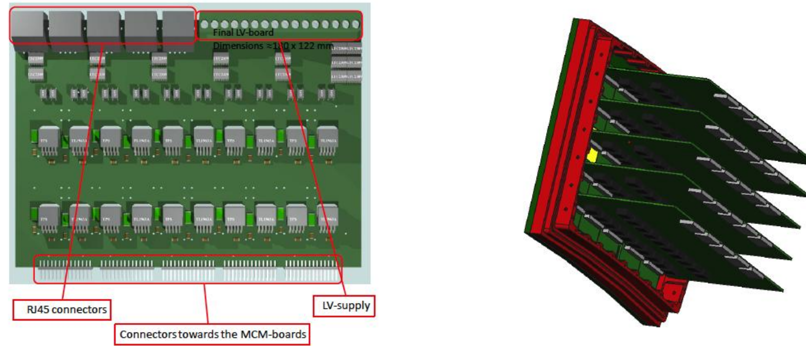

Figure 6: Concept of the LV-Board (left) and five LV-boards mounted on the MCM Board of one module (right).

The overall layout of the LV-board is ready and shown in Figure 6 (left). The maximum width of the board is limited by the dimensions of the module and the minimum width is given by the positioning of the connectors to the MCM boards, which in turn depends on the layout of the cooling pipes. The final dimensions and layout, thus, still have to be fixed before the design can be completed. The LV-boards are connected to the MCM-board via the adaptor board. No cables will be used, which probably simplifies and speeds up the assembly procedure, as will be tested with the mock-up system, and it is also be favorable from a noise point of view. A schematic view of a module with five mounted LV-boards are shown in Figure 6 (right). A LV-board prototype providing the voltages for one MCM board has been built and has been used to verify the I2C communication with the Detector Control Boards (see Section 7).

7. The Detector Control System

In order to control and monitor the LV-boards and the MCM boards, we have designed two boards, a master control and one slave module (called 5to1) both containing microprocessors. The slave module contains one microprocessor per LV-board for one pad module. The master board contains one microprocessor only, which can communicate with up to four 5to1 boards. A schematic view of the system is shown in Figure 7 (left) together with the corresponding boards (right). The boards are ready and have been successfully tested. We plan to monitor about 700 parameters from the LV- and MCM-boards per module. For this we are proposing to use DOOCS [5], which is already used by the DESY LCTPC-group with good experience. The system is currently being developed.

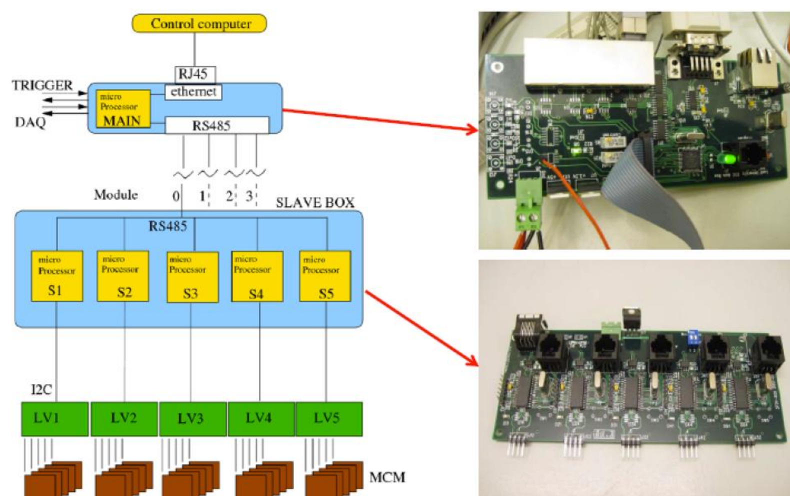

Figure 7: A schematic view of the DCS (left) and the corresponding boards (right).

8. Readout of one LPTPC pad module

On one LPTPC pad module 25 MCM's will be arranged in a 5x5 matrix, which thus contain 128 x 25 = 3200 channels in total. This is consistent with a pad size of about 1 x 8.5 mm^2. The layout leaves some space on the sides as well as on top and bottom for the connection of HV-cables and cooling pipes, although the limited space probably will call for some innovative solutions.

9. Conclusions

In this paper we present the state-of-the-art for the readout system of a large TPC based on the SALTRO16 chip, focusing on the design developments in order to achieve a significant reduction in size of the front-end electronics to match the detector pad size. The SALTRO16 chip does not provide an ideal solution for our application and has led to several cumbersome compromises in the PCB design. The disadvantages of the SALTRO-based system are, for example, the many connectors that are needed to link the various subsystems, the many voltage levels, which have led to a clumsy voltage supply system, and the many chip configurations that have to be set externally.

Since it is not likely that a final readout chip will be developed within the next years further improvements of the PCB design have to be based on the SALTRO16 chip. Using novel techniques in PCB design, including 3D mounting of chips and possibly HDI (High Density Interconnect) technology, it will still be possible to construct front-end electronics that meets the requirements of small pad sizes. However, the SALTRO16 chip can not constitute the final solution for a large TPC at the ILC due to the insufficient sampling depth.

Acknowledgments

This work is supported by the AIDA project of the Commission of the European Communities under the 7th Framework Program and by the Swedish Council (VR). G. De Lentdecker is Research Associate of the Belgian FRS-FNRS.

References

[1] R. Diener on behalf of the LCTPC collaboration, *Development of a TPC for an ILC Detector*, *Physics Procedia* 37 (2012) 456-463.

[2] L. Musa et al., *The ALICE TPC Front End Electronics*, Proc. of the IEEE Nuclear Science Symposium, 20-25 Octobre 2003, Portland.

[3] M. De Gaspari, Systems-on-Chip (SoC) for applications in High-Energy Physics, PhD Thesis, University of Heidelberg 2012.

[4] S. Martoiu et al., *Development of the scalable readout system for micro-pattern gas detectors and other applications*, 2013 JINST **8** C03015.

[5] *The Distributed Object Oriented Control System (DOOCS)* http://tesla.desy.de/doocs/doocs.html