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Design of a Solid-State Fast Voltage Compensator for klystron modulators requiring constant AC power consumption

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Keywords: Klystrons, Power quality, Pulsed power systems, Switching converters.

Abstract

This paper proposes a novel topological solution for klystron modulators integrating a Fast Voltage Compensator which allows an operation at constant power consumption from the utility grid. This kind of solution is mandatory for the CLIC project under study, which requires several hundreds of synchronously operated klystron modulators for a total pulsed power of 39 GW. The topology is optimized for the challenging CLIC specifications, which require a very precise output voltage flat-top as well as fast rise and fall times (3µs). The Fast Voltage Compensator is integrated in the modulator such that it only has to manage the capacitor charger current and a fraction of the charging voltage. Consequently, its dimensioning power and cost is minimized.

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ABSTRACT

This paper proposes a novel topological solution for klystron modulators integrating a Fast Voltage Compensator which allows an operation at constant power consumption from the utility grid. This kind of solution is mandatory for the CLIC project under study, which requires several hundreds of synchronously operated klystron modulators for a total pulsed power of 39 GW. The topology is optimized for the challenging CLIC specifications, which require a very precise output voltage flat-top as well as fast rise and fall times (3µs). The Fast Voltage Compensator is integrated in the modulator such that it only has to manage the capacitor charger current and a fraction of the charging voltage. Consequently, its dimensioning power and cost is minimized.

Index Terms — **Klystrons, Power quality, Pulsed power systems, Switching converters.**

1 INTRODUCTION

The utilization of pulsed power converters is growing more and more nowadays, particularly in the medical and in the experimental particle physics domain. They are generally based on capacitor discharge topologies, which allow a certain decoupling between the charging power (usually low) and the output power (usually very high, as the stored energy is released during a short period of time). In order to reduce power consumption, new accelerators under study foresee the utilization of a large number of pulsed power converters, which are typically synchronously operated. As the number of converters increases, the decoupling between the total output peak power versus the average charging power provided by the utility grid becomes a challenging issue. A passive solution would consist in increasing the size of the capacitor banks in order to respect a maximum percentage of power fluctuation on the grid side. However this solution implies an unjustified increase in modulators size and cost (passive elements and civil engineering). Therefore, active solutions able to solve the power fluctuation issue in a more efficient way shall be found. This is the case of a new linear accelerator under study at CERN (CLIC - Compact Linear Collider) which requires the design and construction of a new klystron modulator [1] capable of respecting the challenging specifications summarized in Table 1. Since for this accelerator several hundreds of klystron modulators are required to operate synchronously, producing a total pulsed power of 39GW, optimal topological and design solutions must be evaluated such that only a constant average power (300MW) is withdrawn from the utility grid.

2 FAST VOLTAGE COMPENSATOR PRESENTATION

In order to achieve the constant power consumption objective, the main strategy consists in stabilizing the charging power at the DC side, provided by the capacitor charging unit. If we consider a capacitor charger without intermediate energy storage, the stabilization of the output DC power implies the stabilization of the input AC power. A first solution consists in trying to increase the bandwidth of the capacitor charger and regulate the charging current, I_{CH}, in order to make the DC power flow constant [2]. However this can be quite

Table 1. CLIC Modulator's output pulse specification

Nominal pulse voltage	V_{sn}	180 kV
Nominal pulse current	I_{sn}	160 A
Pulse peak power	P_{mod_out}	28.8 MW
Rise & fall times	t_{rise}, t_{fall}	3 µs
Settling time	t_{set}	5 µs
Flat-top length	t_{flat}	140 µs
Repetition rate	RR	50 Hz
Voltage overshoot	V_{ovs}	1 %
Flat-Top Stability	FTS	0.85 %
Repeatability	REP	10 - 50 ppm

challenging due to the typical high voltage output ratings and the fast pulse transients to be compensated by the charger unit.

A different active solution integrating the regulation of the output pulse and the charging voltage into a single power converter (Dual Purpose Active Bouncer or DPAB) was presented in [3]. This topological solution, illustrated in Figure 1.a), is able to greatly reduce the power fluctuation levels. However it also presents some drawbacks. First of all the DPAB must be dimensioned in order to withstand the pulse operation ratings (i.e. modulator primary current). This implies that, even though the charging current is very low, the current ratings required during the pulse are usually high and impose the selection of high power semiconductors. These components present higher switching losses than the lower power ones, reducing the efficiency of the system. Furthermore, due to the voltage drop in the transformer during the pulse, it is not possible to regulate the output and the charging voltages at the same time.

A novel solution, illustrated in Figure 1.b), consists in assigning the output voltage and the charging voltage regulation tasks to two different power converters: an active bouncer and a Fast Voltage Compensator (FVC), respectively. By using an individual power converter for each of the compensation tasks, the drawbacks of the DPAB solution are suppressed: the FVC can use low power semiconductors (leading to lower switching losses), the active bouncer can be optimized for very high-bandwidth in voltage and current, and the voltage drop issue across the pulse transformer is not affecting the AC power stabilization action anymore. Figure 2 shows the ideal waveforms of the FVC during a complete cycle. The FVC maintains the charging voltage constant. Therefore the charging unit only supplies a constant charging current (which requires extremely low dynamics) to achieve the objective of constant power consumption.

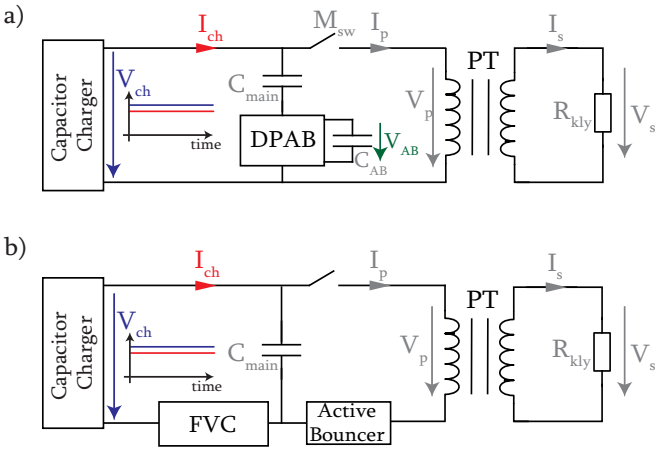

Figure 1. a) Classical monolithic modulator topology equipped with a dual purpose active bouncer (DPAB); b) with a fast voltage compensator for constant AC power consumption and active bouncer.

3 FAST VOLTAGE COMPENSATOR DESIGN

3.1 OUTPUT FILTER DESIGN

For a given pulsed power application and considering a perfectly squared-shaped output current, the required average charging current is:

$$I_{CH} = I_P . T_P . RR \tag{1}$$

Where I_P is the modulator current in the primary side of the transformer, T_P is the pulse duration and RR the repetition rate. The main capacitor bank is dimensioned in order to experience a defined voltage discharge ΔV, during the pulse, as shown in equation (2).

$$C_{main} = \frac{T_P . (I_P - I_{CH})}{\Delta V} \tag{2}$$

The modulator system can be modelled as depicted in Figure 3. The capacitor charger would ideally consist of a constant current source; and the FVC would operate as a voltage source that regulates the charging voltage V_{CH} at a constant value. In order to simplify the analysis, a simple LC output filter for the FVC has been selected. With the purpose of achieving a constant charging voltage, the FVC output filter capacitance voltage evolution should compensate the voltage change rate across C_{main} (see Figure 2). Equating these slopes during the pulsing and charging phases, one can calculate the current flowing through the FVC filter inductance on each operation phase, as shown in equation (3) and (4) respectively.

$$I_{FVC\_pulsing} = I_P . \frac{C_{FVC}}{C_{main}} - I_{CH} . (1 + \frac{C_{FVC}}{C_{main}}) \tag{3}$$

$$I_{FVC\_charging} = -I_{CH} . (1 + \frac{C_{FVC}}{C_{main}}) \tag{4}$$

Notice that the FVC current on each operation phase is ideally constant and influenced by the size of the main capacitor bank and the FVC output capacitance. For the sake

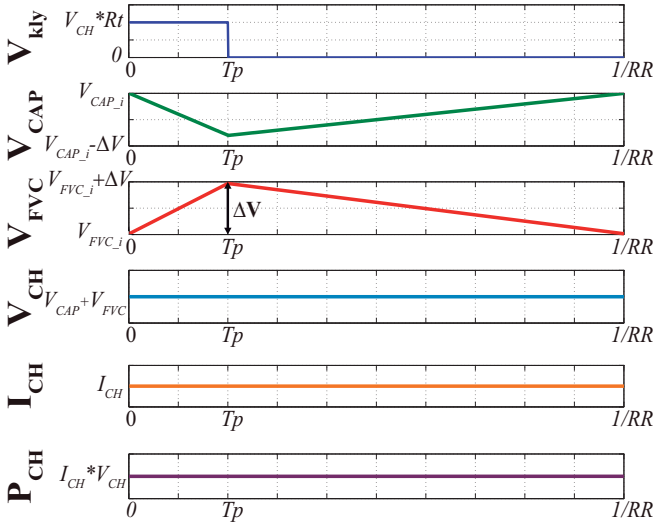

Figure 2. Output voltage pulse, C_{main} voltage, FVC voltage, charging voltage, charging current, and charging power waveforms during a complete cycle.

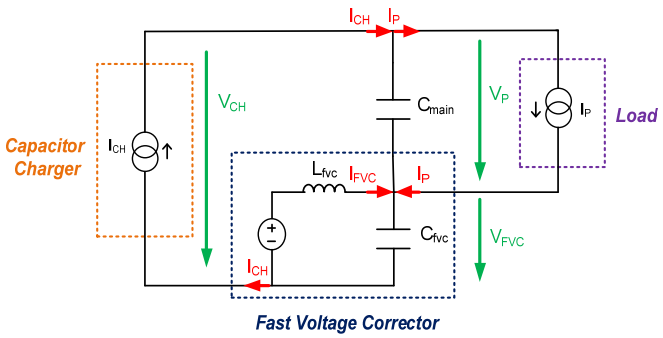

Figure 3. Modulator simplified model.

of a dimensional analysis, one has to define the LC output filter and the converter topology (1,2, or 4 quadrant). Figure 4 shows the influence of the FVC output filter capacitor C_{FVC} size on the FVC nominal constant currents for each operation phase, considering a modulator respecting CLIC specifications. During the charging phase, the FVC current is always negative and experiences a very small variation when increasing C_{FVC}. On the other hand, the current during the pulsing phase varies from negative (for small C_{FVC} values) to positive. This implies that the converter would need to be either unidirectional or bidirectional in current, depending on C_{FVC} selection. A special case would be the capacitance value between the two regions, where no current from the FVC would be required during the pulse.

Although the current during the pulsing phase has little influence in the FVC average current ($Tp<<1/RR$), it has a great impact on the topology selection. In order to reduce the FVC dimensioning power and losses, the designer should tend to select a low C_{FVC} value.

To define whether the FVC should be a 1, 2, or 4 quadrant converter, and energy flow analysis during one complete operational modulator cycle (charging + discharging phases) shall be carried out. As illustrated in Figure 2, the FVC output voltage can be either unidirectional or bidirectional. The analysis from Figure 4 shows that the output current can be either unidirectional or bidirectional as well. Depending on the FVC output voltage and current reversibility, the neat energy flow throughout the FVC converter would be completely different. If during a complete operation cycle the FVC supplies and recovers the same amount of energy, a dedicated capacitor charger for the FVC would not be required. Three FVC topologies are possible:

1. Unidirectional in voltage and bidirectional in current.
2. Bidirectional in voltage and unidirectional in current.
3. Bidirectional in voltage and current.

The first one would require a very high FVC current during the pulse in order to achieve zero average energy, as the pulse time is very short in comparison with the charging time. The remaining two solutions are both interesting; however the bidirectional in current and voltage solution allows the utilization of a bigger filter capacitor C_{FVC} value for the same current, decreasing the inductance value for the same level of

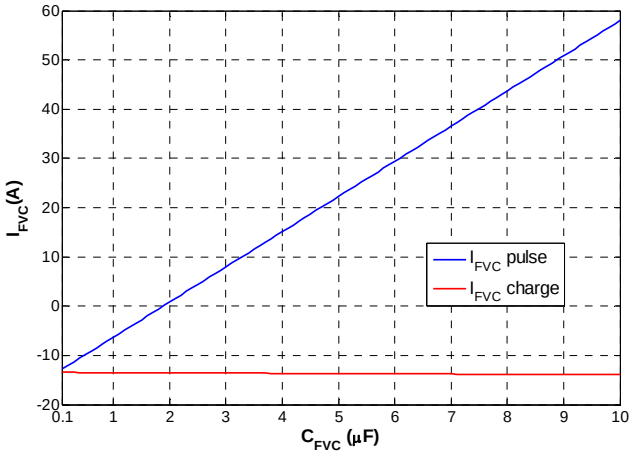

Figure 4. FVC currents in the pulsing and charging phases for different FVC output filter capacitor, C_{FVC}, values.

switching frequency harmonics attenuation. Figure 5 shows the ideal waveforms achieved with a 4-quadrant topology and the energy balance during a complete cycle.

In order to complete the output filter dimensioning analysis, a given bandwidth and switching harmonics attenuation must be specified. Systematic numerical simulations on a CLIC specified modulator have been carried out to study the relation between the FVC voltage closed-loop bandwidth versus the DC (and AC) power fluctuation. Results are shown in Figure 6. In this particular example, in order to achieve a 1% power fluctuation, a minimum of 15 kHz closed-loop bandwidth is required. Considering a typical design margin of 20% between the closed and the open-loop bandwidths, the LC filter can be defined. The switching frequency would be derived from the output ripple specifications.

3.2 CONTROL STRATEGY

The FVC load changes during the two operating phases: charging and discharging (pulsing). During the pulsing phase the klystron and the main capacitor bank are connected in parallel to the FVC output filter capacitance, providing additional damping to the filter. However, during the charging

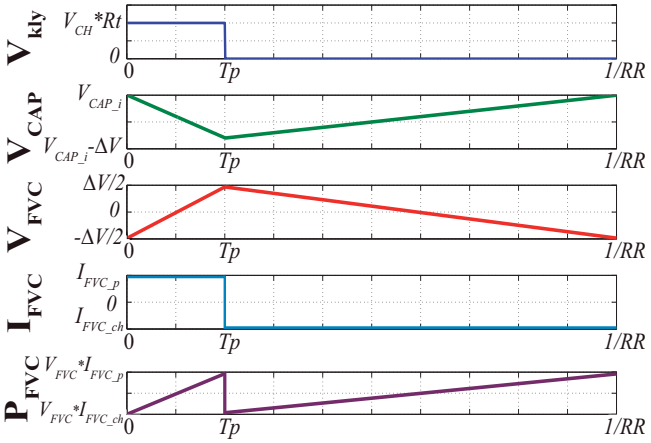

Figure 5. FVC power flow is centered on zero, resulting in zero average energy flow during a complete cycle.

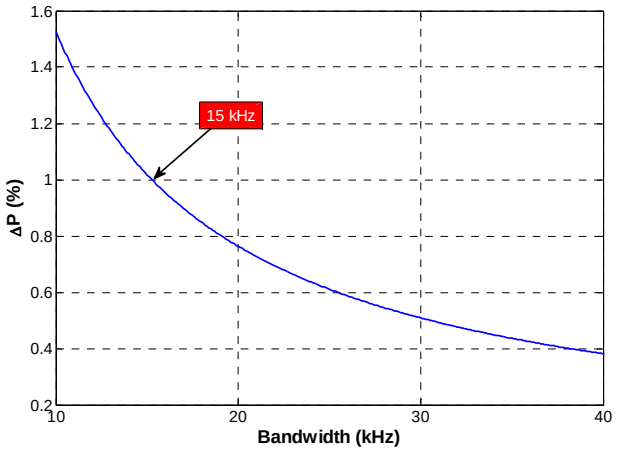

Figure 6. Percentage of power fluctuation versus FVC closed-loop voltage bandwidth.

phase the load is composed of a different circuit involving the capacitor bank and the charger's output impedance, which should be very low since it operates as a current source. In this last case special care must be taken in order to avoid possible low-range harmonic amplifications due to the resonance peak of the equivalent LC filter (C composed of C_{FVC} + C_{main}). In order to adapt the FVC regulation to each load case, a two controller structure is proposed, as shown in Figure 7.

Each of the controllers is only acting during a given operating phase. They consist of polynomial RST digital controllers [4], able to specify different dynamics for regulation and tracking, which is particularly important during the transition between two operating phases.

4 PERFORMANCES EVALUATION BY NUMERICAL SIMULATION

In order to validate the performances of the FVC, a numerical simulation considering a modulator with CLIC specifications and a primary voltage of 15kV has been carried out. A single H-bridge with the parameters shown in Table 2 has been considered for the FVC converter.

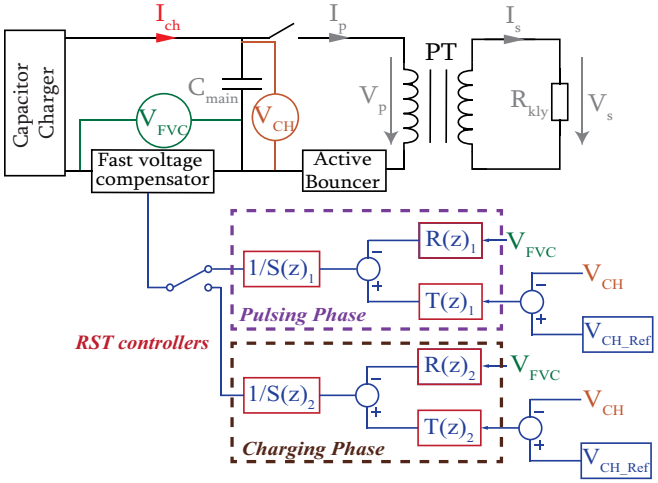

Figure 7. FVC Control strategy.

Table 2. Fast Voltage Compensator simulation parameters

DC Bus	1000 V
Inductance value	100 µF
Filter capacitor	7 µC
Switching frequency	100 kHz
Modulator capacitor bank	333 µF

Figure 8 shows the simulation results. The power fluctuation has successfully been reduced to a maximum of 0.08%. The current in the FVC is positive during the pulsing phase (with a maximum of 53 A) and negative during the pulsing phase (with a maximum value of -43A).

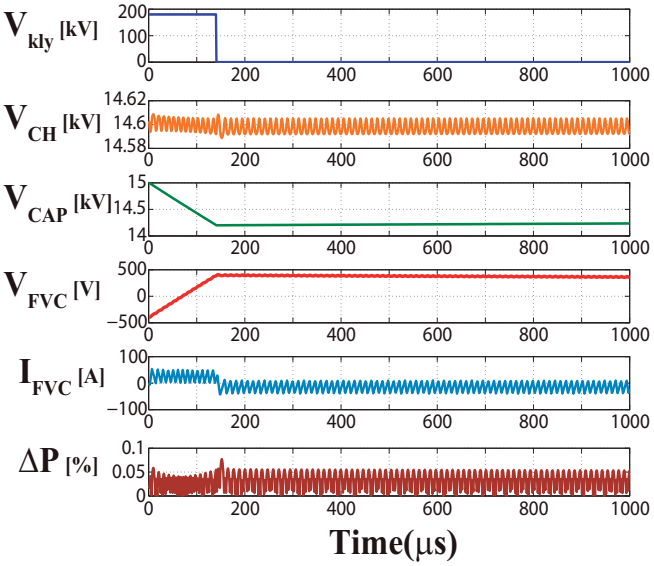

Figure 8. Numerical simulation results.

5 CONCLUSION

The proposed FVC solves the drawbacks of the previously proposed solution (DPAB), which is only interesting when the charging and the primary current values are close (e.g. long pulse modulators using step-up transformers with low transformation ratios). Numerical simulation on CLIC specifications have shown very good performances, superior to the DPAB, making this solution the most interesting candidate as a power fluctuation compensation system for CLIC's Drive-Beam klystron modulators.

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