The CLIC Vertex Detector

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The CLIC Vertex Detector

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ABSTRACT: The precision physics needs at TeV-scale linear electron-positron colliders (ILC and CLIC) require a vertex-detector system with excellent flavour-tagging capabilities through a measurement of displaced vertices. This is essential, for example, for an explicit measurement of the Higgs decays to pairs of b-quarks, c-quarks and gluons. Efficient identification of top quarks in the decay $t \rightarrow Wb$ will give access to the ttH-coupling measurement. In addition to those requirements driven by physics arguments, the CLIC bunch structure calls for hit timing at the few-ns level. As a result, the CLIC vertex-detector system needs to have excellent spatial resolution, full geometrical coverage extending to low polar angles, extremely low material budget, low occupancy facilitated by time-tagging, and sufficient heat removal from sensors and readout. These considerations challenge current technological limits. A detector concept based on hybrid pixel-detector technology is under development for the CLIC vertex detector. It comprises fast, low-power and small-pitch readout ASICs implemented in 65 nm CMOS technology (CLICpix) coupled to ultra-thin planar or active HV-CMOS sensors via low-mass interconnects. The power dissipation of the readout chips is reduced by means of power pulsing, allowing for a cooling system based on forced gas flow. This contribution reviews the requirements and design optimisation for the CLIC vertex detector and gives an overview of recent R&D achievements in the domains of sensors, readout and detector integration.

KEYWORDS: Particle tracking detectors; Performance of High Energy Physics Detectors; Electronic detector readout concepts (solid-state); Front-end electronics for detector readout

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1 Introduction

The proposed ILC and CLIC concepts [1–4] for linear colliders with centre-of-mass energies from a few hundred GeV up to 3 TeV and with luminosities of a few 10^{34} cm^{-2}s^{-1} both have a large physics potential, complementing and extending the measurements of the current LHC experiments. They will allow for precision measurements of Standard Model physics (e.g. Higgs, top) and of new physics potentially discovered at the 14 TeV LHC (e.g. SUSY). Moreover, direct and indirect searches for new physics over a large range of mass scales will be performed. In the case of CLIC the higher energy of up to 3 TeV comes at the price of high rates of beam-induced backgrounds overlapping with the physics events within the bunch trains of only 156 ns duration [5]. Time stamping of hits on the few ns level is therefore required for most sub-detectors at CLIC, in order to separate physics events from beam-induced backgrounds. The demands for precision physics, in combination with the challenging experimental conditions at CLIC, have inspired a broad detector R&D program. In particular, the vertex-detector system has to fulfil unprecedented requirements in terms of material budget and spatial resolution in a location close to the interaction point, where the rates of beam-induced background particles are highest. The ongoing CLIC vertex-detector studies focus on ultra-thin hybrid pixel detectors and aim for integrated solutions taking into account constraints from mechanics, power delivery and cooling.

2 Vertex-detector requirements

The primary purpose of the CLIC vertex detector is to allow for efficient tagging of heavy quarks through a precise determination of displaced vertices. Monte Carlo simulations show that these goals can be met with a high-momentum term in the transverse impact-parameter resolution of $a \approx 5\mu$m and a multiple-scattering term of $b \approx 15\mu$m, using the canonical parametrisation

$$\sigma(d_0) = \sqrt{a^2 + b^2 \cdot \mathrm{GeV}^2/(p^2 \sin^3\theta)}, \tag{2.1}$$

where p is the momentum of the particle and θ is the polar angle with respect to the beam axis.

These requirements can be met with multi-layer barrel and endcap pixel detectors with an inner radius of approximately 30 mm, operating in a magnetic field of 4-5 T and using sensors with a single-point resolution of $\approx 3\mu$m and a material budget of $\approx 0.2\%$ of a radiation length (X_0) for the beam-pipe and for each of the detection layers.

Beam-induced backgrounds are expected to lead to an occupancy of up to 3% per bunch train in the innermost layers [5]. Time slicing of hits with an accuracy of ≈ 10 ns will be required to separate such backgrounds from physics events.

The radiation exposure of the vertex-detector is expected to be moderate, compared to the present LHC pixel detectors. For the inner-detector layers a total 1-MeV neutron-equivalent fluence of less than $10^{11} n_{eq}/\mathrm{cm}^2/\mathrm{y}$ and a total ionising dose of less than 1kGy are expected [5].

The R&D aims at achieving the single-point resolution target with pixels of $\approx 25\mu\mathrm{m} \times 25\mu\mathrm{m}$ and analog readout. The material-budget target corresponds to a thickness equivalent to less than 200 μm of silicon, shared by the active material, the readout, the support and the cooling infrastructure. This implies that no active cooling elements can be placed inside the vertex detector. Instead, cooling through forced air-flow is foreseen, limiting the maximum power dissipation of the readout to ≈ 50 mW/cm^2. Such low power consumption can be achieved by means of power pulsing, i.e. turning off most components on the readout chips during the 20 ms gaps between bunch trains.

3 Flavour-tagging performance

In the following we give examples showing the importance of achieving an excellent flavour-tagging performance with the CLIC vertex-detector system. All studies have been performed based on simulation models fulfilling the requirements outlined in the previous section and using the multi-variate flavour-tagging package LCFIPlus [6].

3.1 Measurement of the top Yukawa coupling

Linear electron-positron colliders allow for a direct measurement of the top Yukawa coupling through the process $e^+e^- \to t\bar{t}H$. A full-simulation study for CLIC with an energy of $\sqrt{s} = 1.4$ TeV, an integrated luminosity of 1.5 ab^{-1} and assuming unpolarised beams has been performed [7], following a similar study for ILC at 1 TeV [8]. It includes physics background events as well as pile-up overlay from $\gamma\gamma \to$hadrons. The Higgs boson is reconstructed in the $H \to b\bar{b}$ decay mode and the top quarks through the decay $t \to Wb$, with subsequent fully hadronic or semi-leptonic

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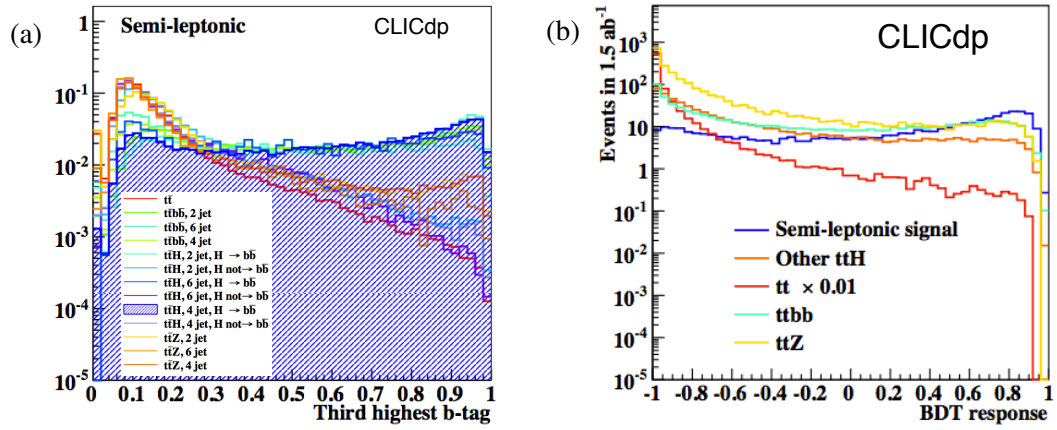

Figure 1: Event selection variables for signal ($t\bar{t}H$, 4 jet, $H \to b\bar{b}$) and background samples in the semi-leptonic channel of the $t\bar{t}H$ analysis. (a): third-highest b-tag value, normalised to unit area. (b): multi-variate classifier output for final event selection. From [7].

decay of the two W bosons. The resulting 6- and 8-jet final states are challenging for the jet clustering and missing-energy reconstruction. Efficient identification of up to 4 b-jets and a good lepton reconstruction are crucial ingredients of the analysis.

The LCFIPlus flavor-tagging package assigns each jet with a b- and c-probability. Figure 1(a) shows the distribution of the third-highest b-tag in each event for signal and background simulation samples in the analysis that includes the semi-leptonic W-decay channels. A clear distinction between signal and background is observed with this variable, which is an important input to the multi-variate final event selection based on a boosted-decision-tree (BDT) classifier (figure 1(b)). The statistical uncertainty on the cross-section measurement of the $t\bar{t}H$ process achieved in this analysis is 12.0% (10.9%) in the semi-leptonic (fully hadronic) decay channels, resulting in a combined uncertainty of 8.1%. The resulting uncertainty on the ttH coupling g_{ttH} is 4.3% for the combination of all considered decay channels. The systematic uncertainties are expected to be negligible. The achievable precision on the determination of the couplings at the LHC, for comparison, is approximately 7–10%, assuming a dataset of 3 ab^{-1} collected at an energy of 14 TeV [9].

3.2 Impact of detector geometry on flavour-tagging

Design optimisation studies for the vertex detector were performed using simulated full-detector b- and c-tagging performance results as benchmarks and considering constraints from mechanical engineering and cooling-system studies [10]. The flavour-tagging performance was assessed for jets at various energies and directions.

Figure 2(a) shows one of the simulated layouts with a spiral arrangement of the end-cap detectors, allowing for air-flow into and out of the barrel region. The obtained performance for this geometry is similar to the one for the corresponding disk geometry, except for the barrel-endcap transition region, where the spiral layout leads to a reduction in the number of layers for a small azimuth-angle range. (figure 2(b)).

The comparison between a geometry with 5 single detection layers and one with 3 double layers with common support results in similar overall performance for jet energies above 100 GeV.

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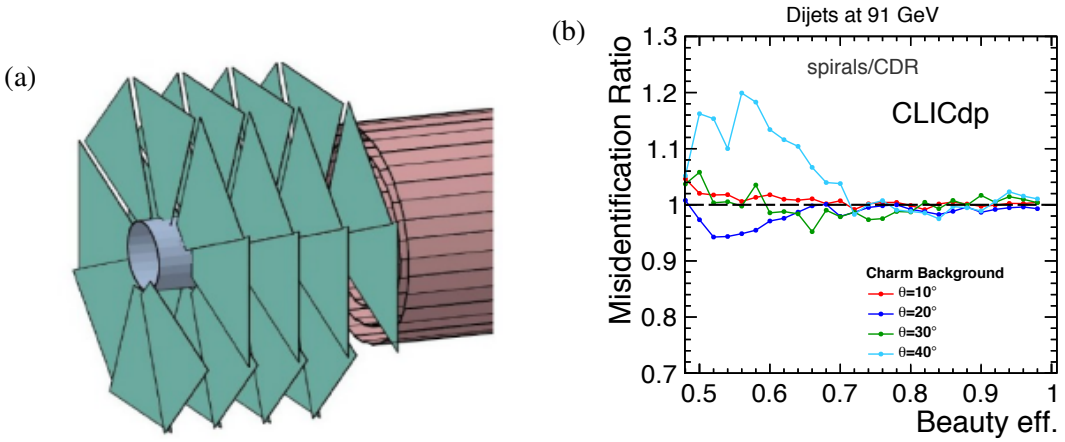

Figure 2: (a): simulation layout with spiral end-cap geometry. (b): resulting b-tagging performance for dijets at 91 GeV in comparison with a disk layout (CDR), shown as the ratio of the misidentification probabilities for the background consisting of charm jets (b). From [10].

For jet energies below 100 GeV the double-layer geometry shows a small improvement, due to the reduced amount of material for the supports (figure 3(a)).

A significant degradation in performance is observed after doubling the amount of material per layer from the reference simulation value of $0.1\%X_0$ to the design target of $0.2\%X_0$, as shown in figure 3(b) for the case of c-tagging. The background-rejection of the geometry with doubled material budget is approximately 5–35% worse, depending on the type of background and the analysis-dependent required signal efficiency.

3.3 Impact of flavour-tagging on physics performance

The impact of a decrease in flavour-tagging performance on the physics-analysis results was estimated for the example of Higgs production in the vector-boson fusion process with subsequent decay of the Higgs to pairs of b- and c-quarks: $e^+e^- \to H\nu\bar{\nu}$, $H \to b\bar{b}, c\bar{c}$. This analysis was performed for an energy of 3 TeV and an integrated luminosity of 2 ab^{-1}. Typical jet energies are of the order of 130 GeV. The analysis results obtained with nominal flavour-tagging parameters were scaled following a change in fake rates of $\pm 20\%$, corresponding approximately to a change of the amount of material in the vertex-detector region by a factor of two (see previous sub-section). The resulting change in statistical precision for the cross-section determination amounts to $\pm 6-7\%$ ($\pm 15\%$) for the $H \to b\bar{b}$ ($H \to c\bar{c}$) decay channels. Approximately 30% more integrated luminosity would be required to compensate for a loss in statistical precision by 15%, corresponding to approximately 1 year of additional running at the highest energy.

4 Hybrid detector-readout technology

In order to meet the vertex-detector requirements discussed in section 2, hybrid-pixel-detector systems are under study, combining fast charge collection through drift in high-field sensors with high-performance readout ASICs. The target thickness for both the sensor and readout layers is only 50 μm each.

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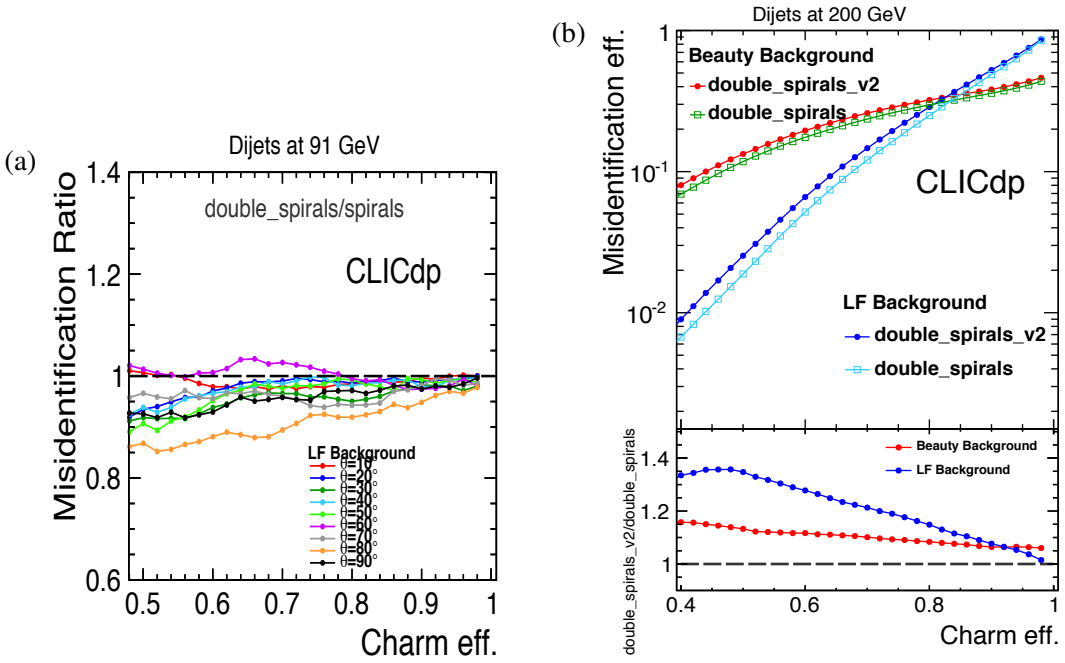

Figure 3: Charm-tagging performance of the double-layer geometry for dijets at 91 GeV. (a): comparison with a single-layer layout in terms of the ratio of the misidentification probabilities for light-flavour background. (b): comparison of the c-tagging performance of dijets at 200 GeV for a double-layer geometry (double_spirals) with a similar geometry with approximately twice the amount of material per detection layer (double_spirals_v2). Misidentification probabilities for beauty and light-flavour background and in the lower part of the figure their corresponding ratios are shown. From [10].

4.1 Thin-sensor assemblies

Planar pixel sensors with 55μm pitch and different thicknesses (50-300 μm) were procured from different vendors and bump-bonded to Timepix [11] readout ASICs (100 and 700 μm thickness). Slim-edge sensor designs (250–450 μm, two guard rings) are compared to designs with active edges (20–50 μm, one guard ring above the edge pixels). Preliminary beam-test results show very good efficiencies in both cases, extending beyond the edge pixels [12]. For 50 μm sensor thickness and nominal readout parameters, the fraction of multi-pixel clusters is approximately 20%. Single-point resolutions of approximately 3 μm have been extracted for clusters of two pixels using charge interpolation and taking into account non-linear charge sharing.

4.2 CLICpix readout chip

The CLICpix hybrid readout chip [13] will be implemented in a 65 nm CMOS process. A CLICpix demonstrator chip has been produced in 65 nm CMOS technology, including a 64×64 pixel matrix and power-pulsing capability. The pixel size is 25 μm$\times$25 μm. Simultaneous 4-bit Time-Of-Arrival (ToA) and Time-Over-Threshold (ToT) measurements are implemented in each pixel, allowing for a front-end time slicing with approximately 10 ns and for measuring the charge to improve the position resolution through interpolation. The full chip can be read out in less than

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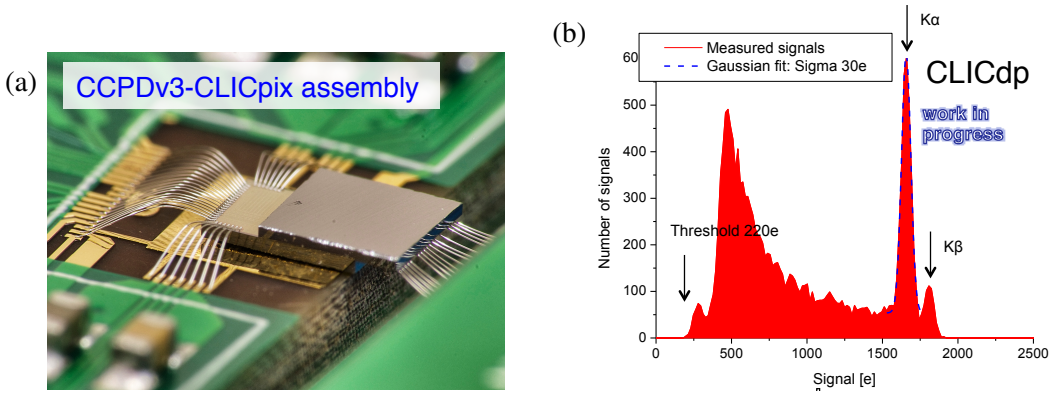

Figure 4: (a): hybrid glue assembly of a CLICpix prototype chip with a CCPDv3 active sensor on top. (b): ^{55}Fe spectrum observed on a single-pixel test output of the CCPv3 chip.

800 μs (for 10% occupancy), using a 320 MHz readout clock and zero suppression. The power consumption of the chip is dominated by the analog frontend with a peak power corresponding to 2 W/cm^2. The total average power consumption can be reduced to a value below the target of 50 mW/cm^2 by means of power gating for the analog part and clock gating for the digital part.

Readout tests have confirmed that the CLICpix demonstrator chip is fully functional and the power consumption and performance are in agreement with simulations [14].

4.3 Active sensors with capacitive coupling

The first hybrid assemblies of CLICpix prototype chips with CCPDv3 active sensors have been produced and tested. The sensors are implemented in a 130 nm high-voltage CMOS process [15]. A deep n-well above the p substrate surrounds low-voltage p-wells and acts as the signal collecting electrode. A nominal operation voltage of -60 V at the n-well results in a depletion layer of approximately 10 μm. The fast drift signal collected in this depletion layer passes through a two-stage transimpedance amplifier in each pixel and the resulting voltage signal is capacitively coupled to the CLICpix ASIC through a layer of glue a few microns thick (figure 4(a)).

Laboratory tests with radioactive sources show a good signal-to-noise performance for the active sensor output (figure 4(b)). Preliminary test-beam results with CLICpix-CCPDv3 assemblies suggest a detection efficiency of $> 99\%$ for minimum ionising particles and a high fraction of single-pixel clusters with a position resolution of approximately 7 μm, as expected for 25 μm pixel pitch.

4.4 Through-Silicon Via (TSV) technology

Through-Silicon Via (TSV) vertical interconnects remove the need for wire bonding connections on the side of the readout ASICs and therefore allow for an efficient tiling to form larger modules with minimal inactive areas.

A “via last” TSV process developed in collaboration with CEA-LETI has demonstrated the feasibility of TSVs on functional detector chips from the Medipix/Timepix chip family [16]. The project uses Medipix3 readout wafers produced in 130 nm CMOS technology. A “via last” process is used that includes thinning of the ASIC wafers to 120 μm and results in vias of 60 μm diameter.

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Tests on the processed wafers show good results, with a low resistivity of the vias ($< 1\ \Omega$) and a sufficient isolation to the outside (leakage current $< 1\ \mu$A at 1 V). Preliminary functional tests on a sub-sample of the chips before and after TSV processing indicate no significant deterioration of the performance.

A continuation of the TSV project with CEA-LETI aims to produce TSV assemblies with Timepix3 ASIC wafers thinned to 50 μm.

5 Detector integration

The detector performance requirements lead to challenging constraints for the mechanical and electrical integration of the vertex-detector components and its cooling system. An integrated approach is followed, addressing several of the critical R&D issues in these domains:

- *Power delivery and power pulsing.* A low-mass power-pulsing and power-delivery system optimised for the small duty cycle of the CLIC machine has been developed [17]. Controlled current sources deliver a low and almost constant current (< 300 mA per ladder) into the vertex region through low-mass cables. The energy needed by the readout ASICs during the time of the collisions and detector readout is stored locally in silicon capacitors. Low-dropout regulators provide the necessary stability of the output voltage for the analog ($\Delta V \approx$ 16mV) and the digital part ($\Delta V \approx 70$mV) of the readout ASICs. Prototypes have been tested successfully with dummy loads emulating the power consumption of the 12 readout ASICs in a half ladder. The total contribution of the powering infrastructure to the material budget of each barrel layer is approximately $0.1\%X_0$. It is expected to decrease to less than $0.05\%X_0$ with evolving silicon-capacitor technology.

- *Cooling.* Even with power pulsing a total power of approximately 500 W will be dissipated in the vertex detectors alone. To limit the amount of material in the vertex-detector region, a cooling system based on forced air flow is under development [18]. Finite-element Computational Fluid Dynamics (CFD) simulations show that air cooling is feasible. For a mass flow of 20 g/s, the temperature increase in the vertex detector is limited to approximately 40 ^{o}C. The proposed cooling scheme is being validated in thermal mockups. Preliminary results confirm the validity of the simulations.

- *Mechanical supports.* The low overall material budget leaves only about $0.05\%X_0$ per detection layer for mechanical supports. Prototypes based on Carbon-Fibre-Reinforced Polymers (CFRP) are under study. Bending-stiffness calculations are validated in finite-element simulations and with bending tests. Measurements within the thermal mockup show that the induced vibrations are at an acceptable level of approximately $1-2\ \mu$m RMS amplitude for the direction perpendicular to the detector plane and at nominal flow conditions.

- *Assembly and access scenarios.* Assembly and access scenarios for in-situ testing have been developed, taking into account the constraints from the surrounding detector elements. Realistic cabling layouts are proposed and evaluated in terms of their impact on the global and local material budget.

6 Conclusions

The precision physics requirements at CLIC pose challenging demands on the performance of the vertex detector system. Full-simulation flavour-tagging studies have been performed to assess the influence of the detector design on the physics performance and to optimise the proposed detector layouts. A broad hardware R&D program is in place, addressing the challenges for the CLIC vertex detector in an integrated approach.

References

[1] T. Behnke et al., *The International Linear Collider: technical design report. Volume 1*, CERN-ATS-2013-037 (2013).

[2] M. Aicheler et al., *A multi-TeV linear collider based on CLIC technology: CLIC conceptual design report*, CERN-2012-007 (2012).

[3] L. Linssen et al., *Physics and detectors at CLIC: CLIC conceptual design report*, CERN-2012-003(2013).

[4] P. Lebrun et al., *The CLIC programme: towards a staged e^+e^- linear collider exploring the terascale, CLIC conceptual design report*, CERN-2012-005 (2012).

[5] D. Dannheim and A. Sailer, *Beam-induced backgrounds in the CLIC detectors*, LCD-Note-2011-021 (2011).

[6] *LCFIPlus*, https://confluence.slac.stanford.edu/display/ilc/LCFIPlus.

[7] S. Redford, P. Roloff and M. Vogel, *Physics potential of the top Yukawa coupling measurement at a* 1.4 *TeV Compact Linear Collider using the CLIC SiD detector*, CLICdp-Note-2014-001 (2014).

[8] P. Roloff and J. Strube, *Measurement of the top Yukawa Coupling at a* 1 *TeV International Linear Collider using the SiD detector*, LCD-Note-2013-001 (2013).

[9] K. Agashe et al., *Snowmass 2013 Top quark working group report*, (2013).

[10] N. Alipour Tehrani and P. Roloff, *Optimisation studies for the CLIC vertex-detector geometry*, CLICdp-Note-2014-002 (2014).

[11] X. Llopart et al., *Timepix, a 65k programmable pixel readout chip for arrival time, energy and/or photon counting measurements*, *Nucl. Instrum. Meth.* **A 581** (2007) 485.

[12] S. Redford, *R&D for the Vertexing at CLIC*, CLICdp-Conf-2014-008 (2014).

[13] P. Valerio, R. Ballabriga and M. Campbell, *Design of the 65 nm CLICpix demonstrator chip*, LCD-Note-2012-018 (2012).

[14] P. Valerio et al., *A prototype hybrid pixel detector ASIC for the CLIC experiment*, CLICdp-Conf-2013-003 (2013).

[15] I. Peric et al., *High-voltage pixel detectors in commercial CMOS technologies for ATLAS, CLIC and Mu3e experiments*, *Nucl. Instrum. Meth.* **A 731** (2013) 131.

[16] D. Henry et al., *TSV last for hybrid pixel detectors: application to particle physics and imaging experiments*, talk given at the 63rd *IEEE Electronic Components and Technology Conference (ECTC)*, May 28–31, Las Vegas, U.S.A. (2013).

[17] G. Blanchot, D. Dannheim and C. Fuentes, *Power pulsing schemes for vertex detectors at CLIC*, CLICdp-Conf-2013-005 (2013).

[18] F. Duarte Ramos, H. Gerwig, M. Villarejo Bermudez, *CLIC inner detectors cooling simulations*, LCD-Note-2013-007 (2013).

2015 JINST 10 C03025