Trigger **D**ata **S**erializer ASIC Chip for the ATLAS New Small Wheel sTGC Detector

Jinhong Wang[1],

On behalf of the ATLAS Muon Collaboration

[1]University of Michigan

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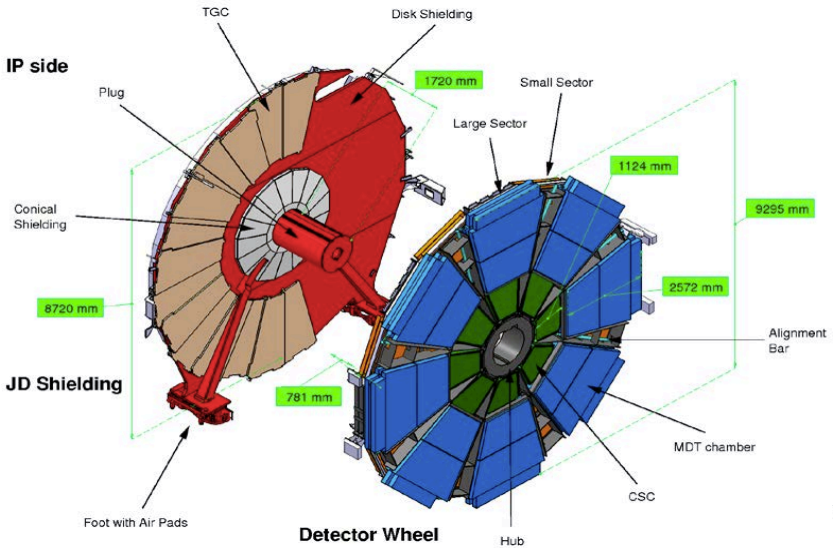
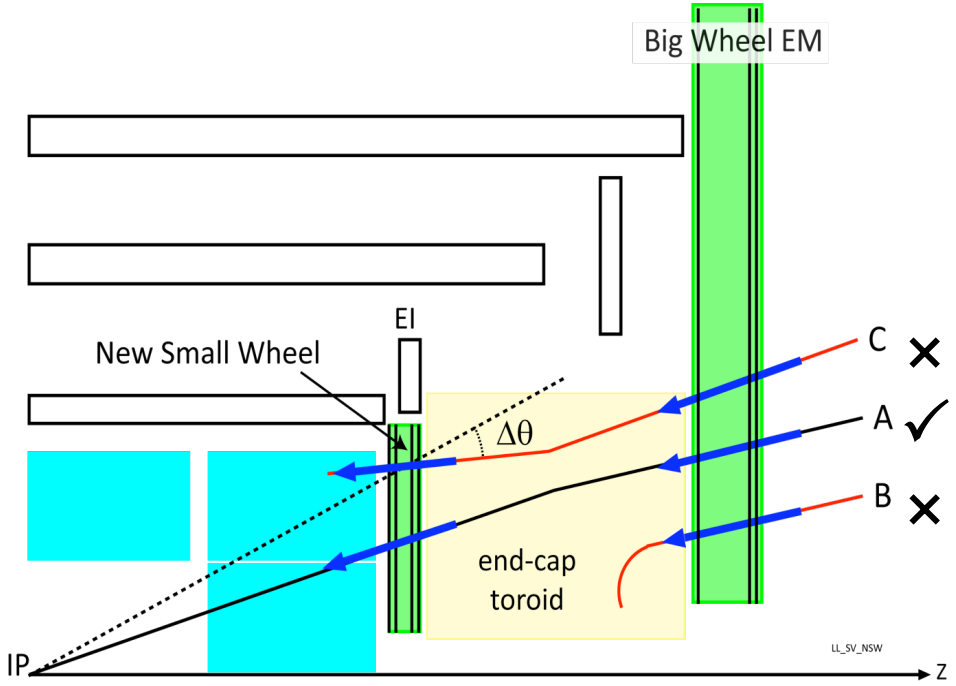
Outline

- Background: Overview of Trigger Data Serializer (TDS) in sTGC trigger
- Design of TDS
  - strip-TDS as an example
  - first prototype of TDS (TDS version I: TDSVI)
  - Parameters on TDSVI
- The Serializer in TDSVI: GBT-SER-DM
  (The GBT Serializer in IBM 130 nm CMOS DM323 Metallization)
  - Architecture of GBT-SER-DM
  - Prototype of GBT-SER-DM
  - GBT-SER-DM performance
  - A stable, fixed latency link with TDS Serializer and serial protocol
- Conclusion

NSW trigger concept

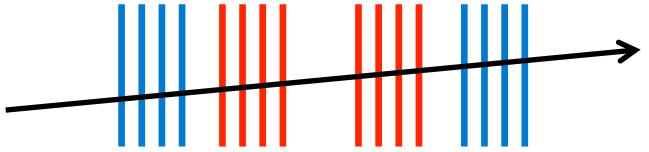
- Phase I upgrade: Increased backgrounds, but must maintain existing trigger rate
- Filter "Big Wheel" muon candidates to remove tracks that are not from the IP
  Only track "A" should be a trigger candidate: pointing: $\Delta\theta < \pm 7.5$mrad





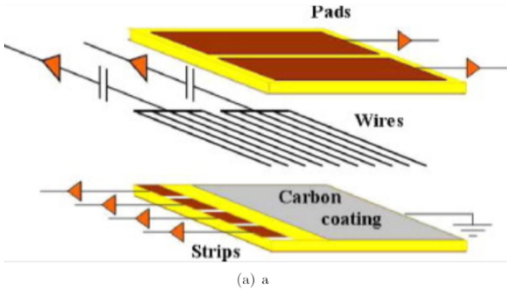
New Small Wheel – defines basic layout and envelopes

- 16 detector layers in total
- 2 technologies, **MicroMegas** and **sTGC**



sTGC trigger scheme

1/16th sector



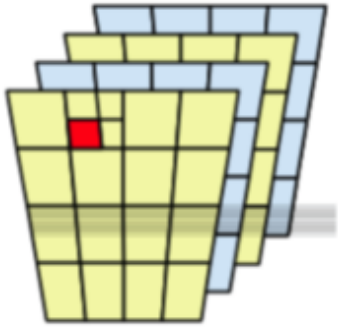
On Rim of NSW FPGAs

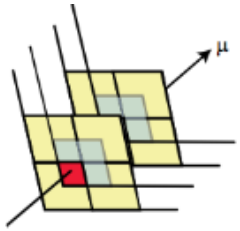
Pad Trigger

Router

USA 15

sTGC Trigger Processor





sTGC

Pad VMM

Pad TDS

Strip VMM

Strip TDS

Strip VMM

Strip TDS

one Strip TDS chosen

On-chamber ASICS

Problem: no BW to read all strips

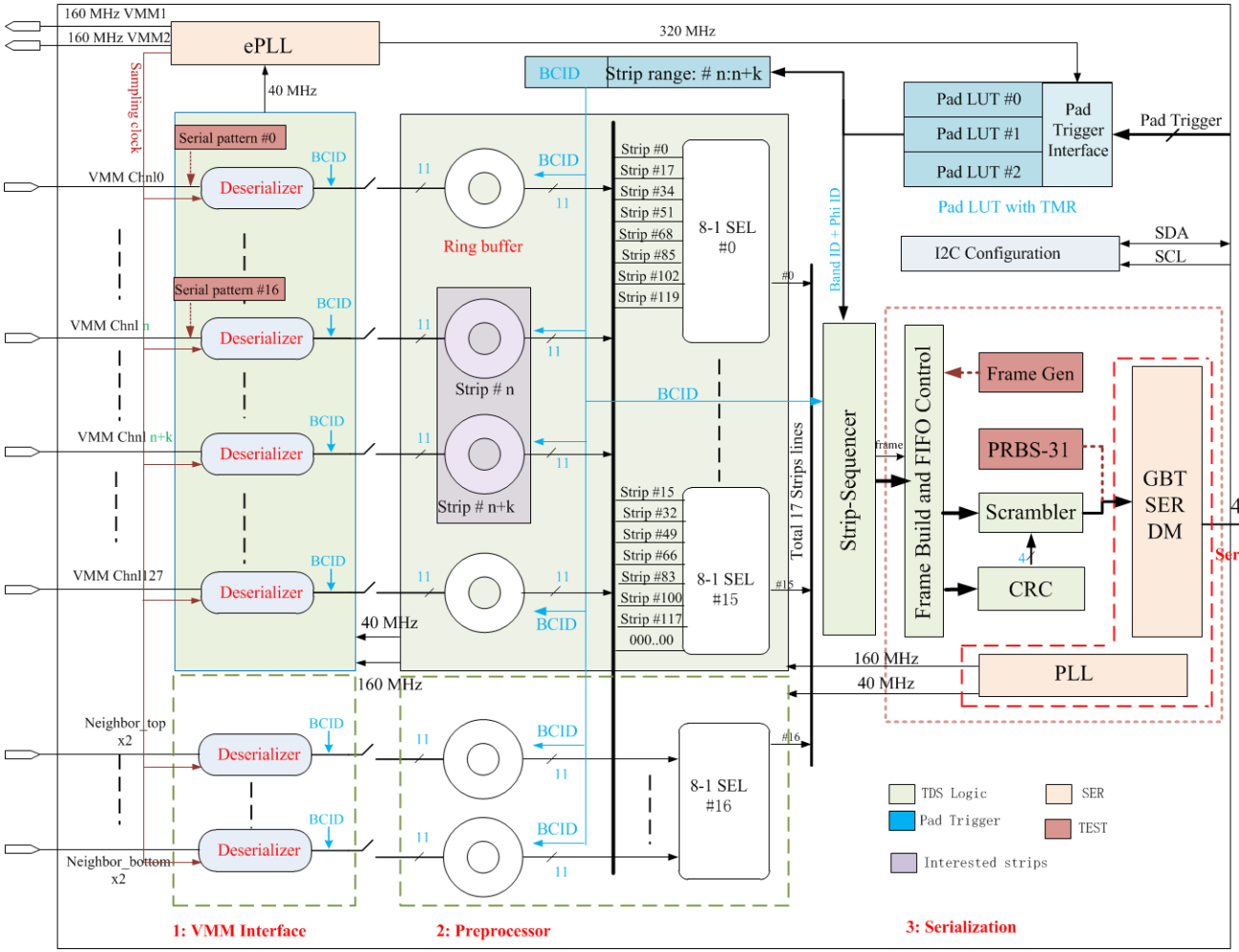
Pad trigger uses pad tower coincidence to choose ONLY the relevant band of strips.

Physical pads staggered by ½ pad in both directions

Logical pad-tower defined by projecting from 8 layers of staggered pad boundaries

Pad-tower coincidence = 2 × 3-out-4 overlapping pads

Design of TDS : strip-TDS



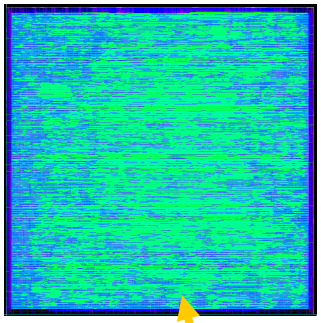
TDS: for strips, pads

- ❑ IBM 8RF-DM 323, 130 nm CMOS; 1.5 Volt supply
- ❑ Each strip-TDS:
  - 128 channels, covering strips from 2 VMMs
    - add BCID for each strip
    - programmable delay for BCID clk
  - Accept pad Trigger, select matching strips
  - Send out strips charge via SER @ 4.8 Gbps per trigger
- ❑ Each pad-TDS:
  - 96 channels, covering 96 pads from (2) VMMs.
  - Sample and Time-stamp pad inputs (96 pads)
  - Send out yes/no info of pads at 4.8 Gbps each BC

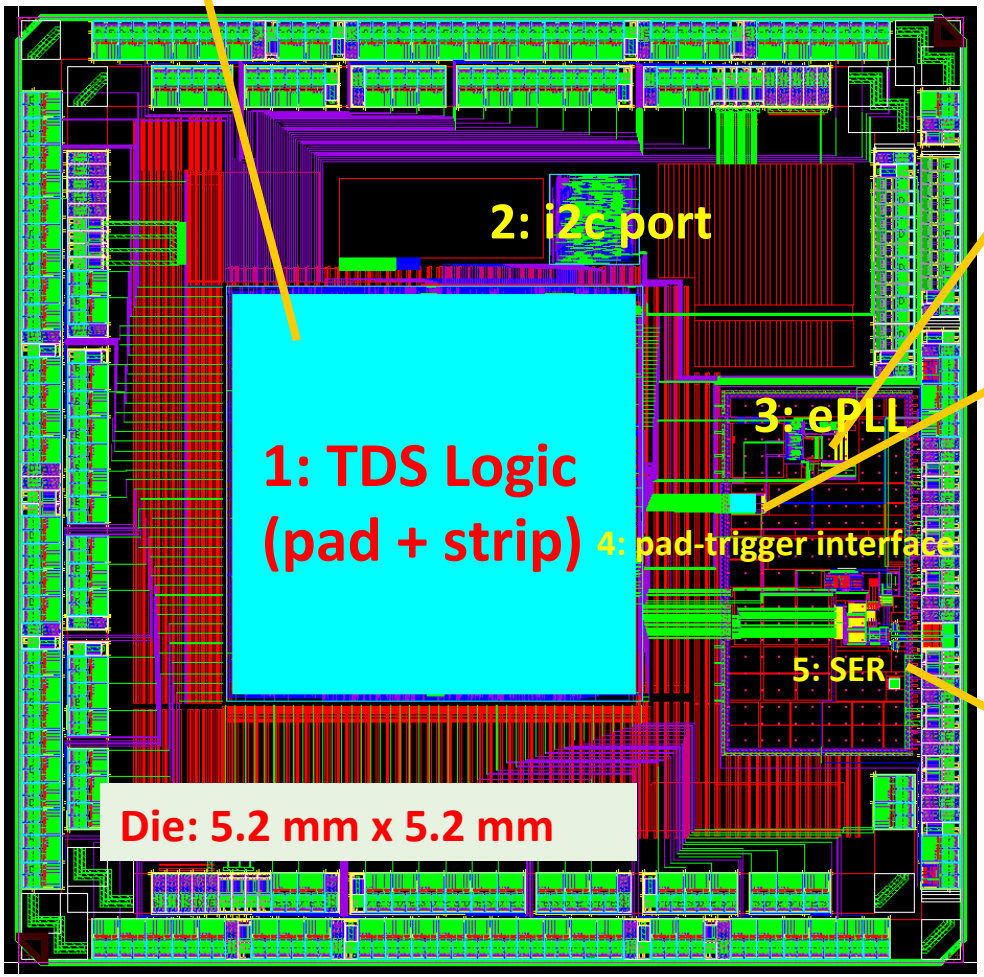
- Three parts: VMM interface, Preprocessor, Serialization
- Challenges in design include: large number of inputs, short latency required , low power consumption, radiation tolerant, etc.

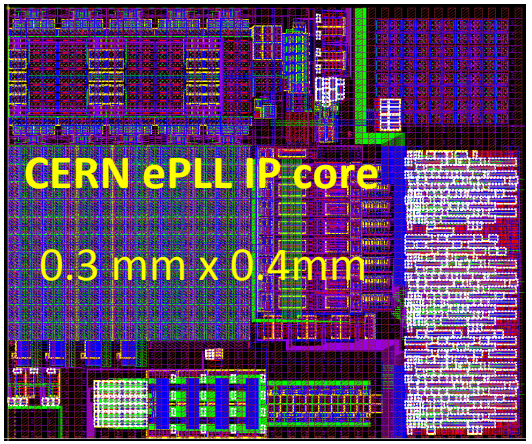
First Prototype of TDS: TDSVI

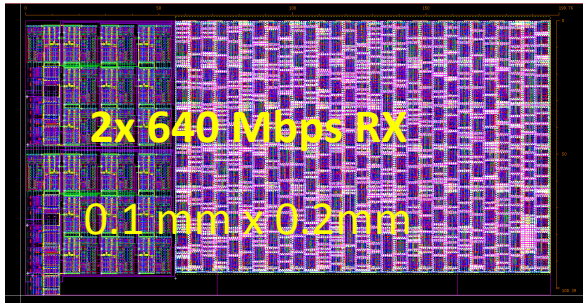
2.3 mm x 2.3 mm

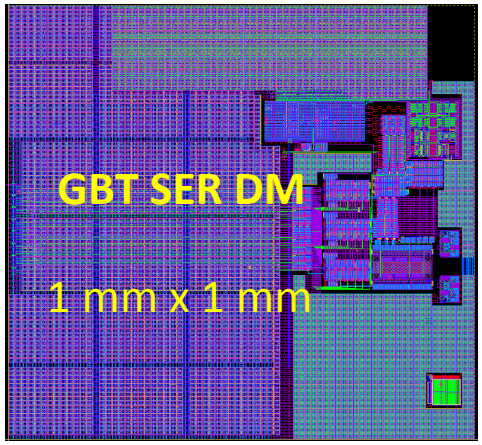


Type	Instances	Area	Area %
sequential	47081	1387708.800	46.7
inverter	13335	80242.560	2.7
buffer	1455	16752.000	0.6
logic	104516	1489987.200	50.1
total	166387	2974690.560	100.0









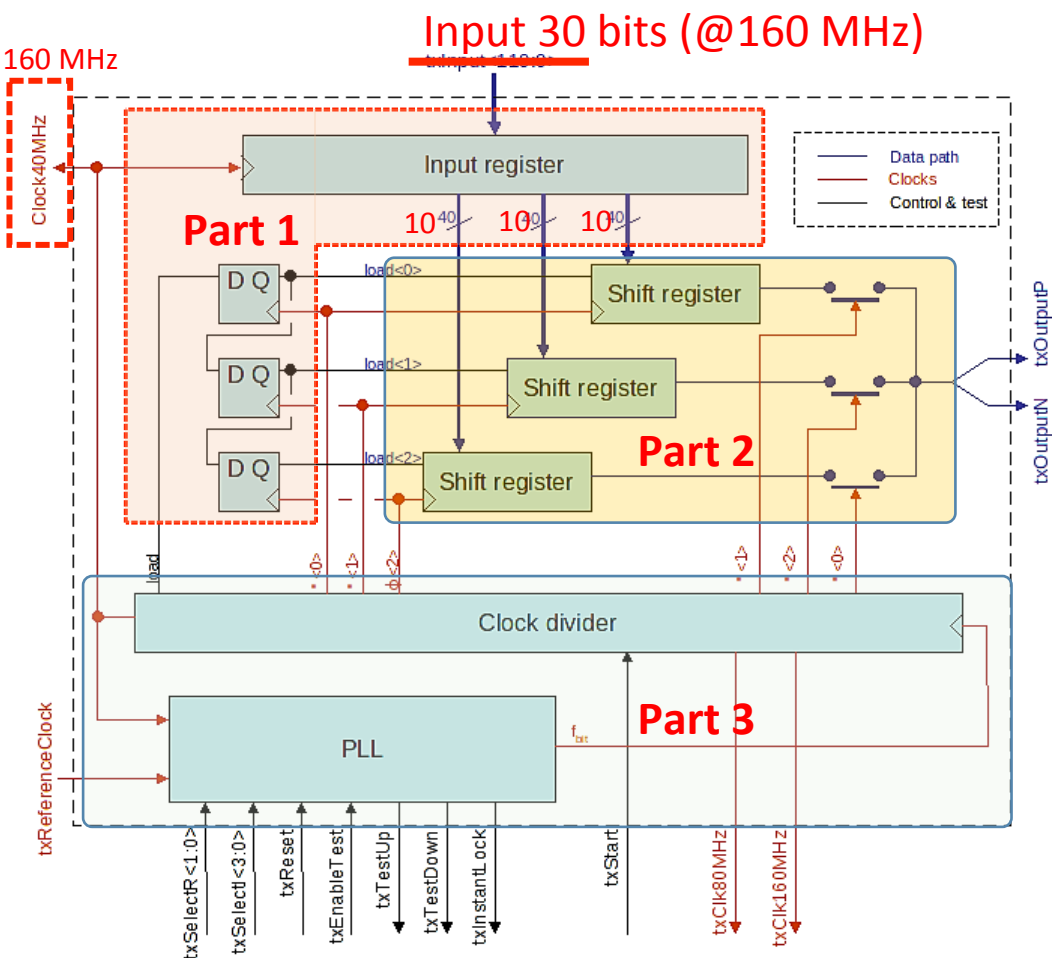
Power, Latency, Package and Current Status

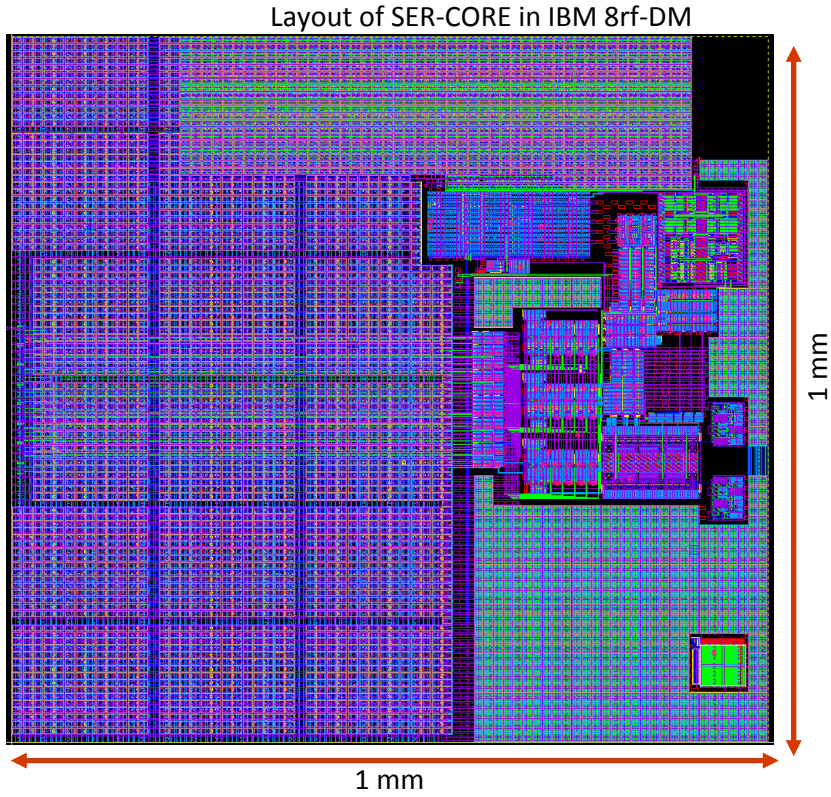
- Total deliverables: design, prototype, production and test of 3,700 TDS chips.
- The total power of one TDS < 1 W:
  digital ~ 300 mW (estimated) + SER 300 mW (tested) + IO 150 mW (estimated) + other
- Strip-TDS latency (<100 ns, estimation from simulation)

  – 18.75 ns for BCID and pad trigger matching
  – 12.5 ns to re-align all selected strips after 8-1 sequencers
  – 12.5 ns for trigger data preparation and format
  – 6.25 for buffer the trigger data for ping-pong FIFO
  – 6.25 ns for scrambler and CRC
  – 4 ns for serializer
  – *22 ns* to deserialize the pad trigger data and decode trigger information
  – 12.5 ns to access pad Look-up-Table (LUT) and find the starting strip address

- Wire-bond BGA, 400 pins, 1 mm pitch
  Package is currently under design at I2A, INC.
- Design submitted on August 18 (MOSIS MPW), Die expected back in mid-Nov.
  Design of Test-board is in progress.

The Serializer in TDSVI: GBT-SER-DM





With respect to the CERN GBT SER IP core:

1: The metallization is converted from IBM 8RF LM62 to IBM 8RF DM323

2: Changes to Part I

❖Instead of running at 40 MHz to load 120 bits, we run at 160 MHz to load 30 bits

❖In this way, the waiting time is reduced to 6.25 ns for 160 MHz

And could seamless interface the logic part which works at 160 MHz

Changes to Part 2

❖Reduce the length of each shift register from 40 bits to 10 bits

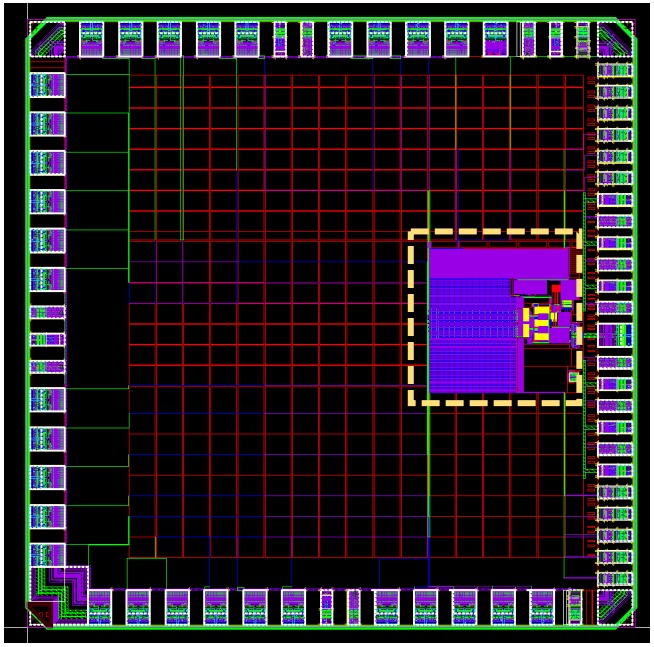
No changes on Part 3

GBT-SER in DM core:

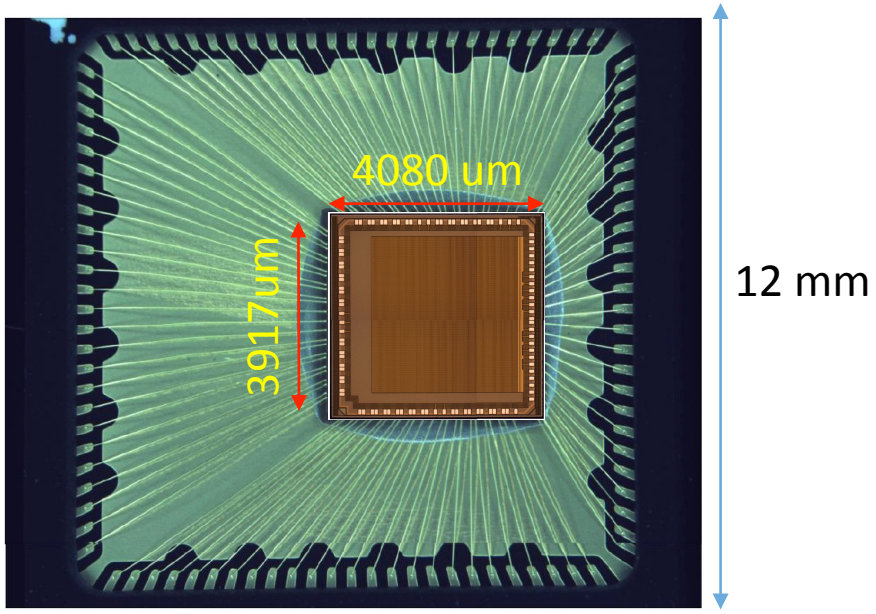
- 1 mm x 1mm ,
- 1.5 Volt ; 300 mW power
- Line rate: 4.8 Gbps, Ref Clk: 40 MHz

A prototype of this core was submitted with VMM2, and tests have been done at UM

Prototype of GBT-SER-DM

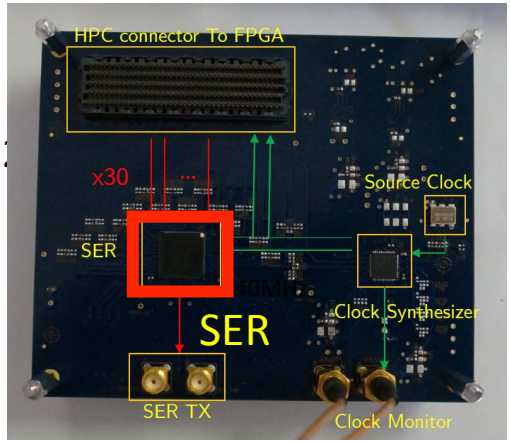


die of Serializer prototype

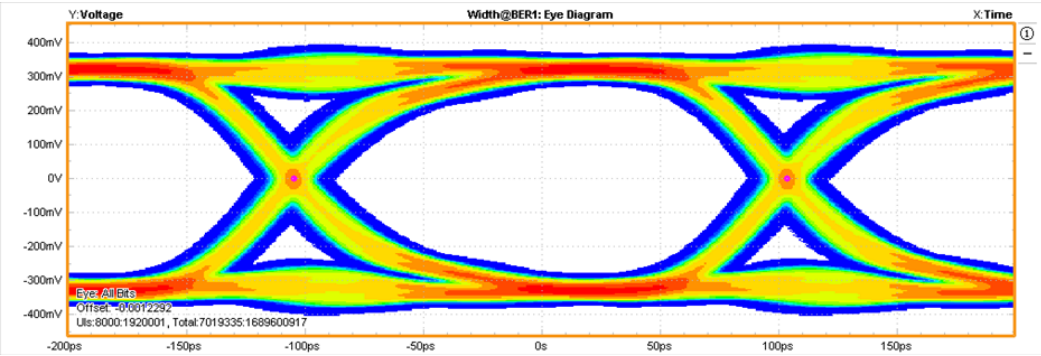


Bonding diagram of die to QFN100

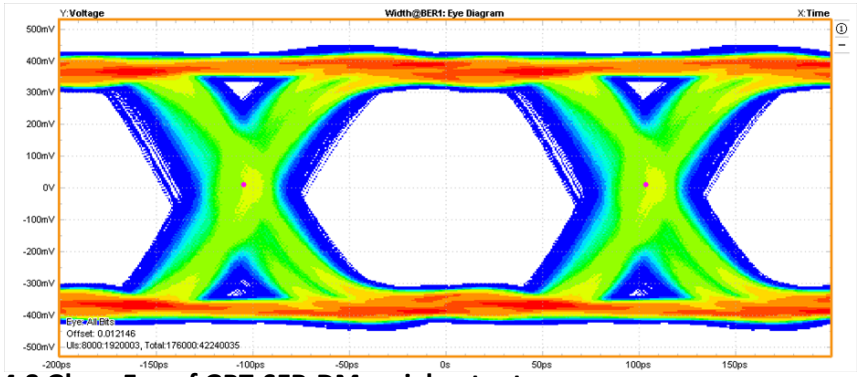
- A recent prototype went with BNL ASD chip (VMM
  submitted at Jan. 31st, 2014
- Serializer core:
  ~1mm ^2, 300 mW power, 1.5 Volt supply
- Prototype in a QFN 100 Package



Performance of GBT-SER-DM



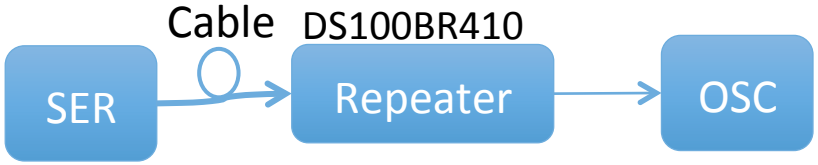
4.8 Gbps: Eye of GBT-SER-DM serial output without repeater

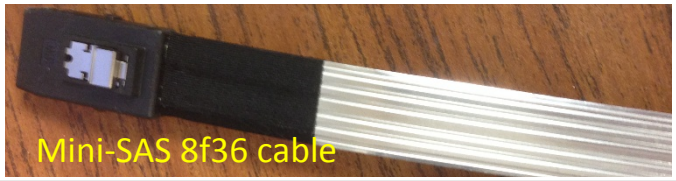


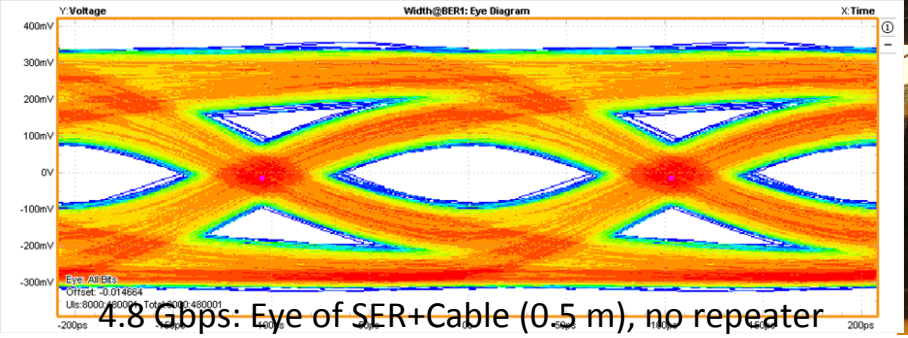
4.8 Gbps: Eye of GBT-SER-DM serial output after 4 m mini-SAS 8F36 cable with repeater

	TJ (ps)	RJ(ps)	DJ(ps)	PJ(ps)	Width@BER (ps)*	Height (mV)
SER	**49.73**	3.351	9.869	*9.869*	**158.6**	~600
SER+Cable+Repeater	**145.97**	10.482	11.175	*11.175*	**62.364**	612.37

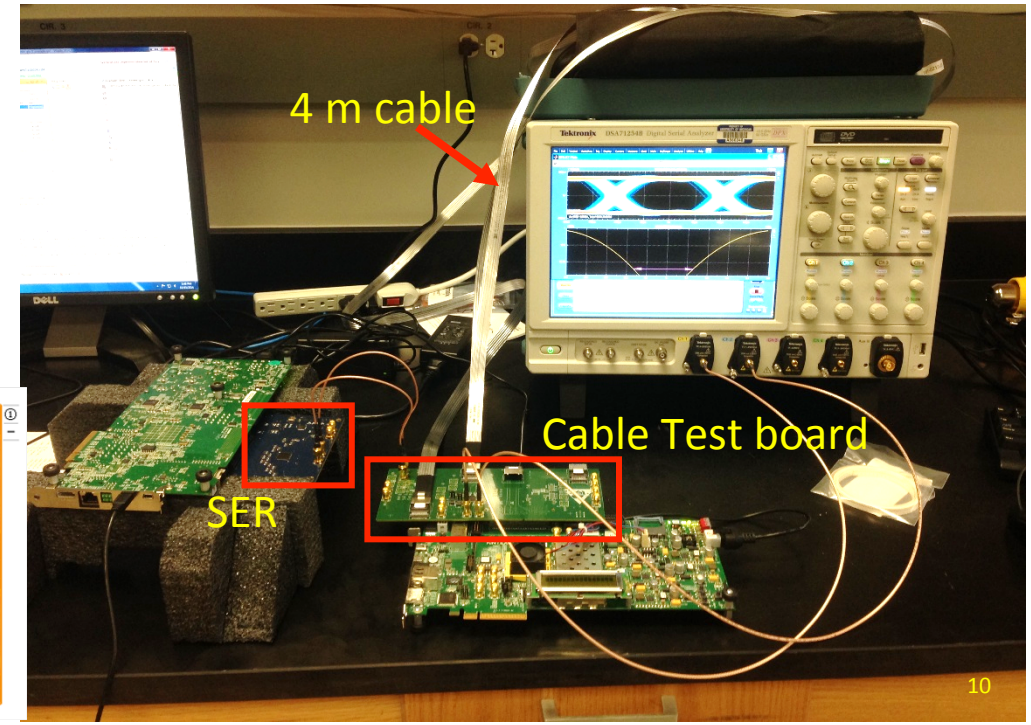
*: For BER = 1E-12, tests done with PRBS-31







4.8 Gbps: Eye of SER+Cable (0.5 m), no repeater



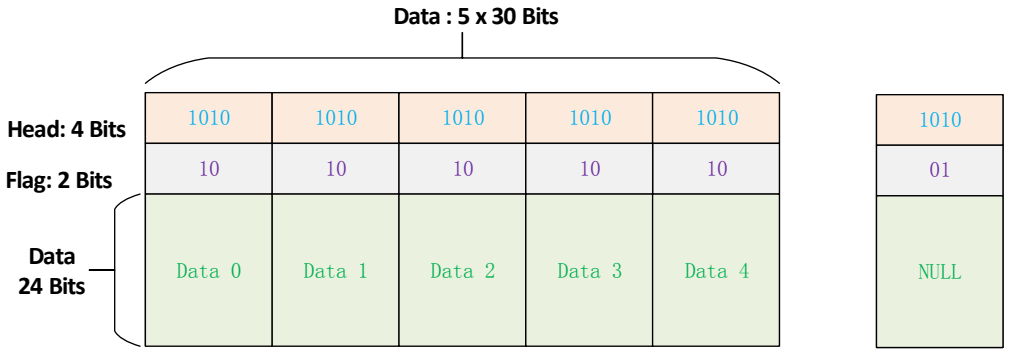
A stable fixed latency link with TDS Serializer

# bits	Data field
12	BCID
8	Band-ID
5	Phi-id
4	Checksum or CRC
29	Total

Field	15 strips with Hi/Low
Hi/Low	1
Hit map	
# strips	15
Strip data	90
Total length	120=29+1+90

- Data: 120 bits / trigger
- Need additional bits for building a stable serial link with router

120 bits of data occupied 4 frames of 30 bits, plus additional serial overhead, At least we need 5 frames to send out all the info.



Example of a data frame

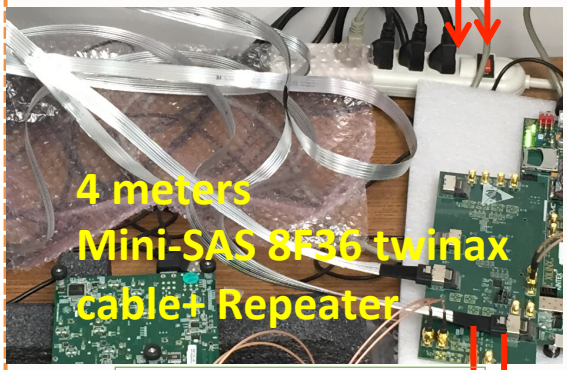
a NULL frame

At the presence of a valid pad trigger
- Use five 160 MHz clks to send out all data from a pad trigger, 30 bits/frame
- When no pad trigger appears
  Send out a NULL packet (30 bits)

A Null packet is only 30 bits length: shorter latency

- header: 1010 for establishing link;
- flag “10” and “01” used for router to quickly identify data or NULL: cutting through switching
- 24*5 bits data are scrambled to be DC balanced
- Scrambler: G(x) = 1+ x^39+x^58

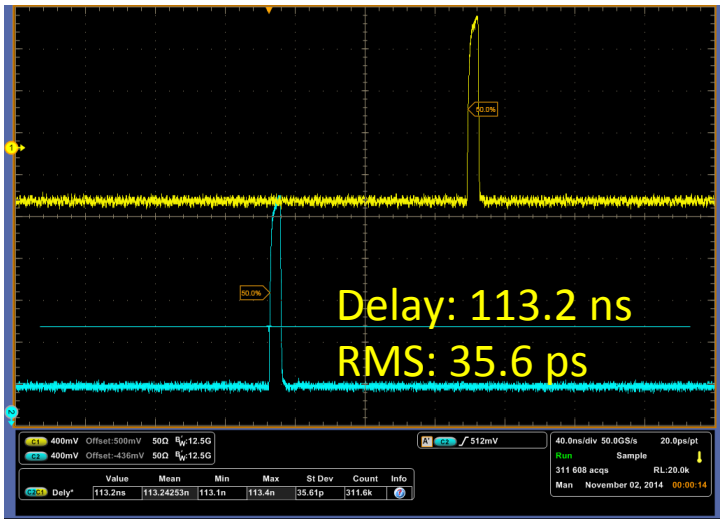
A stable fixed latency link with TDS Serializer



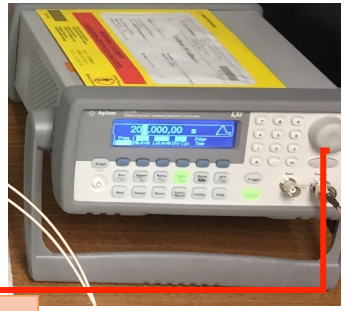
1 meter SMA cable

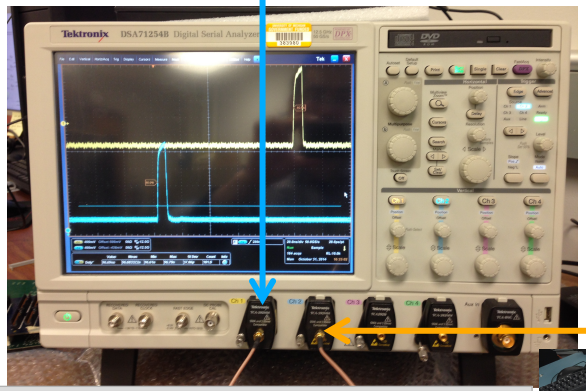
KC705 board

Test Pattern Generator → Scrambler → TDS- SER → cable → Repeater



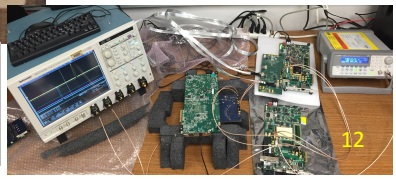
Artix-7 GTP RX → Packet Syn → Descrambler → Packet Analyzer





Reset

Latency includes: (RX end: ~ 60 ns)
TX: ~22 ns + 25 ns cable+ 6.25 ns Reading time



Conclusions and Outlook

Conclusions:

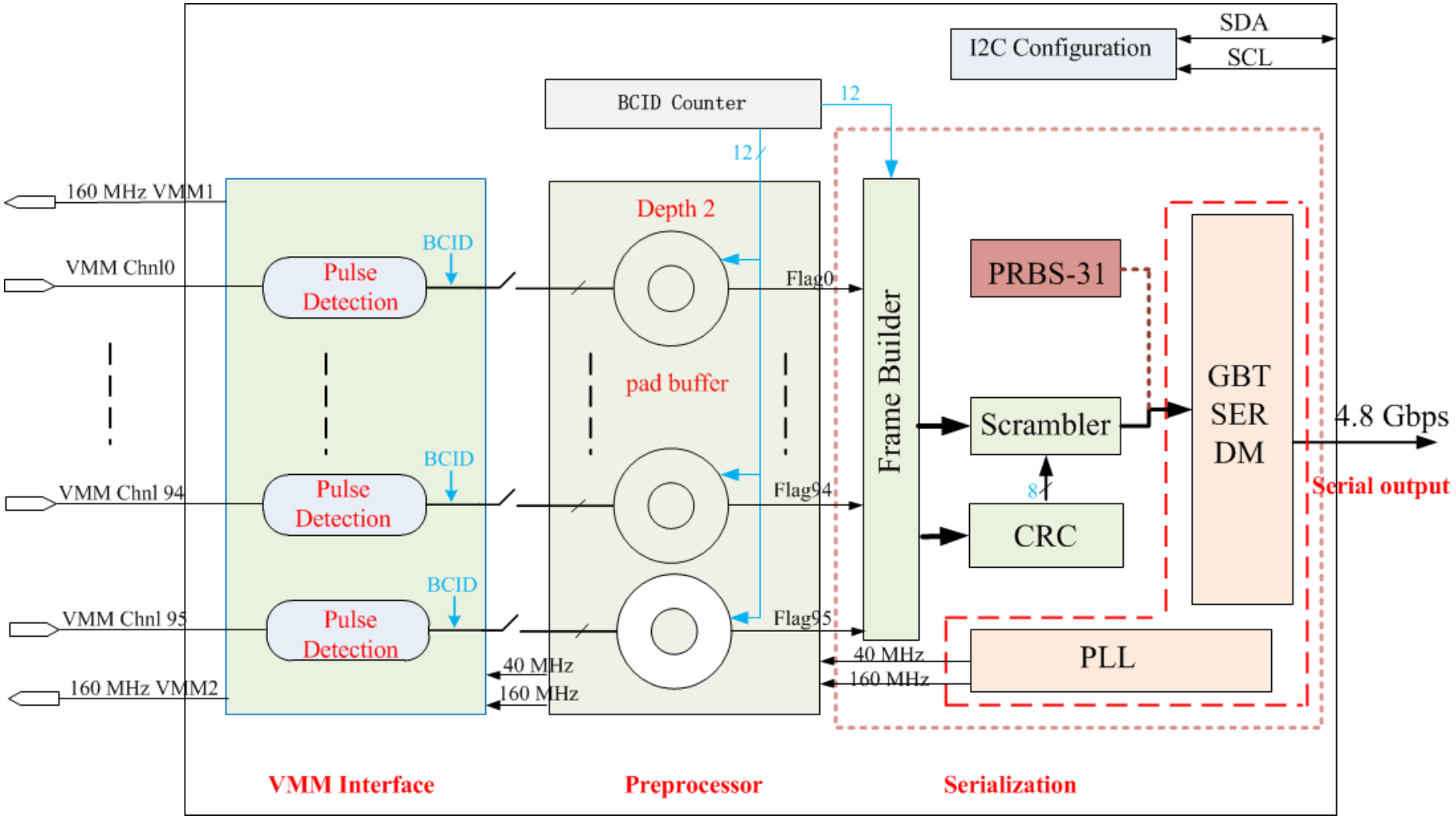
- ✓ Design of TDS has been done.
- ✓ A first Prototype of TDS has been submitted, and currently in design of its BGA package
- ✓ Successfully converted the CERN GBT SER to be used in TDS
- ✓ A prototype of TDS Serializer-only chip has been done, and good performance is demonstrated
- ✓ A stable and fixed latency link has been established with TDS protocol and its embedded Serializer core

Future work:

- ❑ Lab-test of TDS first prototype
- ❑ Radiation test of TDS
- ❑ TDS chip test in real detector setup with VMM2
- ❑ Aiming for a second prototype of TDS: TDSVII

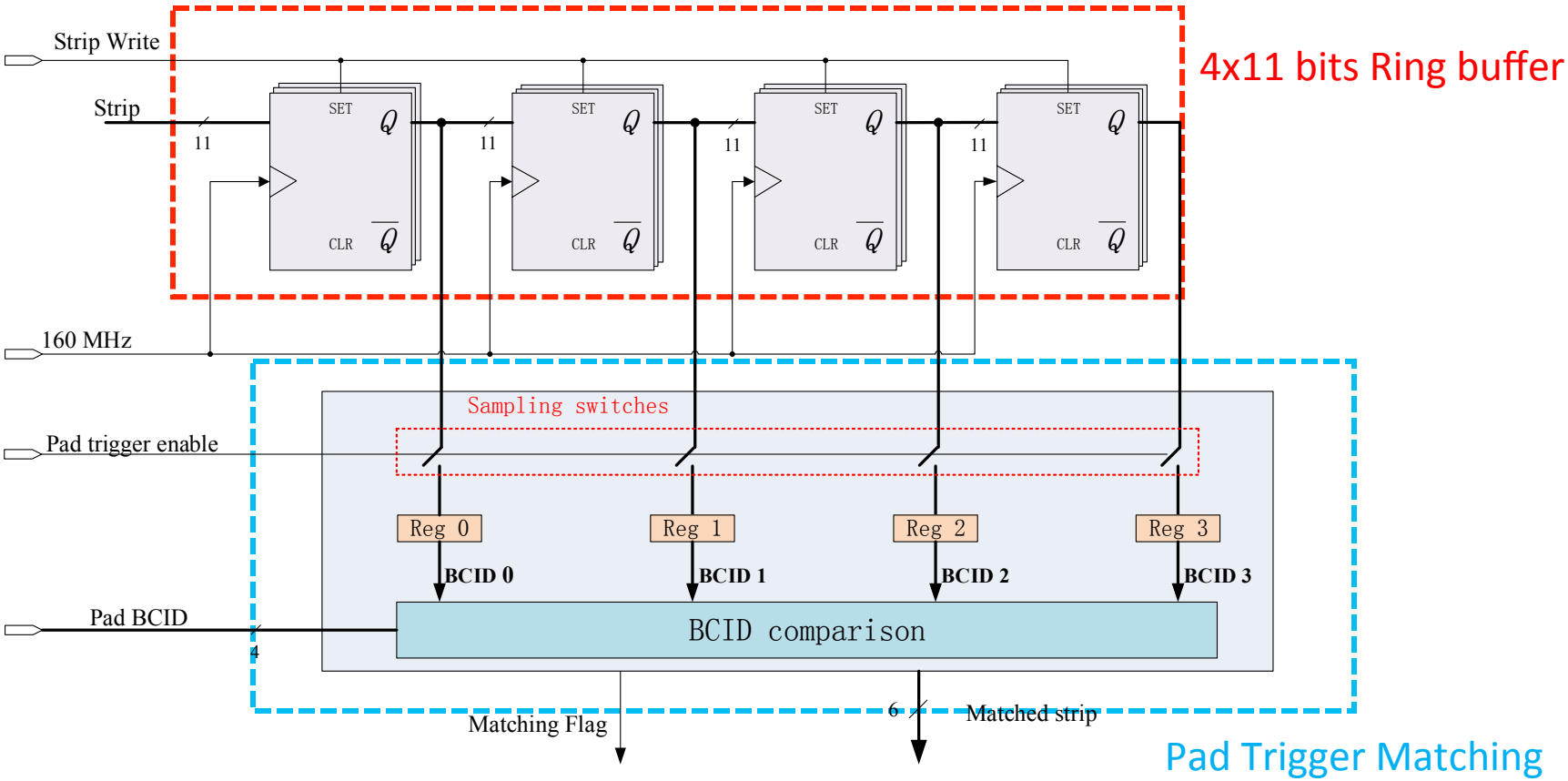
Back up materials

Block diagram of pad-TDS



- Three parts: VMM interface, Preprocessor, Serialization
- Pulse Detection: detects pad pulses from VMM, and latches BCID
- Preprocessor: compare the current BCID with the BCID of pad pulse, to assign yes/no info
- Share the same SER interface with pad-TDS : Scrambler/CRC are not exactly the same but similar

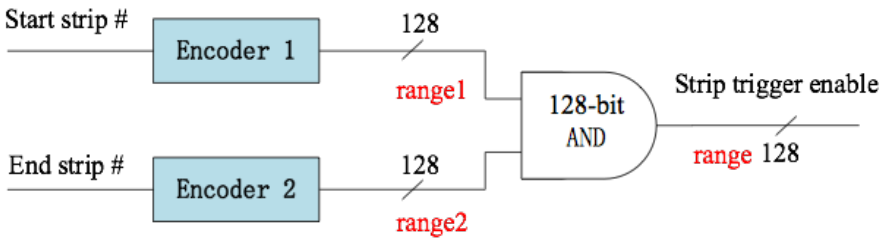
Ring buffer and Trigger matching unit



- Use shift registers to avoid manual control of memory locations manual control of the memory locations would suffer from SEU
- Upon trigger, contents of four mem locations in a channel will all be read and compared against the BCID provided.

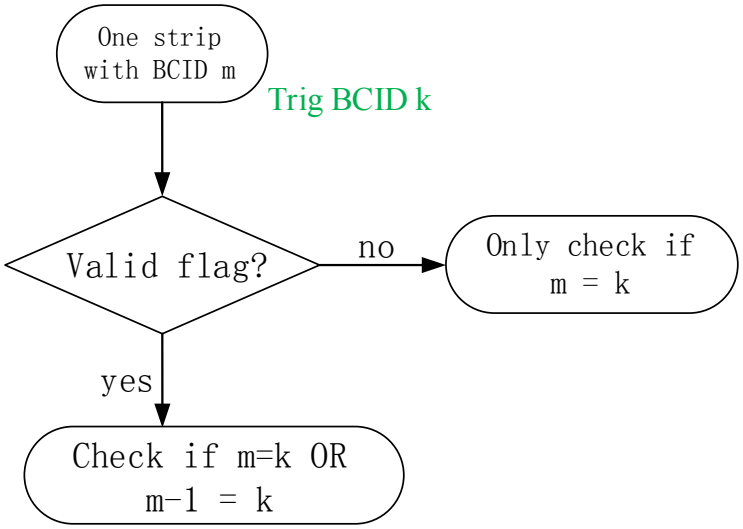
Preprocessor (2): Trigger matching algorithm

- Upon trigger, the range of interested strips are specified as following:



Example: start strip: 10, end strip : 26

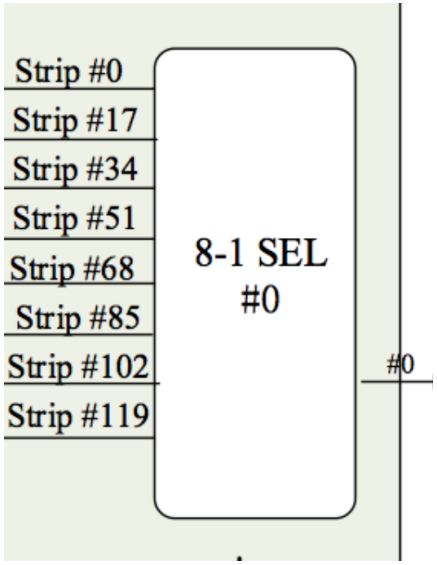
	0	1	2	···	8	9	10	11	···	24	25	26	27	28	···	126	127
range1:	0	0	0	···	0	0	1	1	···	1	1	1	1	1	···	1	1
range2:	1	1	1	···	1	1	1	1	···	1	1	1	0	0	···	0	0
range :	0	0	0	···	0	0	1	1	···	1	1	1	0	0	···	0	0



- In BCID comparison of trigger BCID with strip-BCIDs in the ring buffer:
  if a strip with a BCID flag 'invalid', exact BCID matching will be done
  if a strip with a 'valid' BCID flag, the BCID comparison is done as:
  e.g., a strip with BCID m, and BCID flag = 1, trigger BCID is k,
  we will compare both m with k and m-1 with k in this case, respectively.
  if in either case there is a match, we output it.
- This is because a strip with BCID m and flag =1, may also belong to the previous cycle (BCID m-1)
- Set matching window to 25 ns can turn this function off.

Preprocessor (3): 8-1 selector and sequencer

- 132 chnls are arranged in 17 groups, each group has 8 strips
- For the 8 strips in a group, they are arranged from the 132 chnls by every 17 strips
  e.g, denoted 132 chnls as strip #0- strip #131, in the first group there are: strip #0, #17, # 34 … #119
- The reason for the above arrangement is: we only send out 17 consecutive strips per trigger,
  With the above scheme, there will only be one valid strip at most in each group.
- A sequencer follows the 8-1 selector to maintain the nature sequences of the strips

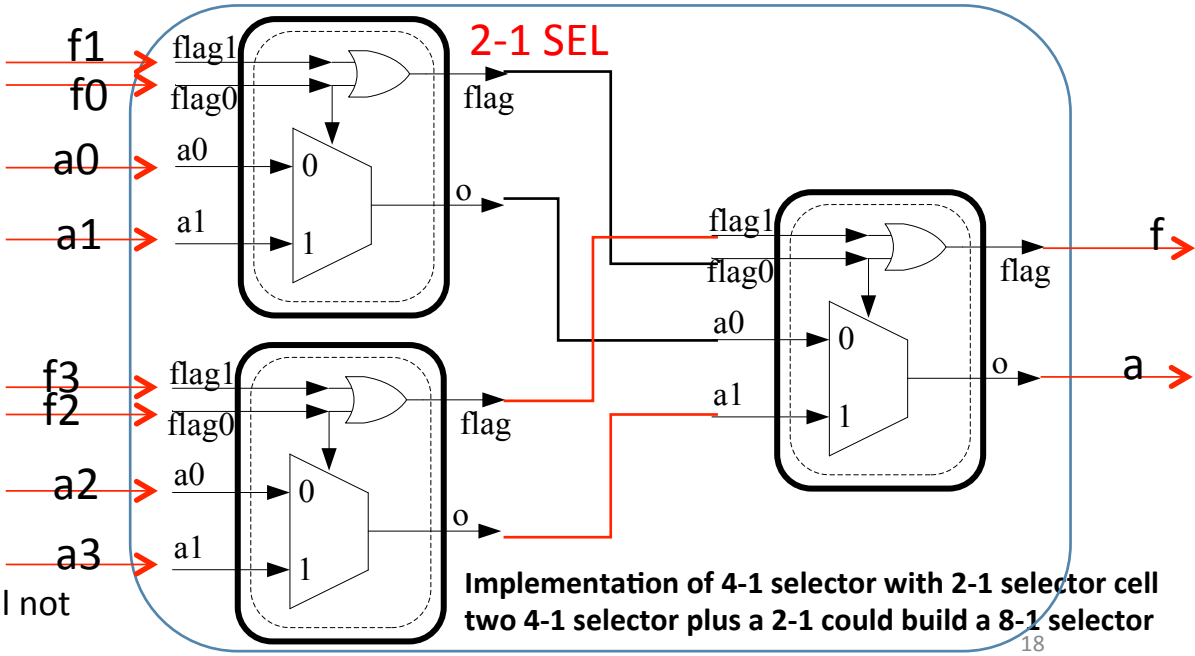


e.g., for interested strips #15- #31,
The output sequence from the 17 8-1 SELs is:
#17, #18, …, #31, #15,#16. (from Sel0-Sel16)

Sequencer will "correct" the order so there will not be confusion to the following circuits

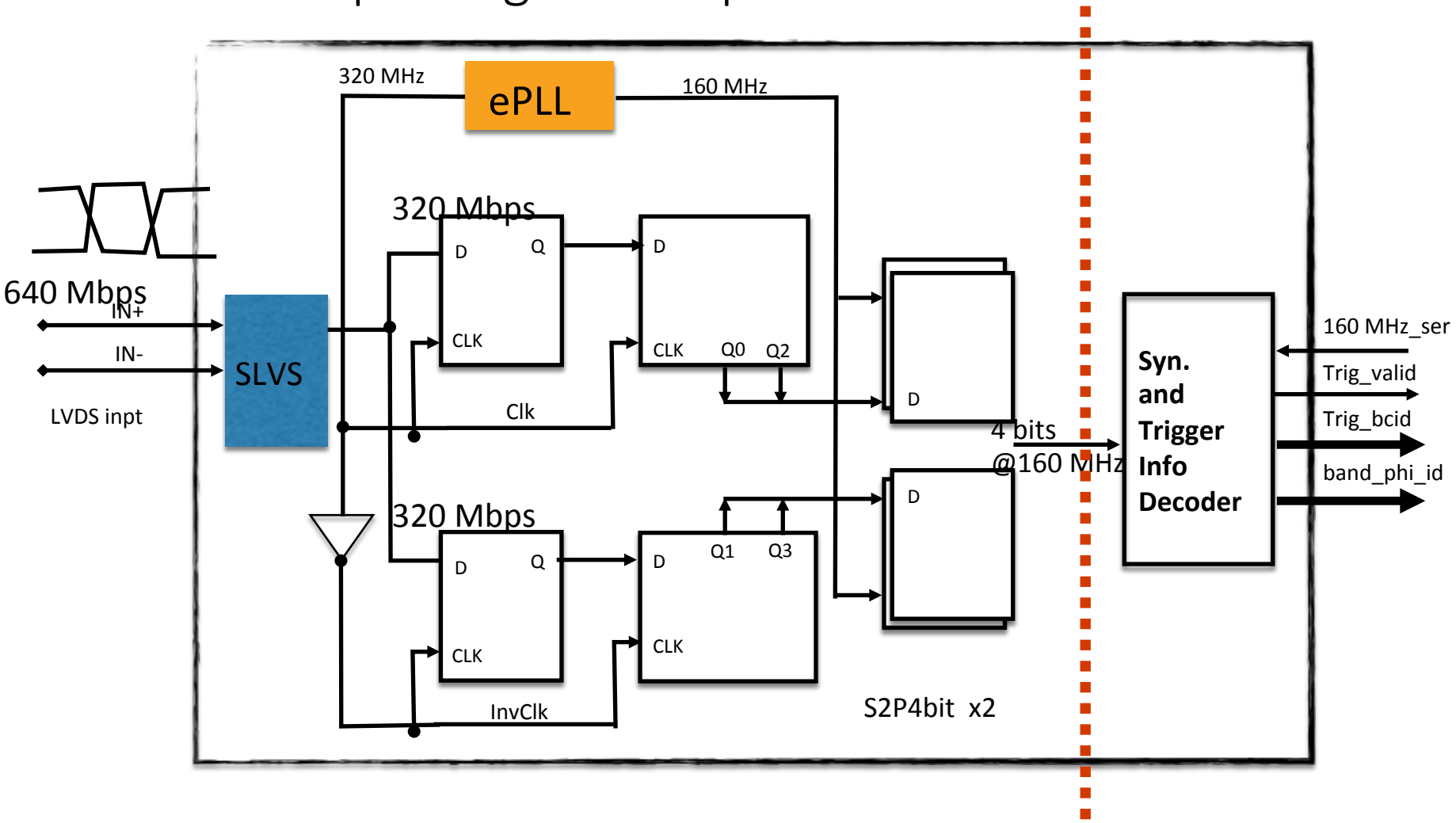
2-1 Priority Sequencer Truth Table

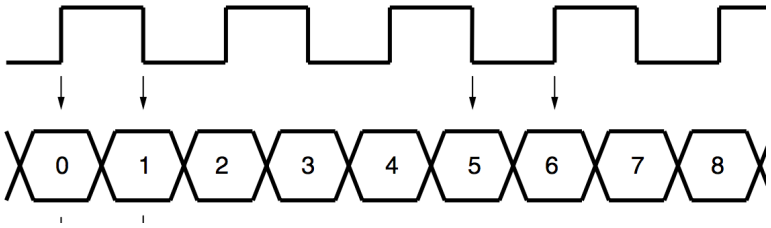
a0	a1	flag0	Flag1	o	flag
x	x	1	x	a0	1
x	x	0	1	a1	1
x	x	0	0	a1	0



Implementation of 4-1 selector with 2-1 selector cell two 4-1 selector plus a 2-1 could build a 8-1 selector

pad-logic to strip-TDS interface





Data format

Line 0	**"10"**	**12 bits trigger BCID**	**2 bits float**
Line 1	**"10"**	**13 bits phi ID + band ID**	**1 bit float**