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Development of precision Time-Of-Flight electronics for LHCb TORCH

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ABSTRACT: The TORCH detector is proposed for the low-momentum particle identification upgrade of the LHCb experiment. It combines Time-Of-Flight and Cherenkov techniques to achieve positive $\pi/K/p$ separation up to 10 GeV/c. This requires a timing resolution of 70 ps for single photons. This paper reports on the electronics developed for such measurements, using commercial Micro Channel Plate (MCP) devices and custom ASICs (NINO and HPTDC). The intrinsic timing resolution of the electronics measured with electrical test pulses is 40 ps. With the MCP photon detector and a pulsed laser, a resolution of 90 ps has been recorded in laboratory tests and 130 ps in test beams.

KEYWORDS: Particle identification methods; Cherenkov detectors; Timing detectors; Photon detectors for UV, visible and IR photons (vacuum)

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1 Introduction

The Time Of internally Reflected Cherenkov light detector (TORCH) [1] is proposed for the low-momentum particle identification upgrade of the LHCb experiment [2]. In this detector, Time-Of-Flight (TOF) and Cherenkov techniques are combined to achieve positive $\pi/K/p$ separation up to 10 GeV/c. Cherenkov photons are generated from a 1cm-thick quartz plate, which is segmented into small identical modules as shown in figure 1. These photons propagate by total internal reflection to the edge of the plate. Subsequently, they are focused to an array of Micro Channel Plate (MCP) photon detectors at the periphery of the detector which time their arrival. In order to achieve effective π/K separation, a time-of-flight resolution of 15 ps per track is required at a distance of approximately 10 meters from the interaction region. This resolution imposes a requirement of 70 ps resolution per single photon.

In this paper, we will report the recent development of such a TOF measurement system based on existing ASICs and commercial MCPs.

2 Electronics development

2.1 Photon detectors

Currently, commercial MCPs that are close to our requirements are Planacon MCPs from Photonis, U.S.A. [3]. The 8×8 channel XP85012 model [4], which covers a 53×53 mm² active area, is used for prototyping at the current stage of development. This type of device is equipped with two MCPs in chevron configuration with a 25 μ m pore diameter and an overall gain of 10^6 . Figure 2 shows such an MCP installed on a mother board in a mechanical assembly together with TORCH customized electronics. The mother board has four high bandwidth connectors on the back side to allow interchange of readout boards in an assembly.

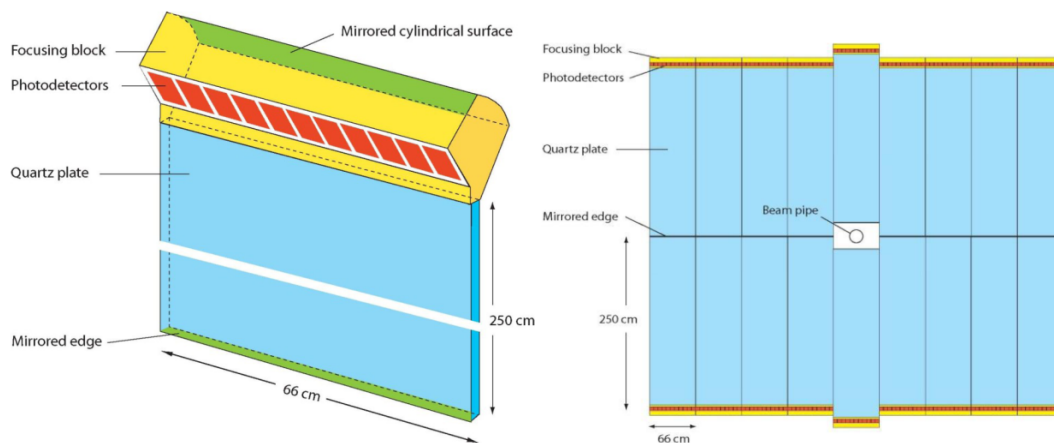


Figure 1. (Left) TORCH detector, (right) segmented quartz plate.



Figure 2. An MCP detector in a TORCH module.

2.1.1 Front-end electronics

Figure 3 shows the general data flow in the developed system. Firstly, the NINO chips amplify the signals from the MCP and measure the Time-Over-Threshold (TOT) according to a user-defined threshold [5]. Its output is a digital pulse whose width depends on the input charge. In order to suit the input requirement of the HPTDCs, the outputs of the NINOs are converted to LVDS signals through external discrete components. The HPTDCs were used in Very High Resolution Mode to offer a maximum 25 ps resolution [6]. In this mode, the HPTDCs perform high resolution interpolation from the individual measurements of four normal channels that are connected by an R-C delay line, therefore a 32-channel HPTDC can only provide 8 channels in this case. The HPTDCs measure the arrival time of the rising and trailing edge of the pulse from the corresponding NINO, which provides the TOT information from the MCP. The HPTDC's data are buffered in the on-board FPGA and subsequently transmit to the readout board to be sent to a DAQ PC. A test input LEMO connector is also included on the FE board. The incoming test pulse is fanned out to all channels of either NINO via a selection jumper and zero-ohm links. A fully assembled FE board is shown in figure 4.

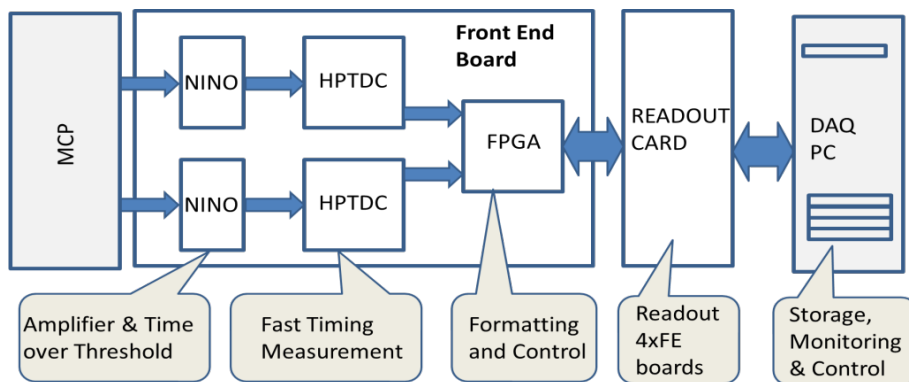


Figure 3. Data flow of the developed system.

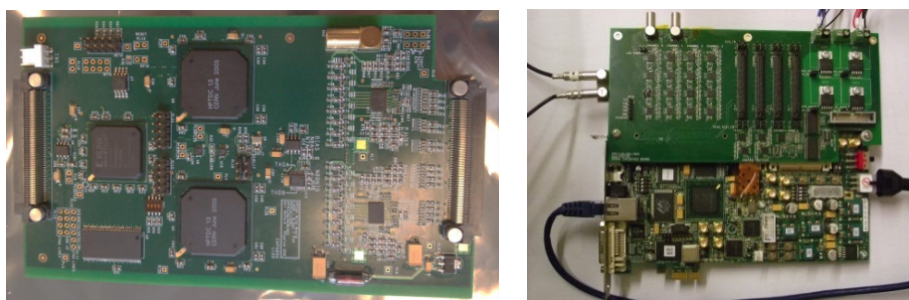


Figure 4. FE board (left) and Readout Board (right).

The firmware of the FPGA provides the following functions: command decoding (control and configuration), HPTDC control, HPTDC data buffering, data formatting and NINO threshold control. The control commands are decoded on the Front-End (FE) boards; according to the command the FPGA will generate control signals for the ASICs, for instance, HPTDC reset, HPTDC measurement start, etc. Once the HPTDC operation is started, data are read by the FPGA and temporarily buffered locally. In some cases, the data are formatted or modified to be compatible with other components in the experiment, for example to work with a telescope in a test beam. The threshold of NINO chips can also be set via the control interface. As well as the control commands, the threshold value and channel number are decoded from the incoming configuration commands. The corresponding channel on a DAC, that provides a threshold bias value, is adjusted via an SPI interface. The threshold and stretcher settings of the NINOs can be independently adjusted.

The assembly of the QFN-packaged NINO is a challenging task. Dedicated jigs have been designed for positioning the NINO ASICs on a PCB as shown in figure 5. Extra holes have been added to the footprint of the large pad in the middle to allow adequate heat going through the PCB during the re-flowing process. We also have experimented with temperature profiles in order to correctly re-flow the NINOs. Finally, the connectivity of NINOs is tested before fully populating a PCB.

2.1.2 Readout and control system

The readout and control system has been implemented on a Xilinx SP605 development board [7] along with a customized PCB to provide a physical interface to the FE boards, as shown in figure 4. The interface board connects to the SP605 via a FMC-LPC connector. LVDS buffer chips are used

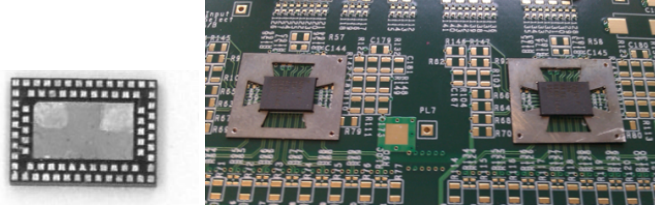


Figure 5. NINO package and assembling of NINO ASICs.

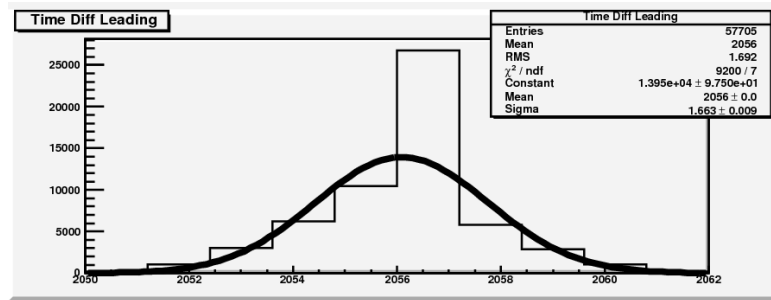


Figure 6. Intrinsic time resolution, the x axis unit in 25 ps.

to protect FPGA I/Os on both SP605 and the FE boards. The interface board also provides the supply of power to the FE board using two on-board regulators. Such a combination allows the operation of up to four FE boards and to control the electronics from a DAQ PC using Giga-bit Ethernet. Control commands and configuration can also be sent to the readout board via the Ethernet, and then transferred to the FEs via serial links. The control commands are four-byte words that can be generated on any platform (Windows, Linux, Android, etc.) with the support of Ethernet and MAC protocol. The commands can be easily modified or extended in readout firmware. Labview-based DAQ software has also been developed to provide data transmission, control and configuration functions.

3 Timing resolution studies

As a first step, the intrinsic timing resolution is measured with electrical test pulses. In this test, two consecutive pulses are injected via the test input, then the difference of the two leading edges are measured on the same channel. The result is shown in figure 6. The standard deviation of the fit gives a timing resolution of $1.66 \times 25 = 41.5$ ps.

The electronics are also used to test the performance of the Planacon MCP photon detector. The performance is investigated with a 20 ps pulsed blue laser at a modest MCP gain. The reference time is provided by a single-channel MCP photon detector coupled to a Constant Fraction Discriminator. A 90 ps overall time resolution has been obtained with the developed electronics. The details of this testing work can be found in [8].

A beam test has been carried out at CERN using the MCP described earlier in a low-intensity muon beam. Two $8 \text{ mm} \times 8 \text{ mm}$ borosilicate bars were coupled to the MCP to produce Cherenkov photons from the incident particles. Time differences were measured against a reference signal provided by a same borosilicate bar coupled to a single-channel MCP, read out with commercial electronics. A preliminary analysis shows the overall timing resolution is of order 130 ps.

4 Conclusion and future work

This paper reports the development and timing resolution results of a precision TOF system for the TORCH detector. The hardware and firmware designs are introduced as well as the challenges in production. The initial tests show that the system has an intrinsic time resolution of ~ 40 ps with electrical pulse injection. Testing work with a pulsed laser shows an overall 90 ps timing resolution using a commercial Planacon MCP.

Possible improvements have been identified. Firstly, implementing Integral Nonlinearity (INL) corrections on the HPTDC chips are known to provide better timing resolution [5]. Secondly, a time walk effect can degrade the timing performance due to an amplitude fluctuation of a signal. This effect has yet to be corrected from the TOT information provided by the NINO. Combining the above two techniques is expected to improve the timing resolution.

Development of a 64-channel FE board using 32-channel NINO chips is also under way, aiming for a higher channel density for future MCPs.

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