EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH

CERN-EP/88-115
September 6th, 1988

Silicon Detector Tests with the RAL Microplex Readout Chip

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Abstract

The design, construction and operation of a 5 layer silicon microstrip detector is described. The detector consisted of silicon microstrip wafers bonded to the RAL Microplex MX2 readout chip. The readout chip provided amplification with double-correlated sampling for each microstrip channel and multiplexing of 128 signals. The circuitry controlling the chip, the readout electronics, the stage holding the microstrip wafers and their alignment, are also described. A single-strip resolution of $10 \pm 0.6\mu m$ was obtained in a test beam. This work is part of a program to design a microvertex detector for the UA1 experiment at the CERN ppbar collider.

Presented at the International Conference on Advanced Technology and Particle Physics, Centro di Cultura Scientifica A. Volta, Villa Olmo, Como, Italy, 13-17 June 1988

[Proceedings published by Nucl. Instr. & Methods]

1. Introduction

Silicon microstrip detectors have been successfully used in fixed target experiments for the direct observation of charm particle decay vertices. Silicon vertex detectors are also planned for heavy quark studies in $p\bar{p}$ and e^+e^- collider experiments. In a collider environment the use of silicon microstrip detectors near the interaction region requires multiplexed readout and low-power electronics due to the very high channel density and limited space. For this reason considerable effort has been devoted to the development of monolithic VLSI front-end chips to be directly bonded to the silicon microstrip wafers [1]. The UA1 collaboration is studying the feasibility of a silicon microstrip vertex detector. We describe here the construction and operation of a five-layer silicon microstrip telescope which is read out by the RAL Microplex readout chip. The performance of the readout chip and the single-hit position resolution obtained are described.

2.1 The Detector System

A schematic of the test beam setup is shown in figure 1. A telescope constructed from five silicon detector elements was aligned in a support box perpendicular to the beam. A detector element, shown in figure 2, consists of a silicon microstrip detector wafer and a Microplex readout chip mounted on a printed circuit board (PCB). A trigger was constructed from four scintillators forming a 1 cm^2 aperture over a length of 50cm. A NIM crate containing the driver box for the control of the readout chip was adjacent to the telescope. The remainder of the equipment was outside of the beam area and consisted of a Macintosh computer with a MacVEE interface [2] and a CAMAC crate which contained the SIROCCO [3] digitizing unit and the trigger logic control modules.

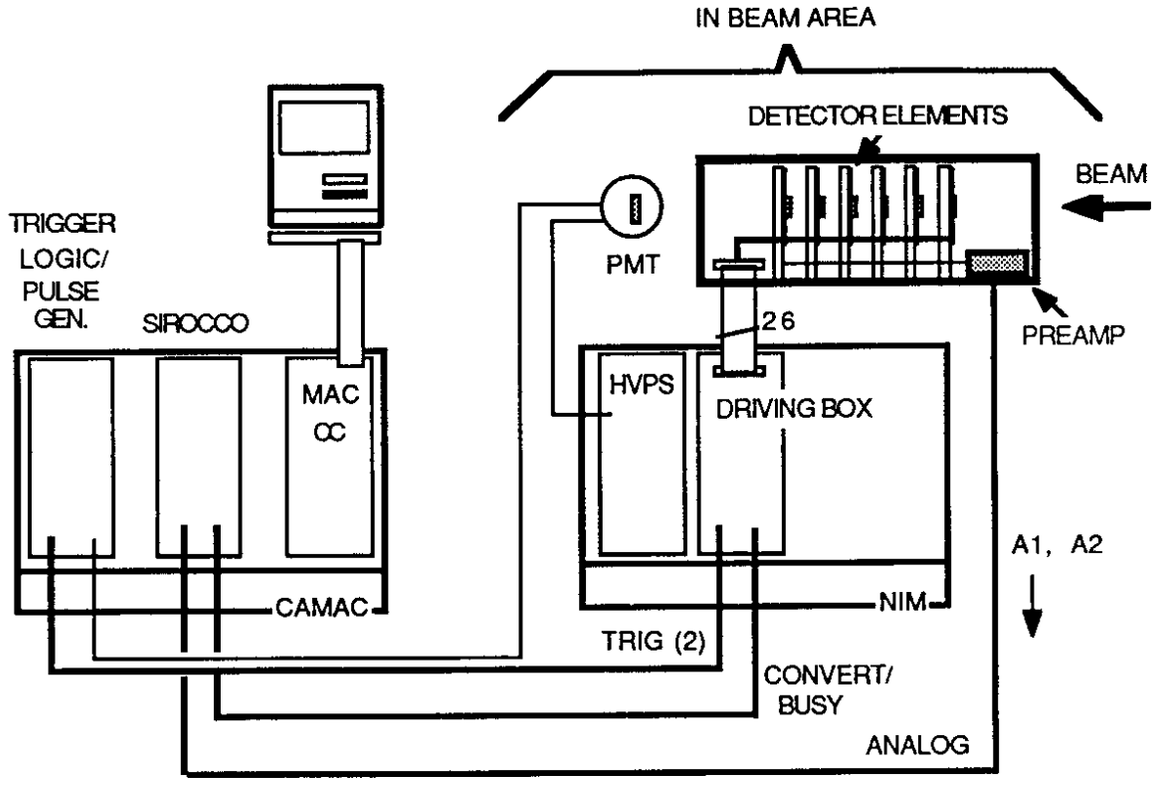


Figure 1. Test Beam Setup.

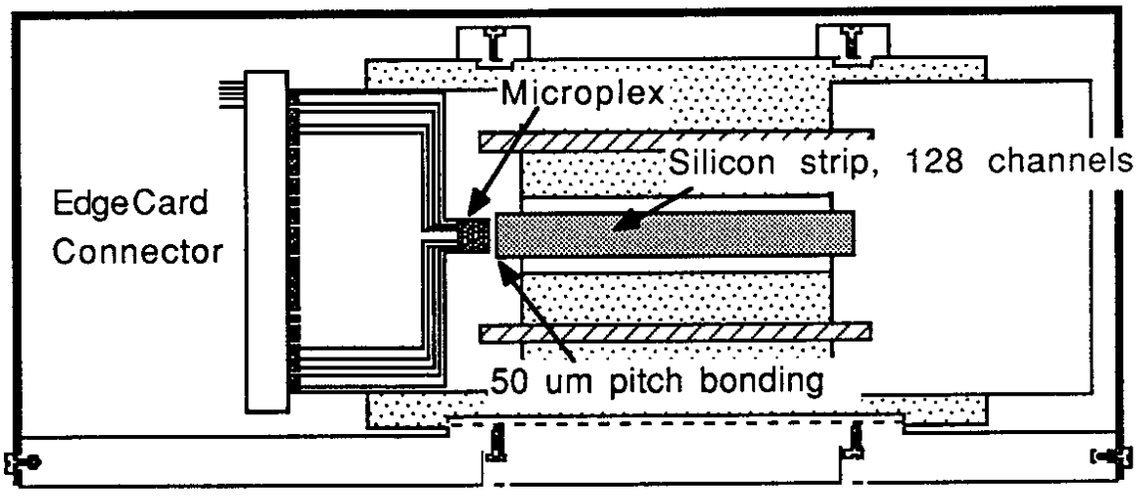


Figure 2. Detector Element in Support/Shielding Box.

2.2 Silicon Microstrip Detector Wafers

The 300mm thick detector wafers were made from high resistivity n-type silicon, and were 26mm by 75mm, each with 512 strips at a pitch of 50μm, running parallel in the long dimension. All but one of the wafers used for the tests were lengthwise-cut 1/3 sections of wafers originally designed for the CDF experiment at Fermilab and manufactured by MICRON

Semiconductor, Ltd. The cutting produced detector pieces of about 170 strips wide and was done for reasons of economy. A silicon microstrip detector consists of an array of parallel p^+n diode strips, each strip acting as one detector channel, and the cathode is a common backplane. This detector was operated with +36 volts on the backplane. Since the input of the Microplex amplifiers holds a strip at +4 volts, the diode is back-biased by 32 volts, near the 45 volts for full depletion.

One of the limiting factors in the performance of the amplifiers is the level of leakage current generated in the silicon detector while back-biased at the depletion voltage. If the current is more than a few hundreds of nanoamps, the signal to noise ratio can become low enough to render the channel unusable. At the same time, its integrating amplifier can become saturated and, therefore, unusable.

Measurements for individual channels of both leakage current and capacitance as a function of depletion voltage in individual channels were made at Rutherford-Appleton Laboratory [4]. These measurements were performed using a programmable integrated circuit testing station equipped with a probe that contacts 32 adjacent readout pads at once. This insures that enough strips are held at a potential so that the field inside the silicon approximates that of a detector bonded to an amplifier (single strip testing is insufficient). The capacitance versus bias voltage test showed that the detector reaches minimum capacitance and is therefore fully depleted at 45 to 50 volts. Leakage currents were on the order of ten nanoamps in most channels; however, some channels were worse and conducted currents on the order of a microamp at bias voltages less than required for full depletion.

This higher level may have occurred in a few of the strips used in the detector, but during the beam tests the total current through 640 strips (5 detectors x 128 strips/detector) varied from 6 to 7μA. Our use of a second-quality grade silicon detectors produced larger leakage currents (by

approximately a factor of 5) when compared to the highest grade silicon detectors, and this may have contributed slightly to a worsening of the single-hit resolution.

At both ends of each strip were bonding pads for connecting to the Microplex readout chip. The bonding pads were arranged in two rows, or tiers (running perpendicular to the strips), in order to accomplish this high bonding density. This necessarily must be the same arrangement for the bonding pads on the readout chip.

2.3 The Microplex Readout Chip

The RAL MX2 Microplex chip is a VLSI integrated circuit chip using CMOS technology with a 3μm feature size. It is a newer version of the Microplex chip developed several years ago using NMOS technology [1]. CMOS is used because of its low power consumption, enabling its use in a >10,000 channel microvertex detector for collider experiments. The RAL chip was designed for the DELPHI microvertex detector. Some design details and the operation of an earlier but operationally equivalent version of the chip, the MX1, (using 5μm feature-size technology) are described in [5], and some test results of the chip used here are described in [6].

The RAL chip is 6.0 x 6.4 mm^2 and has 128 input bonding pads on one end, and 25 bonding pads on the other end for control lines, ground and power supplies. The input pads on the readout chip are arranged in two tiers, as mentioned above, and spaced at a pitch (46μm) slightly smaller than the pitch of the microstrips on the detector (50μm).

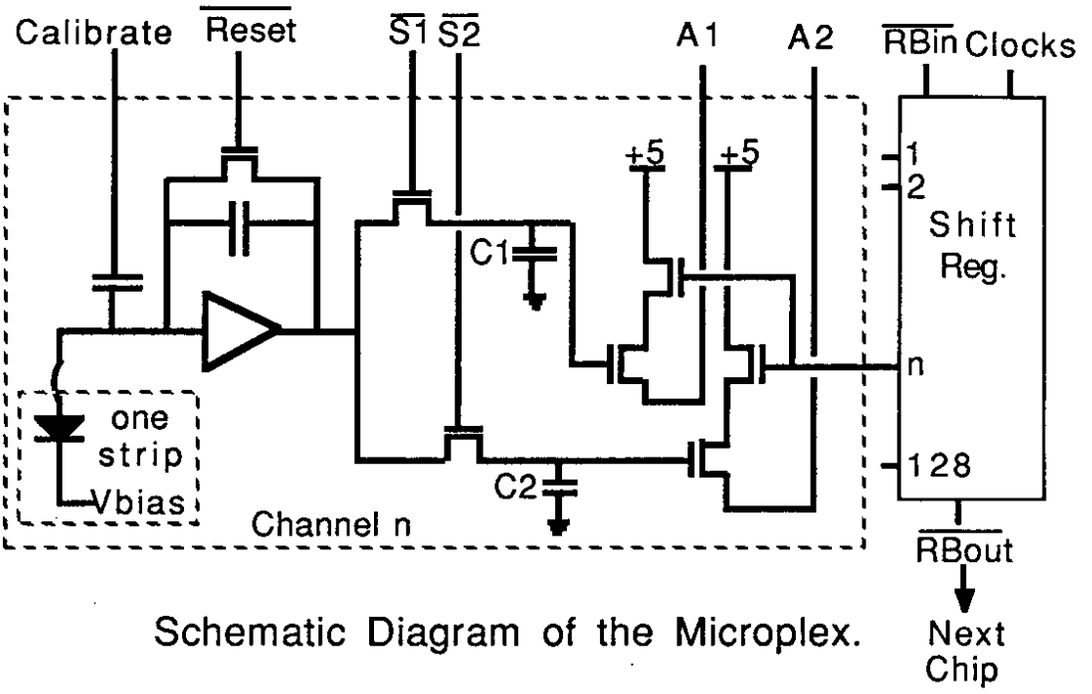
The readout chip provides a double-correlated sample of the charge collected on each of the 128 strips. The output of a current integrating amplifier is recorded on two storage capacitors, one holds the value seen just before a possible signal arrives, the other just after. During readout, signals from these capacitors are treated as a differential pair and subtracted, thus

cancelling out noise characterized by a frequency lower than one over the sampling period. In particular, it reduced the effects of leakage currents (a white noise source).

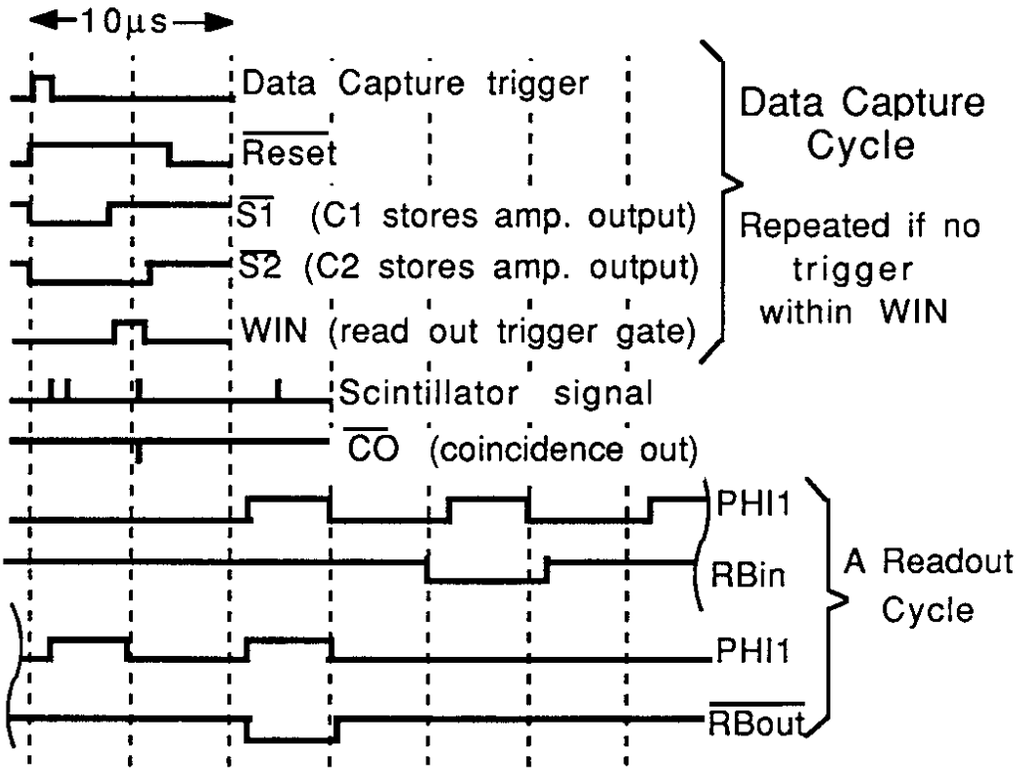
A simplified circuit diagram of one channel and a basic timing diagram appears in figure 3. A *data capture trigger* into the driving box (described below) generated a *data capture cycle*. The $\overline{R}$ control line low zeroes the output of the amplifier, and the $\overline{S1}$ and $\overline{S2}$ signals low places the output of the amplifier on C1 and C2 respectively. After 4μs, C1 was disconnected by the rise of $\overline{S1}$ and retained the voltage value it had at that time. C2 was allowed to follow the output value for an additional 2μs, and was then disconnected. In order to test the operation of the chip at the SPS bunch crossing rate the entire *data capture cycle* has been run as short as 3.8μs.Multiplexing was performed by a 128-stage shift register integrated onto the chip. The two analog levels stored on C1 and C2 were connected to the gates of high input-impedance FETs, whose power supplies were switched on in sequence as the shift register moved the "read bit" through each amplifier stage (this is discussed in more detail in section 2.7). The two signals were converted from current to voltage at the preamp stage and then subtracted at the analog stage inside the SIROCCO digitizing module

2.4 **Mounting and Bonding**

After the Microplex chips had been tested for functionality at the wafer level at RAL, MICRON mounted the chips onto a 6cm by 6cm printed circuit board (PCB) and bonded the 25 control lines. The PCB provided fan-out to a standard edge card connector. The Microplex/PCB unit was then tested at Imperial College using the readout system described below. Using tested Microplex/PCB's, MICRON then assembled the basic parts of the detector elements shown in figure 2, and performed the high density bonding. Further assembly was performed at CERN.



Schematic Diagram of the Microplex.



Data Capture and Read Out Timing Diagram

Figure 3. Schematic and Timing Diagram.

2.5 The Detector Element

A diagram of a detector element is shown in figure 2. The silicon microstrip wafer was mounted as a bridge between two pieces of printed circuit board. Two additional strips of fiber glass were glued either side of the silicon for stress relief. The entire assembly was then glued onto a copper clad PCB which provided the necessary mechanical strength for alignment. The gluing constituted a pre-alignment as the edge of the silicon strip was made parallel to the edge of the board. In order to reduce the material seen by a single particle traversing several silicon microstrip wafers, a window was machined in this board at the location of the wafer. During these tests an additional 1mm of PCB material was in place over each detector as a protective cover.

2.6 The Support Box

A side view of the interior of the support box is shown in figure 4.

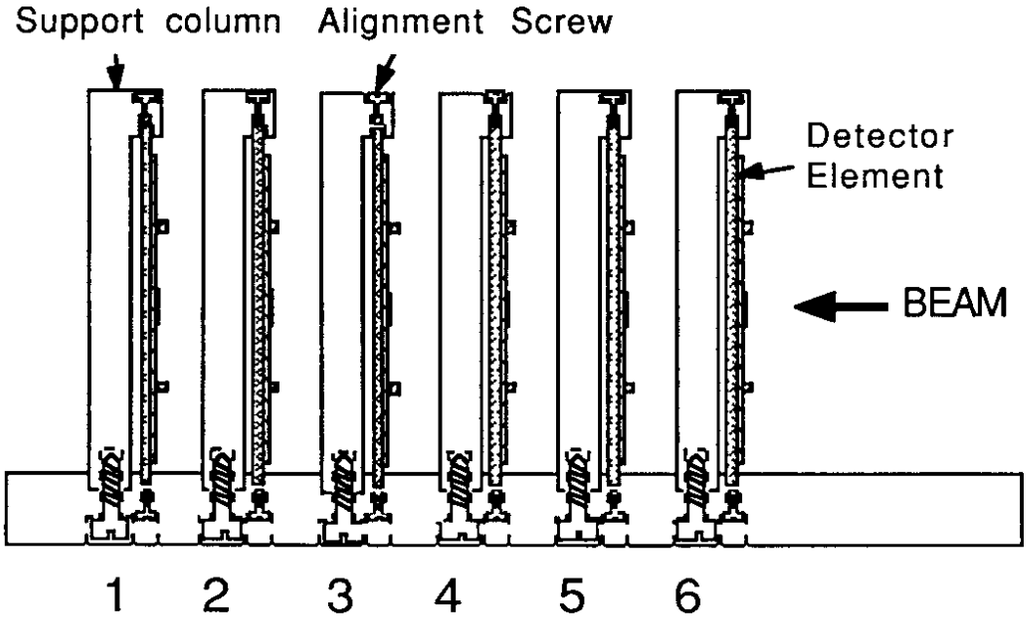


Figure 4. Mounted Detector Elements.

The five detector elements were spaced in 25 mm intervals, and the sixth element shown was a Microplex/PCB only. Grooves were milled across the face of this plate at 25 mm intervals to position the lower edges of the printed circuit boards of the detector elements. A pair of support columns with notched heads were mounted near each groove to hold the upper edges of the detector elements in place. Holes were threaded through the column heads into the notches and through the support base into the grooves. Screws were mounted in these opposing holes to align and maintain the alignment of the detector elements.

The detectors were aligned such that the first strips of each detector lay in a plane parallel to the beam axis. It was possible to measure systematic offsets using reconstructed tracks as long as the first strips of each detector were all parallel (even if they did not all lie in the same horizontal plane). The precision to which the strips could be made parallel from end to end was estimated to be $\pm 10\mu m$, equivalent to ± 0.13mrad for 75mm long strips This reduced possible skewness problems (i.e. a systematic offset of a detector's vertical position as a function of track position *along* the strip).

2.7 **The Driving Box**

The driving box is a double-width NIM module containing the power supply and control circuitry for the Microplex chip. It was designed at RAL and Imperial College, and built at the electronics shop at RAL. This module generated the *data capture cycle* signals in response to a signal from a pulse generator (see figure 3). If a scintillator signal was received during the window (WIN), it generated the *readout cycle* signals. Data were read out from the chip when a "read bit" ($\overline{\text{RBin}}$) was generated in coincidence with the second PHI1 clock pulse as indicated in the timing diagram. Data appeared on the two outputs (A1 and A2 in figure 3) at one channel per clock cycle while a CONVERT signal (equivalent to PHI1, but starting with the

read-bit) synchronized the digitizations. When the shift register in the chip had passed the read bit through all the channels, a $\overline{\text{RBout}}$ (read-bit out bar) signal was sent to the next readout chip's $\overline{\text{RBin}}$ control line in a daisy chain. All other control signals were wired in parallel. The $\overline{\text{RBout}}$ from the last chip shuts off the CONVERT signal. After a *readout cycle* is started, further *data capture cycles* are blocked until all channels have been read out.

2.8 SIROCCO Digitizing Module

The SIROCCO is a CAMAC module [3] specially designed to digitize and record the difference between the two analog signals. This module was made by the EP division at CERN for the DELPHI microvertex detector. It is designed to digitize and store data from up to 2048 detector channels. The SIROCCO also subtracts a pre-programmed pedestal value (one for each channel) and makes a subsequent comparison of the result with a programmed threshold (one per module). As the data were clocked out from the readout chip, the module stores only those data above the threshold along with their corresponding channel number. Even though the SIROCCO had this "zero-skipping" capability, it was decided to read out all channels in order to study the performance of the RAL Microplex chip. The zero skipping feature was intended to reduce the module-to-computer readout time.

3.1 Data Acquisition

Figure 5 shows a scope trace of the analog signal during the *readout cycle* from six Microplex chips (five complete detector elements and an additional bare Microplex chip). The photograph shows 6 x 128 = 768 distinct analog levels in sequence coming from the six chips, being clocked out at 8μs per channel (1 V/div. horizontally). The portion of the signal coming from each chip is shown, and an arrow indicates the transition from one to the next. The RMS noise on a Microplex chip produced about 7 ADC counts; on a

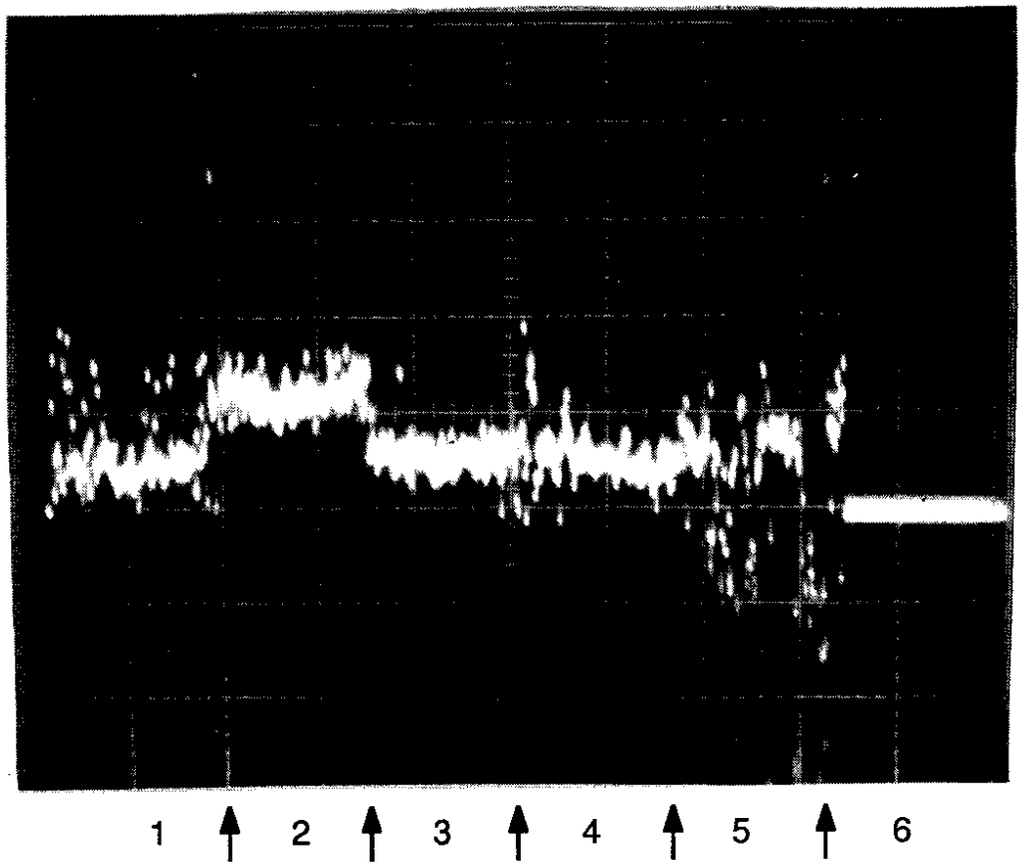


Figure 5. Signal into the ADC.

bonded detector it was about 14 counts; while the signal due to a charged particle through the silicon was about 128 counts, giving a signal-to-noise ratio of 9:1.

The span of voltage in the photograph was approximately 3.5V, corresponding to 2000 ADC units. These are the pedestal levels that would normally be loaded into the SIROCCO memory and subtracted channel by channel from the corresponding signal during subsequent readout cycles. For these tests, however, the pedestal determination and their subtraction was done inside the data acquisition computer.

Several features of interest are visible in the photo. The second detector had higher average leakage currents compared to the other detectors, but was otherwise well behaved. At several places there were levels far from the local average and these were thought to be defective or unbonded strips or amplifier channels. At the beginning of #1 and #4, many levels were

abnormally high. This problem was not investigated but it may be due to imperfections in the silicon aggravated by the 20 unbonded strips immediately beyond the strips bonded to amplifiers. The unbonded strips were not held at 4 volts by the input of an amplifier, and this may have resulted in more leakage current into nearby active channels. Detector #5 showed a large spread in its signal levels which resulted in about 40 channels being unusable. This problem was later mostly corrected by lowering the gain of the FETs in the Microplex, which is done by adjustment of the potential of the preamplifier's input. Updating of the pedestals was done every half hour to correct for their drift.

3.2 **Data Analysis**

The silicon detectors were exposed to the CERN PS test beam composed of positive particles (mostly pions) with momentum 3 GeV/c. Data from 450 triggers were recorded and analyzed. Figure 6 shows the ADC values recorded for a single event after pedestal subtraction. The shaded areas highlight the bins (i.e. the hits) where the ADC values exceed 4σ above zero, and were used for a track. The hits were graphically displayed for each trigger and then scanned for tracks. From this sample, 105 candidate tracks containing at least one hit in each of the 5 detectors were found. The coordinate of each hit was calculated using the centroid of the channels in a cluster. A cluster is one or more adjacent channels with a signal above 4σ, and their nearest neighbors (if the neighbor's signal was >0). A large number of dead channels (40 out of 128) in the fifth detector greatly reduced the efficiency for finding 5-hit tracks. This together with the geometrical factors accounts for the efficiency for 5-hit tracks. The intrinsic efficiency of the detectors was not determined.

Straight line fits were used to measure the (parallel) vertical offsets between detectors, and they varied from 5 to 100μm. The microstrips were

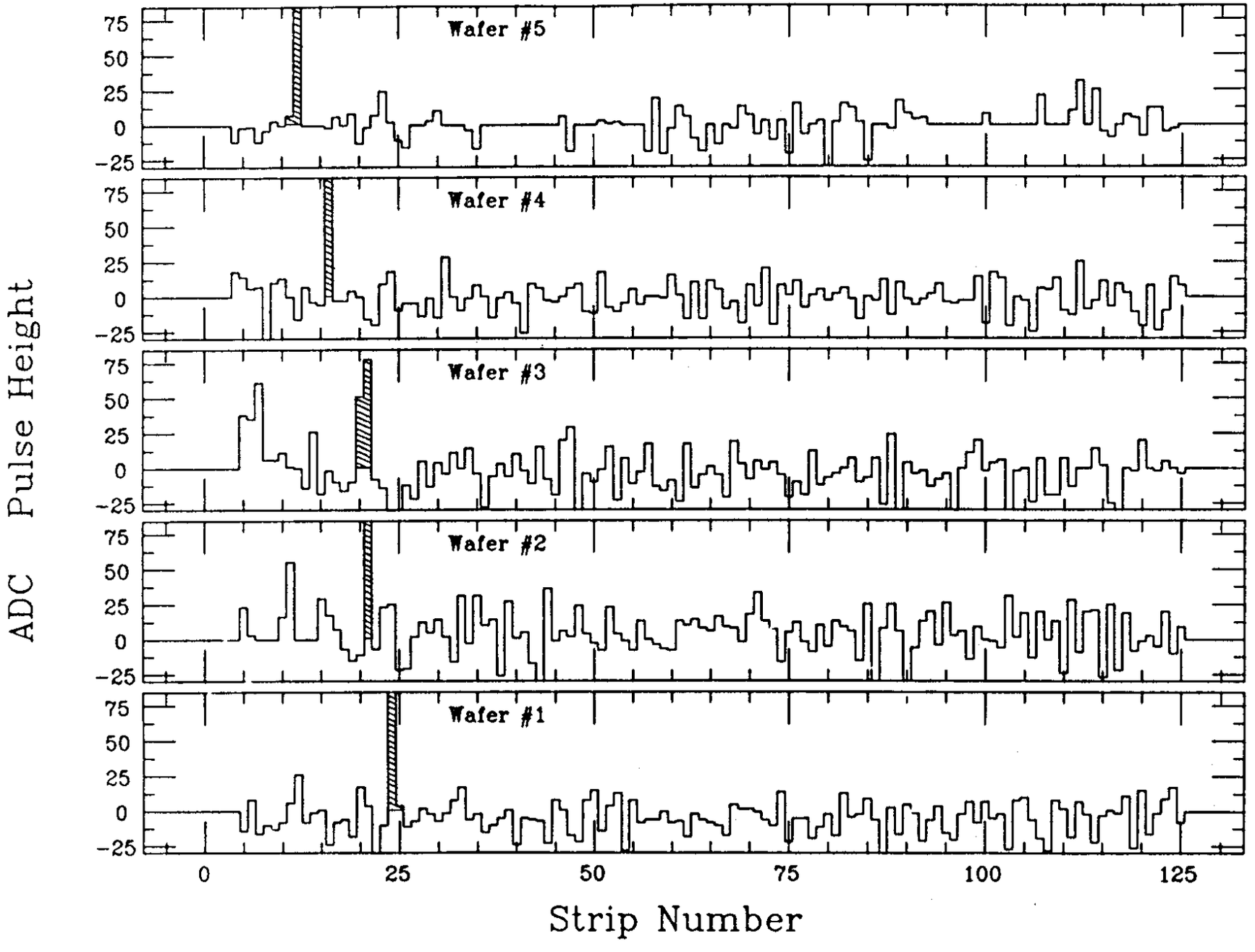


Figure 6. ADC Values for One Event.

estimated to be parallel within ±0.13mrad (see section 2.6). Over the 1cm of sensitive length of strip, non-parallelism contributes ±1.3μm to the position resolution error, which is negligible when it is added in quadrature.

Figure 7 shows the residuals calculated for the 105 tracks after alignment corrections for the five elements. A gaussian fits this curve well and gives a standard deviation of 9.3 ± 0.3μm. The corresponding single-hit resolution is 11.8 ± 0.3μm. This includes a contribution from multiple scattering. The resolution expected for high momentum tracks is 10 ± 0.6μm when Coulomb scattering is unfolded with a Monte Carlo program .

This may be compared to the single-hit resolution expected from a Monte Carlo which generated data in the following way:

1) Generate hit positions of normally incident particles over the range of positions between two strips.

2) For each particle, calculate the expected charge sharing between strips (using the estimated electric field inside the silicon to include the non-linear sharing of charge over inter-strip position), and generate signal heights for two adjacent strips.

3) Smear the signal heights using the signal to noise ratio over a range of ratios.

4) Calculate the resulting position of the centroid of charge.

The signal-to-noise ratio observed was 9:1, and this Monte Carlo implies an expected single-hit resolution of 10.5μm. This is consistent with our above measurement.

4. Conclusion

Compact readout electronics is an essential requirement for the collider operation of silicon microvertex detectors. We have investigated the performance of the RAL Microplex readout chip and have operated it with a

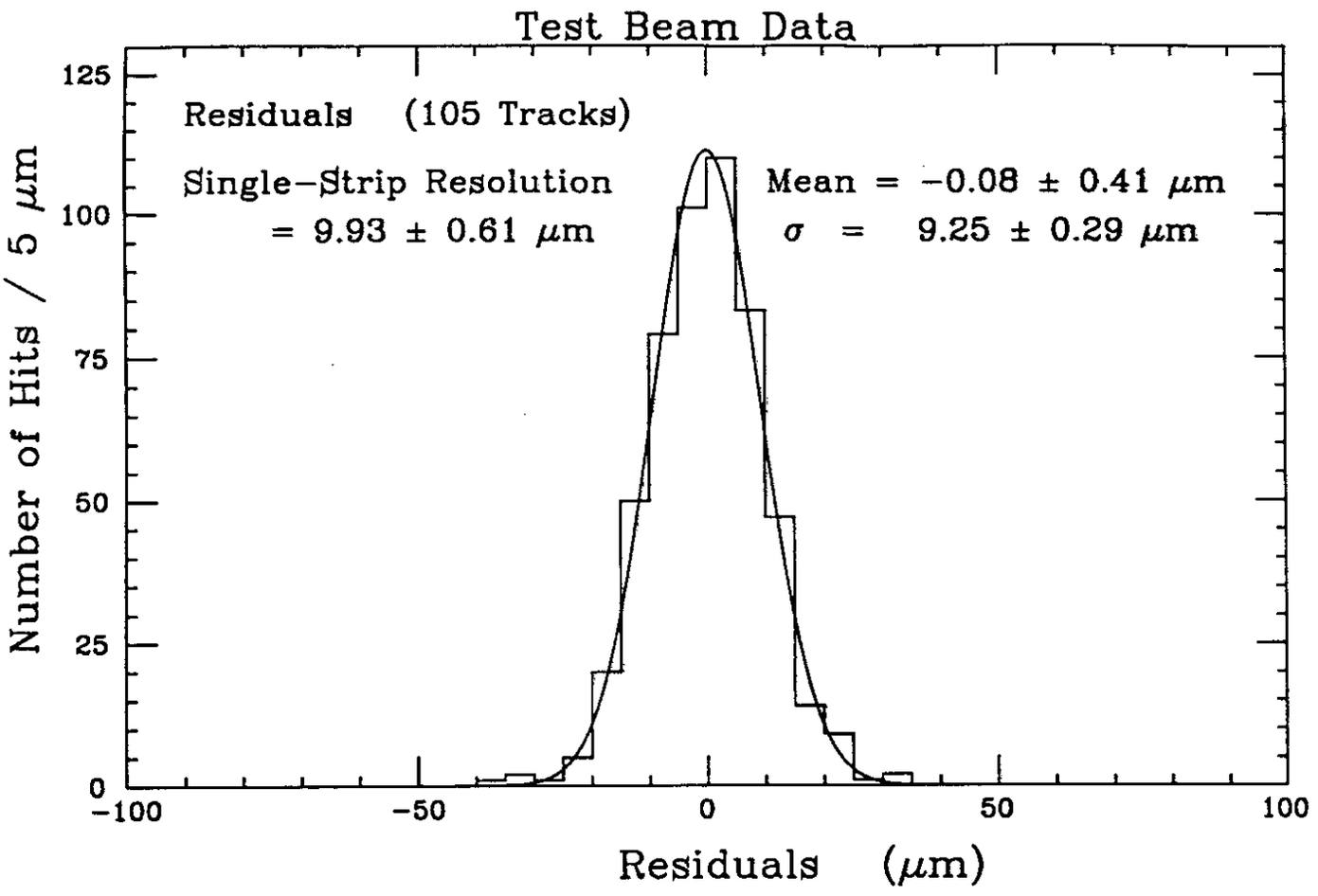


Figure 7.

3.8μs data capture cycle time. Using a five-layer silicon strip detector in a test beam, the single-hit resolution for high momentum tracks was $10 \pm 0.6\mu m$.

Acknowledgements:

We would like to thank P. Weilhammer, R. Horisberger, L. Hubbeling, and B. Boulter of CERN as well as L. Nardini and M. Price of RAL for useful discussions and technical assistance. Thanks are also due to the staff of the CERN SPS test beam facility. This work was supported in part by the U. S. Department of Energy.

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