The ATLAS Level-1 Muon Topological Trigger Information for Run 2 of the LHC

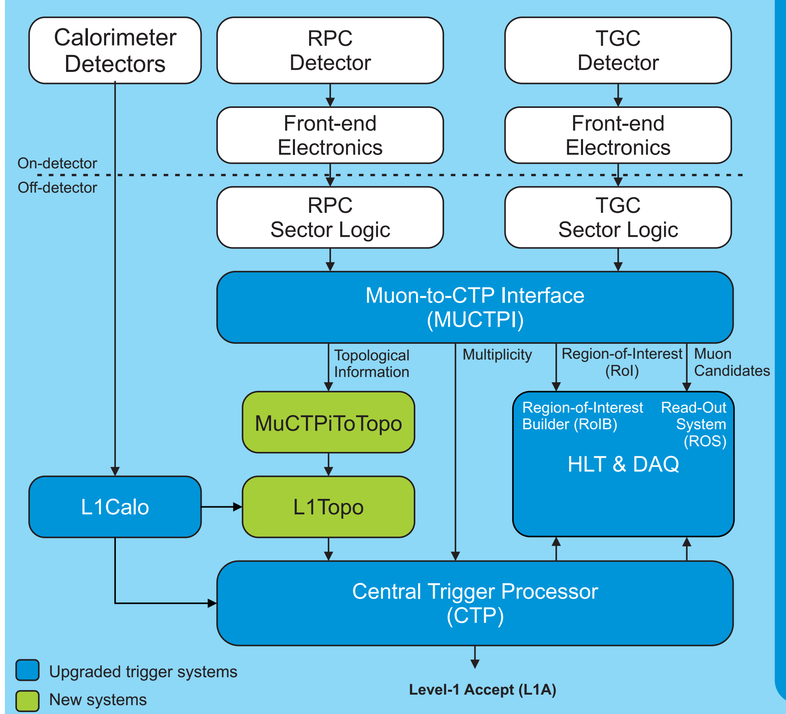
S. Artz [a], B. Bauss [a], H. Boterenbrood [b], V. Buescher [a], R. Degele [a], S. Dhaliwal [b], N. Ellis [c], P. Farthouat [c], G. Galster [c,d], M. Ghibaudi [c,e], J. Glatzer [c], S. Haas [c], O. Igonkina [b], K. Jakobi [a], P. Jansweijer [b], C. Kahra [a], A. Kaluza [a], M. Kaneda [c], A. Marzin [c], C. Ohm [c], M. Silva Oliveira [c,f], T. Pauly [c], R. Pottgen [c], A. Reiss [a], U. Schaefer [a], J. Schaeffer [a], J.D. Schipper [b], K. Schmieden [c], F. Schreuder [b], E. Simioni [a], M. Simon [a], R. Spiwoks [c], J. Stelzer [c], S. Tapprogge [a], J. Vermeulen [b], A. Vogel [a], M. Zinser [a]

[a] Johannes-Gutenberg-Universitaet Mainz (DE), [b] Nikhef (NL), [c] CERN, [d] University of Copenhagen (DK), [e] Scuola Superiore Sant'Anna di Studi Universitari e di Perfezionamento (IT), [f] Juiz de Fora Federal University (BR)

1) Overview

For the next run of the LHC, the **ATLAS** Level-1 trigger system will include **topological information** on trigger objects from calorimeters and muon detectors in order to cope with the increased luminosity. The MUCTPI (Muon-to-Central-Trigger-Processor Interface) system has been upgraded to send muon topological information. In order to extract, encode and send topological information through the existing MUCTPI electrical trigger outputs, the MIOCT (Muon Octant) module firmware has been modified. The topological information from the muon detectors will be sent to the Level-1 Topological Trigger Processor (L1Topo) through the MUCTPI-to-Level-1-Topological-Processor interface (MuCTPiToTopo). Examples of topological algorithms are: search for Lepton Flavour Violation, B_s-physics, Beyond the Standard Model (BSM) physics and others. This poster describes the modifications to the MUCTPI and its integration with the full trigger chain.

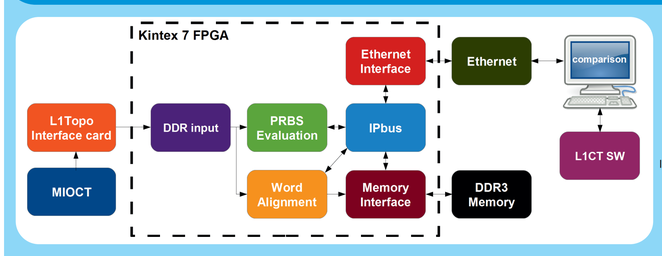
2) ATLAS Level-1 Muon Trigger Overview



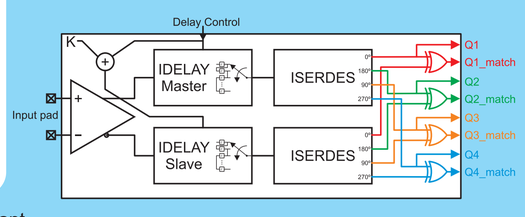
The MUCTPI is part of the ATLAS Level-1 Trigger system and connects the output data from the muon trigger system to the CTP (Central Trigger Processor), HLT (High-Level Trigger) and DAQ (Data Acquisition) system. At every bunch crossing, the MUCTPI receives information on muon candidates from 208 muon trigger sectors and calculates the total multiplicity for each of six momentum thresholds taking into account double counting of muon candidates in different sectors. In Run 2, the MUCTPI will also calculate coarse-grained topological information and send it to L1topo via the MuCTPiToTopo interface.
The CTP will make the final Level-1 trigger decision using the muon multiplicity, the output data from the L1Calo (Calorimeter trigger) and the results of topological algorithms run in the L1Topo.

3) Feasibility Tests in the MUCTPI

Full granularity muon trigger topological information will only be available when the MUCTPI system is completely replaced for Run 3. However, coarse-grained information is going to be available already in Run 2 using the electrical trigger outputs of the current MUCTPI system. The system has 16 MIOCT (octant modules) cards, which receive and process the muon candidate data from the muon trigger detectors. Since the MIOCT electrical trigger outputs were designed to operate at 40 MHz for testing purposes only, a test system was developed to check if reliable data transmission from the MUCTPI was feasible at 8X overclocking, the speed specified in the design.
Using this test system, a high resolution phase scan was performed on the transmitted data, showing a very low BER (Bit Error Rate). This test system was implemented using an **FPGA evaluation board** (Xilinx KC-705) and two FPGA Mezzanine Cards (FMC).

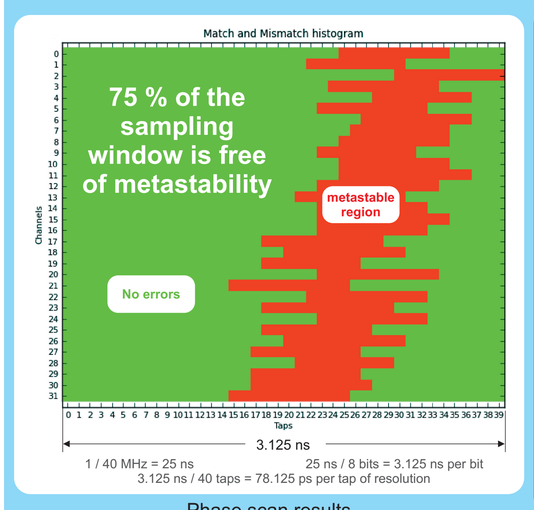


Test system block diagram: The 32 channels from the 16 MIOCT (octant modules) are connected to a custom FMC card, which converts the signals from NIM to LVDS. The input signal is sampled by the DDR input circuit and then checked by the PRBS (Pseudo Random Bit Sequence) Evaluation block. The results are read out through the Ethernet Interface and then processed in a PC. In addition, a data readout path is available in the system. An optimal sampling point is defined in the DDR input, the data are then deserialized and word-aligned. Subsequently the data are written in the DDR3 memory module from where they can be read out through the Ethernet Interface.



DDR input block: Two paths drive the signal with different programmable delay input lines. The data are latched with four different phases and the signal from the two paths are compared to look for transitions.

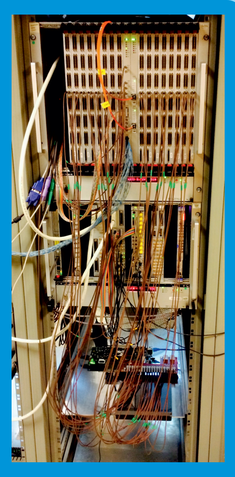
MIOCT module



Phase scan results

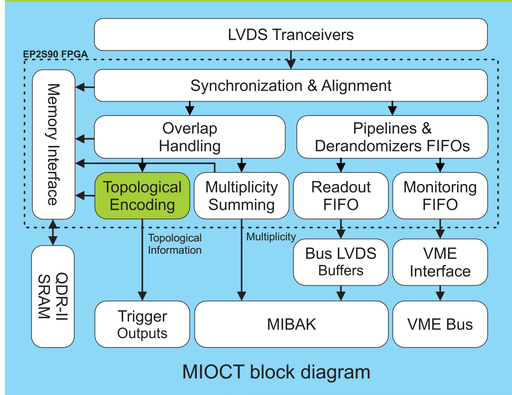
- Outputs overclocked by a factor of 8.
- The feasibility of the upgrade was demonstrated by connecting the 32 channels from the MUCTPI system to the test system.
- An optimal sampling point for each channel can be selected from the phase scan results.
- Test results show a large timing margin ensuring reliable operation.

Bit Error Rate < 10^{-15}
with a confidence level of 95 %



MUCTPI and the test system

4) Upgrade in the MUCTPI



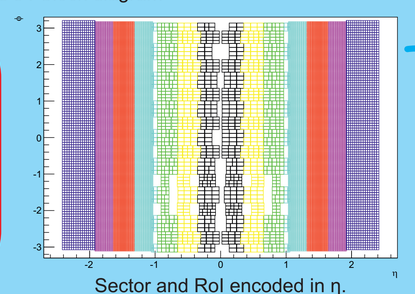
MIOCT block diagram

The 32 electrical trigger outputs (two per MIOCT) of the MUCTPI system will output 8 bits of muon topological information per LHC clock period. In order to provide topological information, the firmware upgrade consisted of extracting and encoding position information from the two candidates with highest transverse momentum and serializing it at 320 Mb/s using DDR outputs. The upgraded MUCTPI system sends muon topological trigger information at an aggregated rate of 10.24 Gb/s.

Bit position	7	6	5	4	3	2	1	0
Trigger output	η			ϕ			p_T	

The data format for the MIOCT trigger outputs was established based on a compromise between the available bandwidth and the best trigger efficiency from physics simulations.

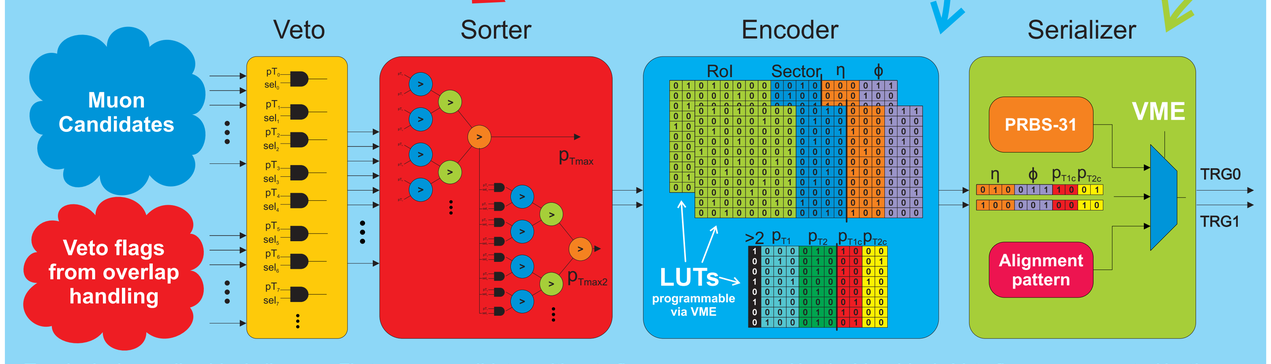
Two candidates from each of the 13 sectors are sorted and 2 candidates with the highest pT are selected for topological enconding



Sector and RoI encoded in η.
Each color corresponds to one code of η.

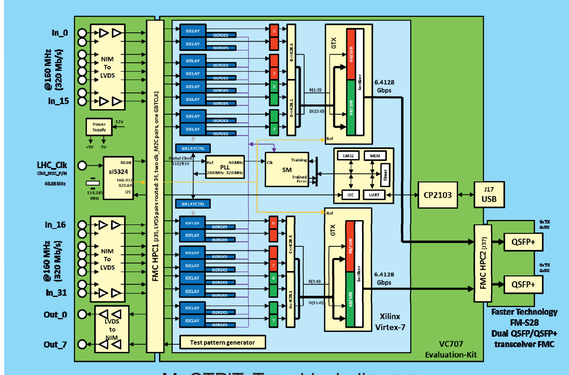
The position information of the two highest-momentum muon candidates is encoded in η and ϕ with bin size Δη x Δϕ ≈ 0.3 x 0.1

In addition to the serialization, a PRBS sequence can be used for phase alignment checking and a fixed pattern can be used for word alignment



Topological encoding block diagram: First, muon candidates with veto flags are suppressed by the Veto block. Veto flags are generated by the overlap handling algorithm to avoid double counting of muons in overlap regions of the detector. The candidates are sorted using parallel processing to minimize latency. The top two candidates are encoded using programmable LUTs. In the last stage the candidates are serialized at 320 Mb/s using DDR outputs. Verification on the target hardware connected to the test system was performed with data from ~ 1 x 10^{10} of bunches, **without errors.**

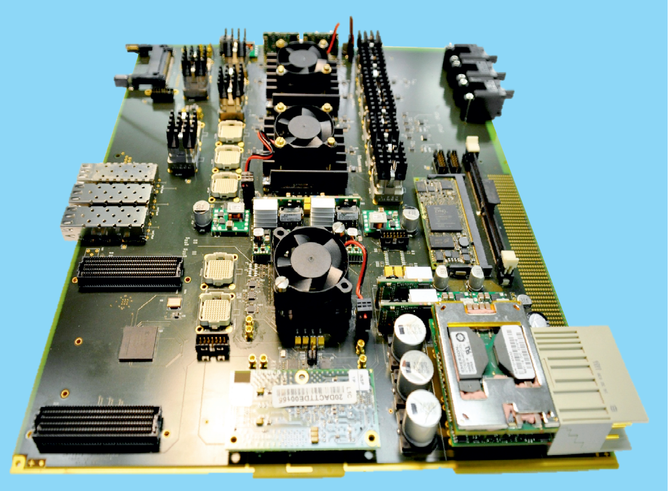
5) MuCTPiToTopo interface & L1Topo Processor



MuCTPiToTopo block diagram

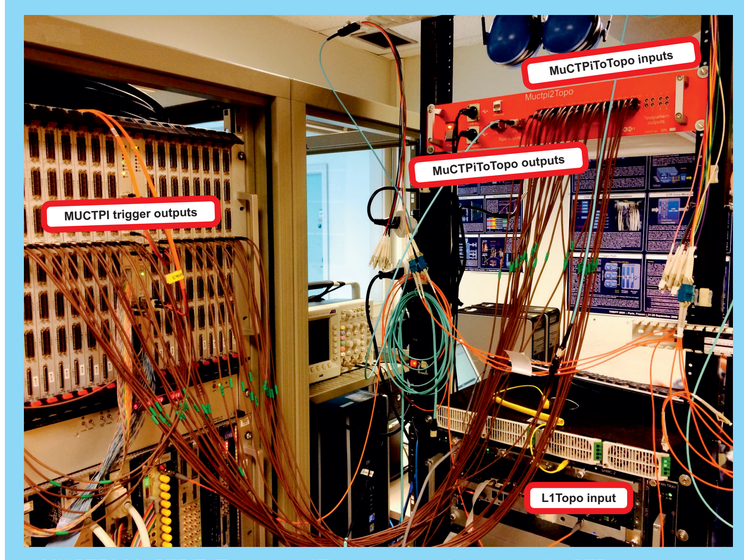
The MuCTPiToTopo interfaces the MUCTPI with the L1Topo processor. The primary components of the board consist of an FPGA development kit, the Xilinx VC707, and two FMC connectors. One connector receives data and the LHC clock from the MUCTPI, and the other transmits to the L1Topo via optical links. Data are aligned based on a training pattern from the MUCTPI, and 2 fold replicated by the MuCTPiToTopo. Further 2 fold replication is achieved by optical splitters to allow processing on each of the L1Topo's four FPGAs.

The L1Topo processor consists of:
- A single ATCA crate equipped with two processor modules.
- Each processor module mounts two large Virtex-7 FPGAs.
- Each FPGA receive an identical copy of L1Calo and L1Muon data and run a specific set of algorithms.
- Algorithms use lists of jets, electron/gamma, tau and muons to perform geometrical cuts, correlations and calculate complex cinematic observable.
- Design optimized for latency and high speed data transmission on the real time data path.
- About 200ns from receiving data and produce the algorithms response.
- Optical links tested up to 12.8 Gb/s.



L1Topo processor module

6) Integration Test Results



MUCTPI, MuCTPiToTopo and L1Topo in integration tests at the CTP laboratory

Integration tests with MuCTPiToTopo and L1Topo were performed and **successful data transmission was established**. During an overnight test, data from 2.6 x 10^6 bunches were sent from the MUCTPI to the MuCTPiToTopo interface. After that, the L1Topo was also included in the chain and the data from the MUCTPI were forwarded to the L1Topo processor by MuCTPiToTopo interface. During the second test, data from 2.6 x 10^3 bunches were checked at L1Topo. **No errors were found in any of the tests.**
Integration tests in the experiment will take place in the autumn of 2014 as part of the commissioning for Run 2.

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