Firmware development and testing of the ATLAS Pixel Detector / IBL ROD card

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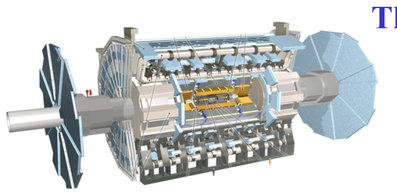
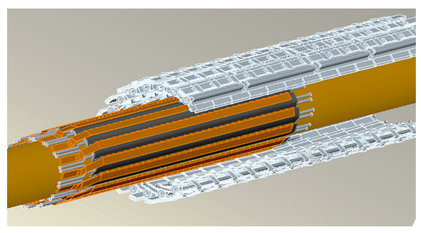
Abstract

The ATLAS Experiment is reworking and upgrading systems during the current LHC shut down. In particular, the Pixel detector has inserted an additional inner layer called Insertable B-Layer (IBL). The Readout-Driver card (ROD), the Back-of-Crate card (BOC), and the S-Link together form the essential frontend data path of the IBL's off-detector DAQ system. The strategy for IBLROD firmware development was three-fold: keeping as much of the PixelROD datapath firmware logic as possible, employing a complete new scheme of steering and calibration firmware and designing the overall system to prepare for a future unified code version integrating IBL and Pixel layers. Essential features such as data formatting, frontend-specific error handling, and calibration are added to the ROD data path. An IBLDAQ testbench using realistic frontend chip model was created to serve as an initial framework for full offline electronic system simulation. In this document, major firmware achievements concerning the IBLROD data path implementation, tested in testbench and on ROD prototypes, will be reported. Recent Pixel collaboration efforts focus on finalizing hardware and firmware tests for IBL. Time plan is to approach a final IBL DAQ phase by the end of 2014.

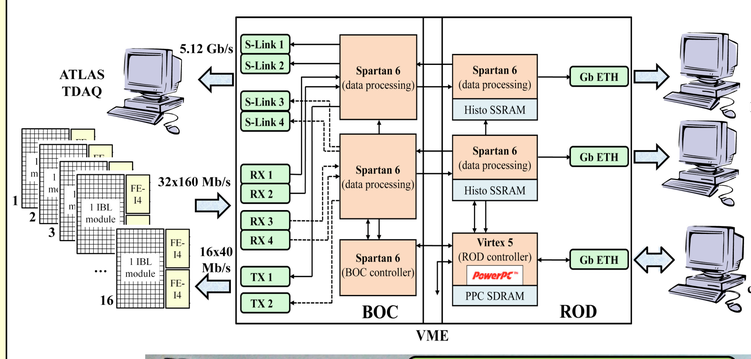
The ATLAS IBL ROD card



Number of pixels 6.02 x 10^6
Pixel size : 50 x 250 um
<R> = 33 mm |Z| < 33.2 cm
14 Staves 224 Modules



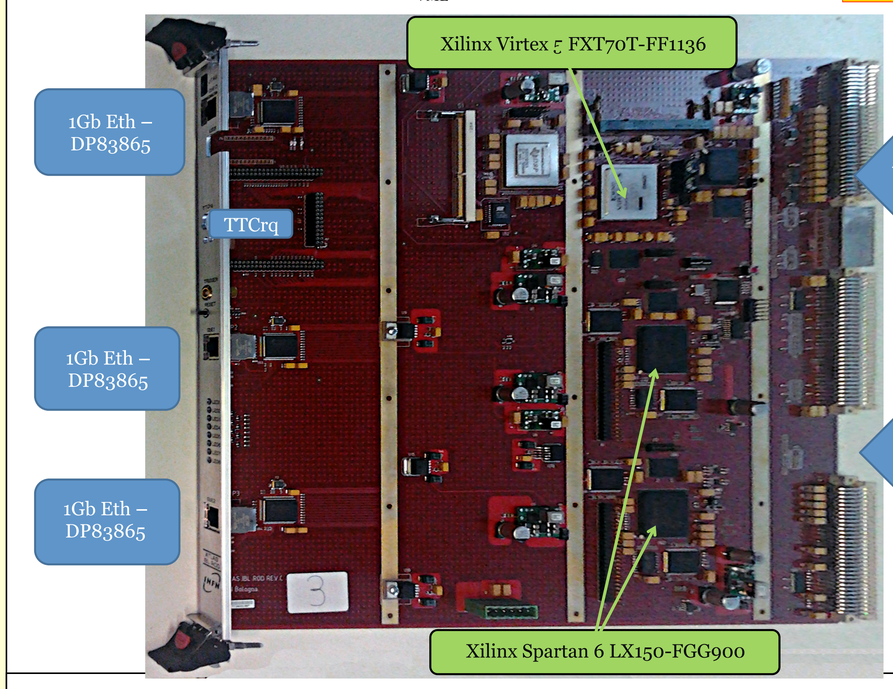
The **ATLAS experiment at LHC** planned to upgrade the existing Pixel Detector with the insertion of an innermost silicon layer, called **Insertable B-layer (IBL)**. The project has been designed in order to increase the tracking robustness against failures as well as to improve the measurements precision even at the higher LHC luminosities. The IBL has been **installed during the current LHC shutdown**.
IBL **read-out electronics has been redesigned** in order to accomplish increased performances. A **new front-end ASIC**, called **FE-I4** has been developed to take the larger occupancy and bandwidth into account. Two limiting factors (obsolescence of components and the maximum bandwidth of VME bus, currently used to readout data during calibration runs) led to a new off-detector design, consisting **of two 9U-VME cards: Back-of-Crate (BOC) and Read-Out Driver (ROD)** respectively implementing optical I/O interface and data processing.



20 Rev D pcb planned for IBL
- **14 for the IBL pixels**
- **1 for DBM**
- **5 as spare cards**

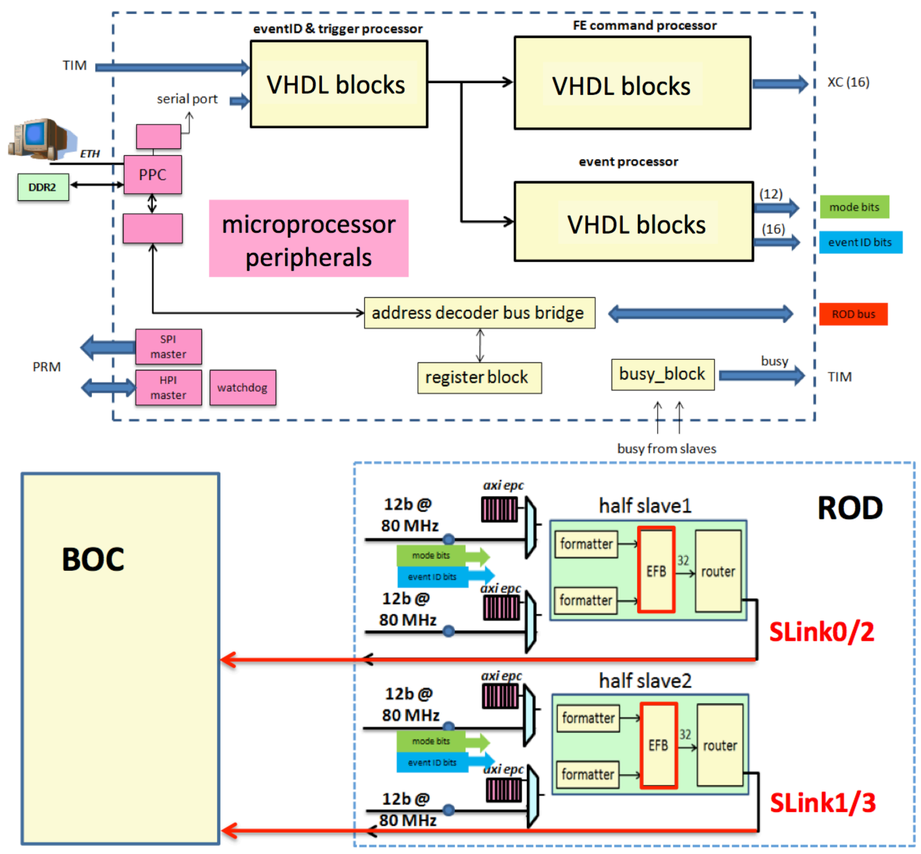
- **14 today running in USA15**

IBL off-detector electronics



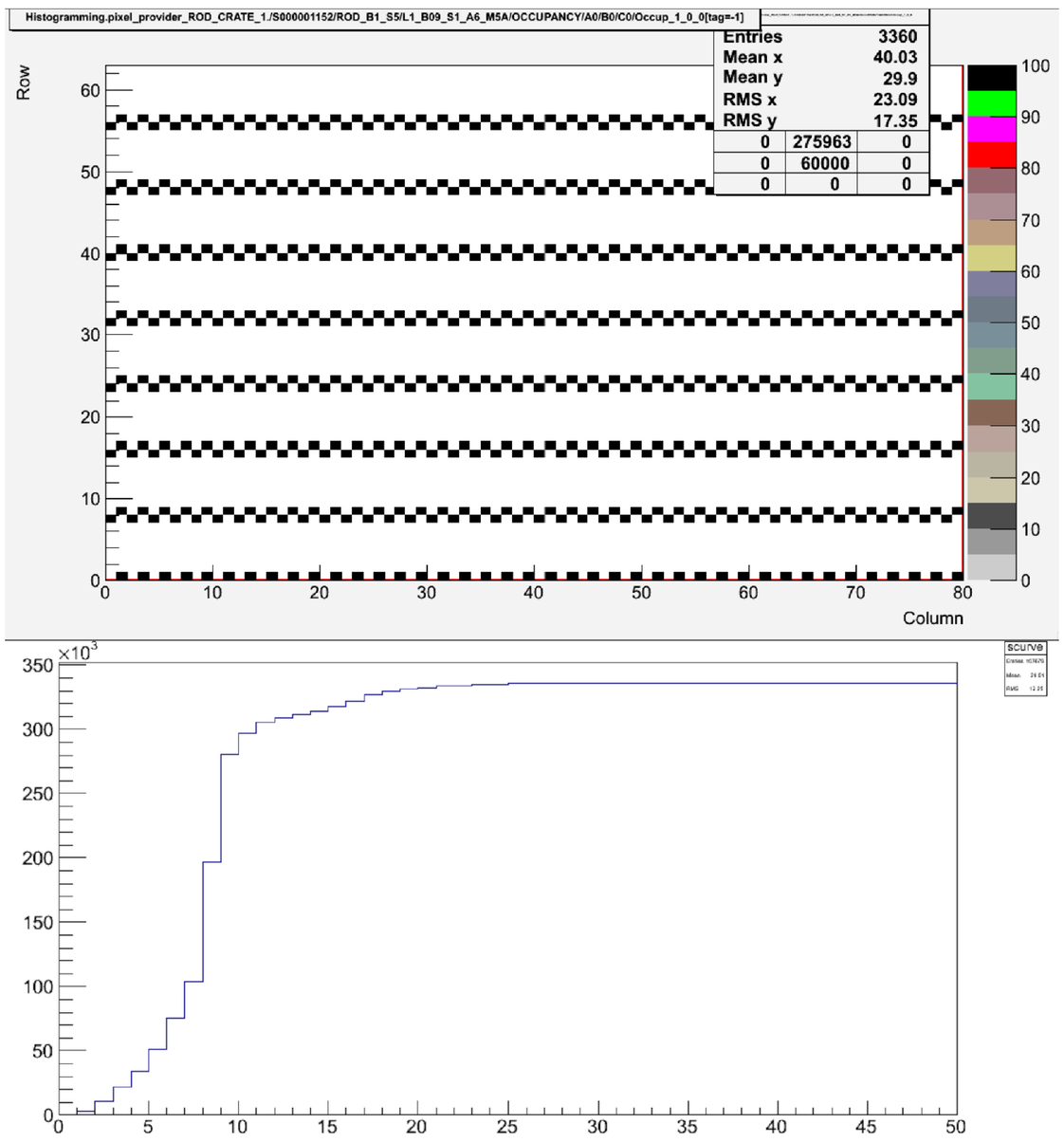
VME 9U 14 layers PCB

Firmware Blocks



Data taking with 32 FeI4 emulators per BOC-ROD, event frame with 8 random hits
Data taking with 2 real FeI4 (with 6 multiplexed copies) on 8 channels (1 SLink) up to 200 KHz
TIM trigger rate: 200 KHz, Test with a TIM-BOC-ROD, ROBIN + PC at CERN

Calibration Runs



Digital scan with 100 triggers, doing 1 of out 8 mask steps

Threshold scan run from the Console: s-curve from all pixels in the chip in one plot

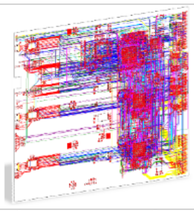
Summary

The 14 RODs for the 14 staves of IBL have already been delivered to CERN and, currently, these boards are running in USA15. Spare 6 boards are still under rework and will be delivered also to CERN very soon.
ROD Firmware is done, each board can interface with 32 FEI4 chips, data taking and calibration also work.
The entire software-firmware system debug is ongoing so that the ROD code is continuously under development for a fine-tuning.
The IBL ROD card is also going to be used for the Pixel Layer 2 readout upgrade, still by the end of 2014. Particularly, 26 boards will be used for the layer 2, and the IBL firmware will be slightly adapted to interface with FEI3 chips instead of FEI4 ones.

Available under Shared Documents at:
ATLAS Insertable B-Layer > Off-detector WG >
> Shared Documents > Readout System > Drafts

The manual is being upgraded with the description of the specifications required by each firmware block. In particular the following paragraphs describe each block:
- Functionality
- External interfaces
- Input data format
- Output data format
- Performances
- Implementation
- Error handling
- Registers

IBL ROD BOC Manual
Developer Version



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ROD Test Procedure

T3M00289
Created Wednesday 05 February 2014
- [x] CERN 28/01/2014 Wednesday
- [x] Visual inspection
- [x] Power supply test
- [x] Temperature test
- [x] PLL Clock test
- [x] Jtag chain check
- [x] V5-S6 Bus check
- [x] BOC2ROD
  - [x] AA55 0
  - [x] AA55 90
  - [x] AA55 180
  - [x] AA55 270
  - [ ] Counter_0
  - [ ] Counter_90
  - [ ] Counter_180
  - [ ] Counter_270
- [x] SSRAM 200MHz
- [x] DDR2 S6
  - [x] A
  - [x] B
- [x] Ethernet S6
- [x] DDR2 V5
- [x] Power supply screws substituted
- [x] ROD BUS
- [x] PROM Standard FW program
- [x] TIM +
- [x] ROD2BOC (S-Link + Ctrl)
- [x] Loaded prom Files (Leds V5 + first_check S6)

ROD

This is the Logbook of ROD

ROD:T3M00289	SENT
ROD:T3M00290	SENT
ROD:T3M00291	SENT
ROD:T3M00293	SENT
ROD:T3M00300	SENT
ROD:T3M00298	SENT
ROD:T3M00299	SENT
ROD:T3M00301	SENT
ROD:T3M00302	SENT
ROD:T3M00303	SENT
ROD:T3M00292	SENT
ROD:T3M00294	DONE
ROD:T3M00295	SENT
ROD:T3M00296	SENT
ROD:T3M00297	SENT

To validate the ROD boards a test procedures has been designed: a set of independent tasks are carried out on each board to test the individual features and I/O communication ports.