Development of an Optical Front-end Readout System for the LHCb RICH HPD Detectors.

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Introduction

This is a continuation of work from ‘Evaluation Of An Optical Data Transfer System For LHCb Detectors’, 7th Workshop on Electronics for LHC Experiments.

- LHCb RICH General Readout Architecture.
- Proof Of Principle Of A Single HPD channel Readout.
  - Level_0 & Level_1 hardware.
  - Choice Of Component For Controller Chip And Memory.
  - Block Diagrams Of Control Functionality.
  - Demonstrated Readout Using Slink.
- Using DLLs (Delay Locked Loop) In The FPGA Chip.
- Summary And Future Work

LHCb RICH General Readout Scheme

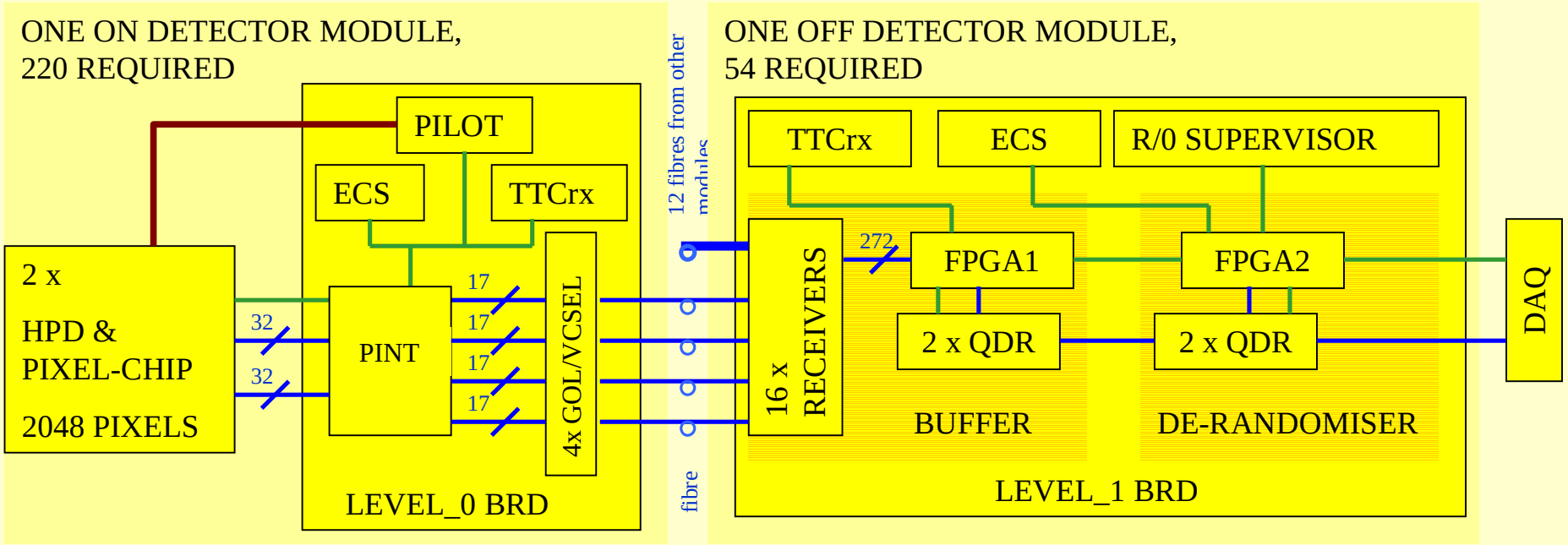
PIXEL-CHIP MULTIPLEXES 1024 TO 32 IN 800ns.

PINT DE-MULTIPLEXES (2x32) CHANNELS TO (4x(16+1)) FOR 16 BIT WIDE GOLs.

FOUR OPTICAL FIBRES/LEVEL_0 BRD TRANSFER DATA TO THE LEVEL_1 BRD.

ONE LEVEL_1 BRD ACCEPTS DATA FROM 16 FIBRES AND STORES IT IN 2 QDRs.

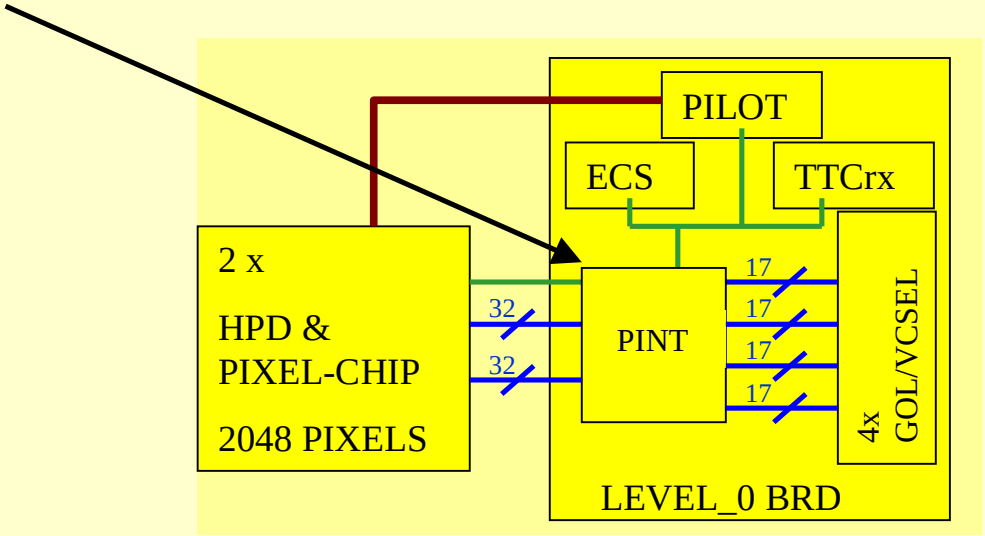
TWO FURTHER QDRs ARE USED TO DE-RAMDOMISE.



Components Of The Level_0 Brd

PINT (Pixel INTerface) . Algorithms are written to use triple redundant logic.

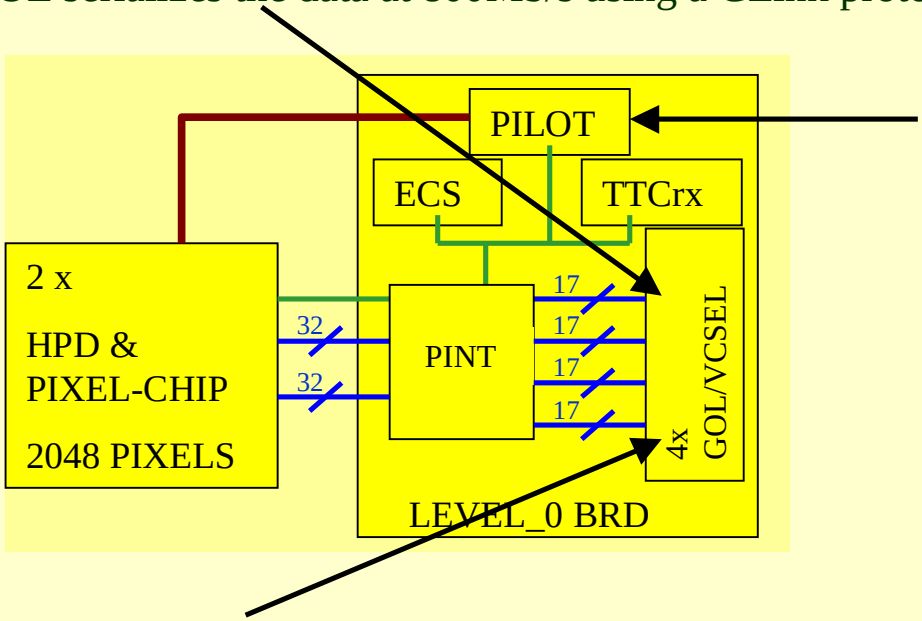
- Accept 32x32 data bits from 2 HPDs on an average 1 MHz level-0 trigger signal.
- Do voltage level and signal protocol translation for interface requirements between other hardware.
- Interface to the TTCrx for 40.08MHz CLOCK, L0 triggers, and control signals through Channel B. Communicate with ECS via a JTAG protocol.
- Add parity, error flags and Bunch count ID to event data therefore increasing the packet size to 32x36x2. Split the data into four channels i.e 17x32x4.
- Store the L0 triggers and generate the control signals for the PIXEL and GOL chips



Components Of The Level_0 Brd

GOL (Giga-bit Optical Link) A CERN rad hard ASIC.

- 2 GOL chips per HPD are required to serialize and transmit the data through the optical links, using the G-Link protocol, therefore 4 GOLs/brd.
- The GOL serializes the data at 800Mb/s using a GLink protocol. (it is also capable of 1600Mb/s)



PILOT, A CERN rad hard ASIC.
A DAC for biasing the Pixel chip.

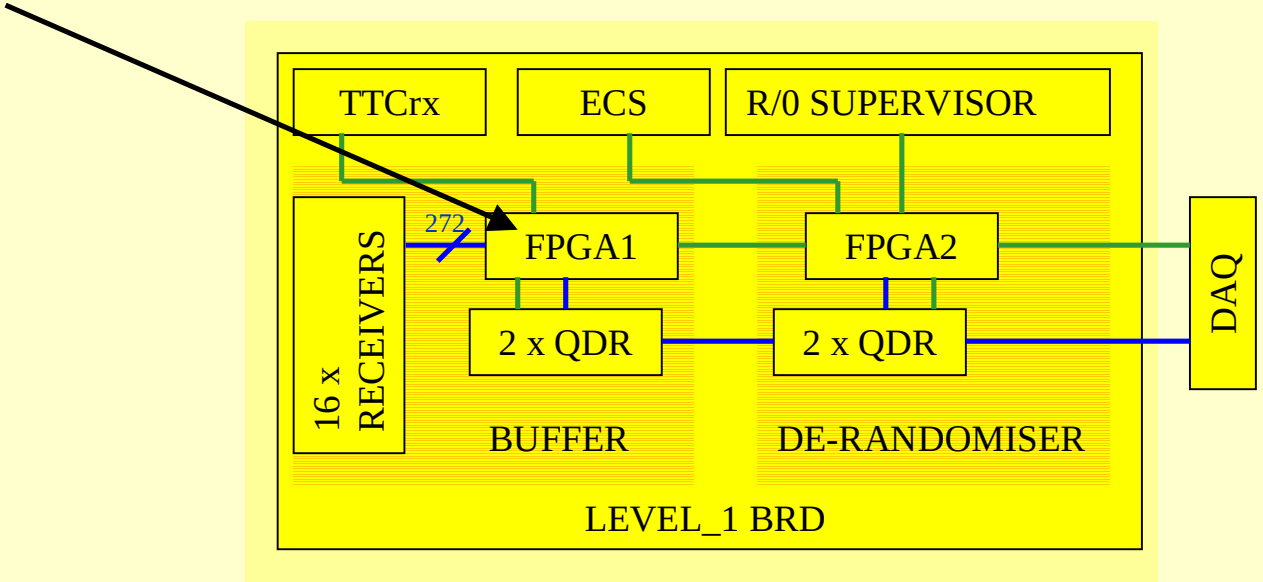
VCSEL (Vertical Cavity Surface Emitting Laser) commercially available.

VSCELs use wavelength ranges 650-850-1300nm for optical transmission and are robust in radiation and magnetic environments.

Components Of The Level_1 Brd

FPGA1

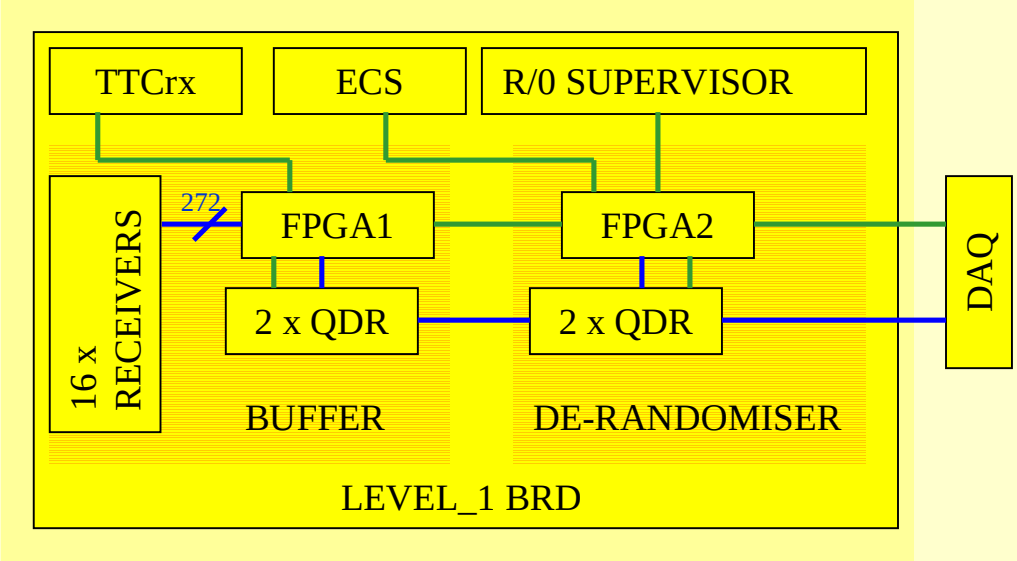
- Accept data from the level_0 @ 640Mbits/S per fibre. Sixteen fibres/brd.
- Interface to the TTCrx for Clk, trigger,bunch ID etc.
- Generate control signals for buffer QDRs.
- Check incoming data using Bunch ID, parity and cyclic redundancy.
- Add further information for Level_1 buffer ID and checking.
- Pass data out on a level_1 ‘YES’ to de-randomiser.



Components Of The Level_1 Brd

QDR (Quad Data Rate SRAM)

- QDR Buffer: Store up to 2K events for 8 HPDs during the level_1 latency of 2ms at a possible continuous 40MHz rate. This has now changed to ~50ms and a study of increasing the QDR depth is being carried out.
- QDR de-randomiser: Temporarily store data under FPGA2 control.

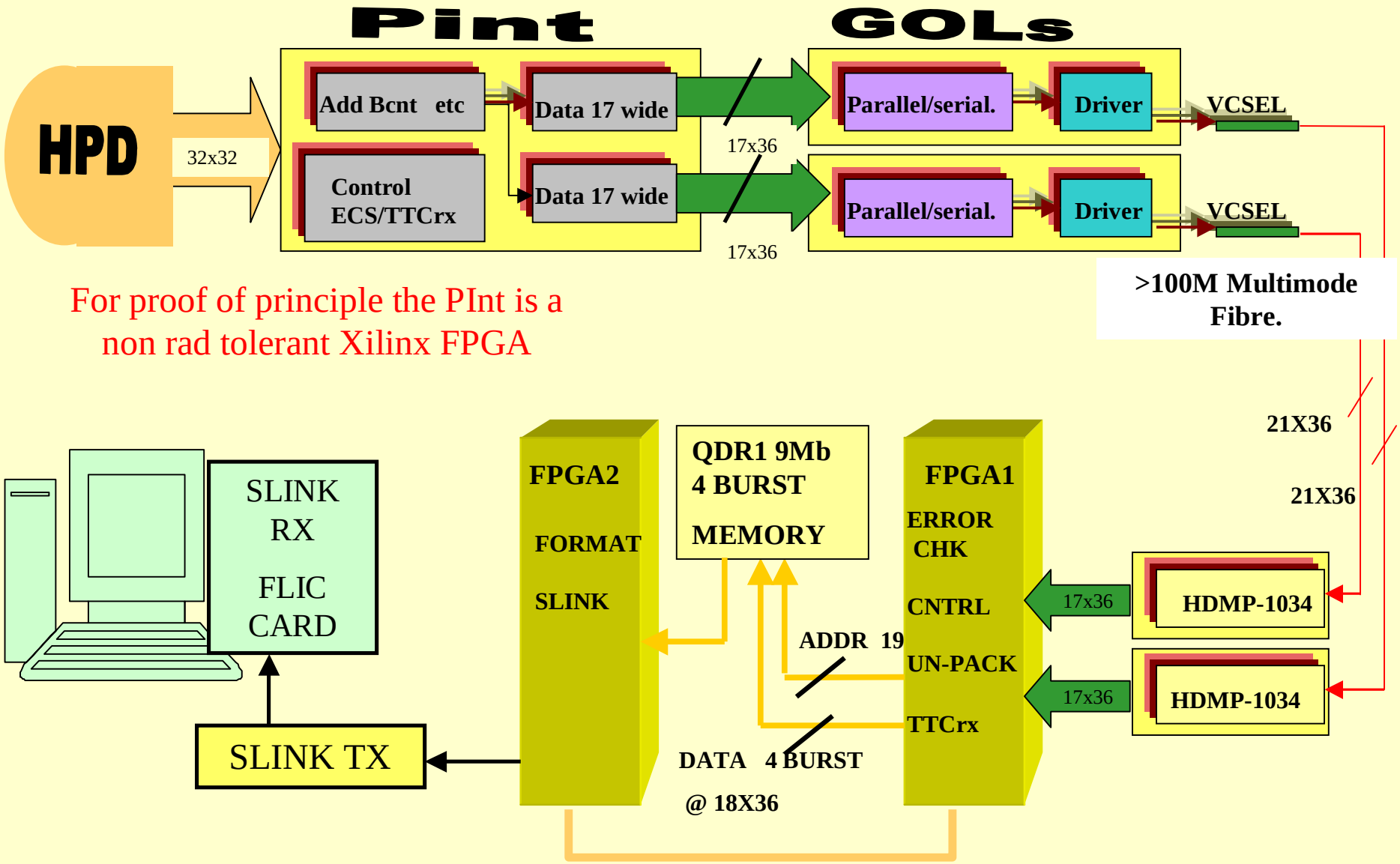


FPGA2

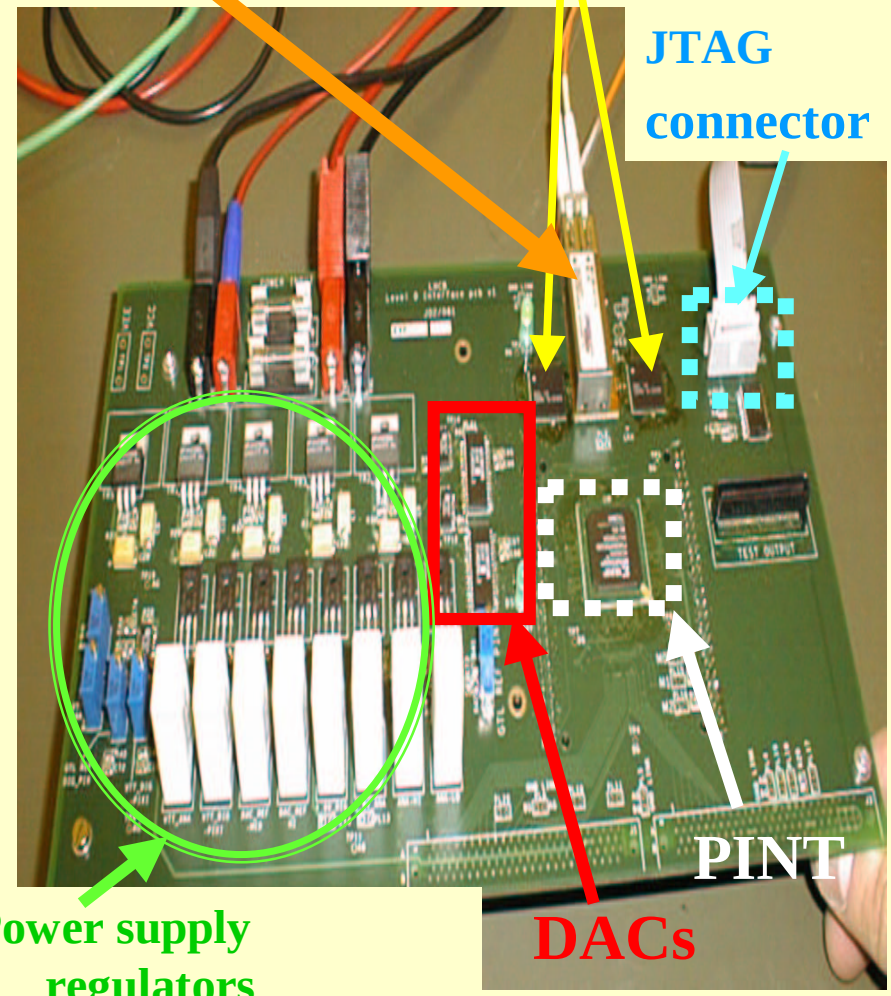
- De-randomise data.
- Interface to DAQ system, possibly using Ethernet.
- Raise error flags to ECS when appropriate.
- Zero suppress data if needed.

Proof Of Principle Stage

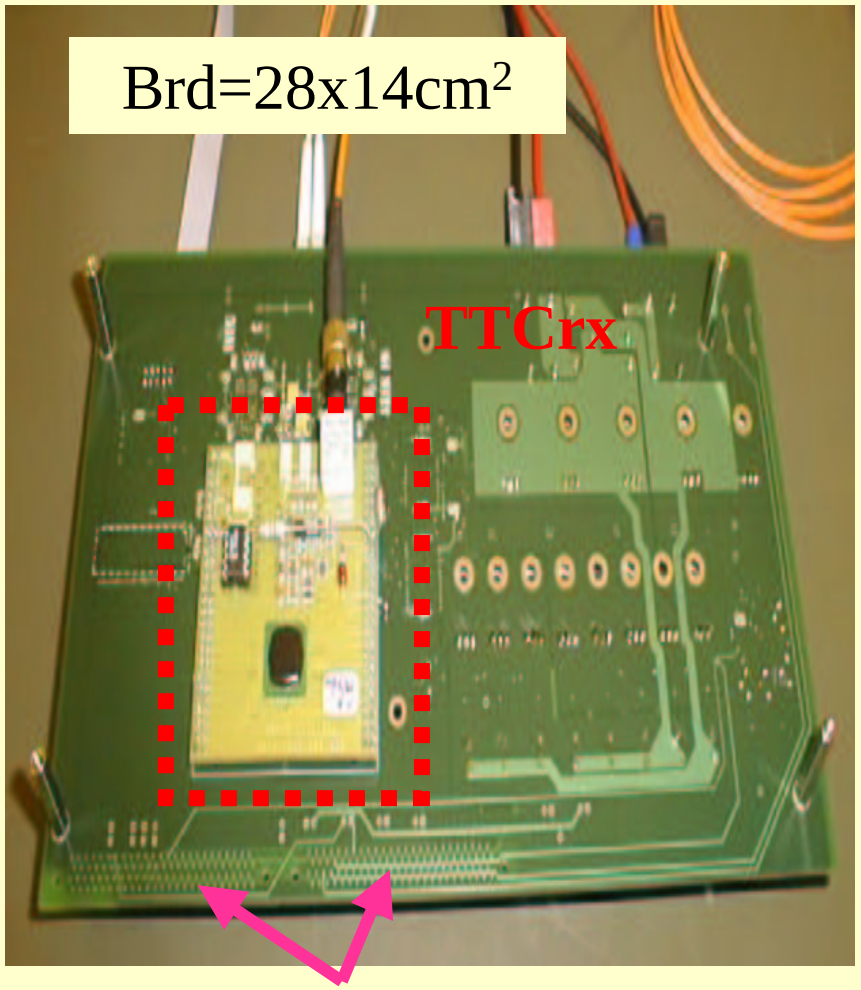
Hardware For Proof Of Principle



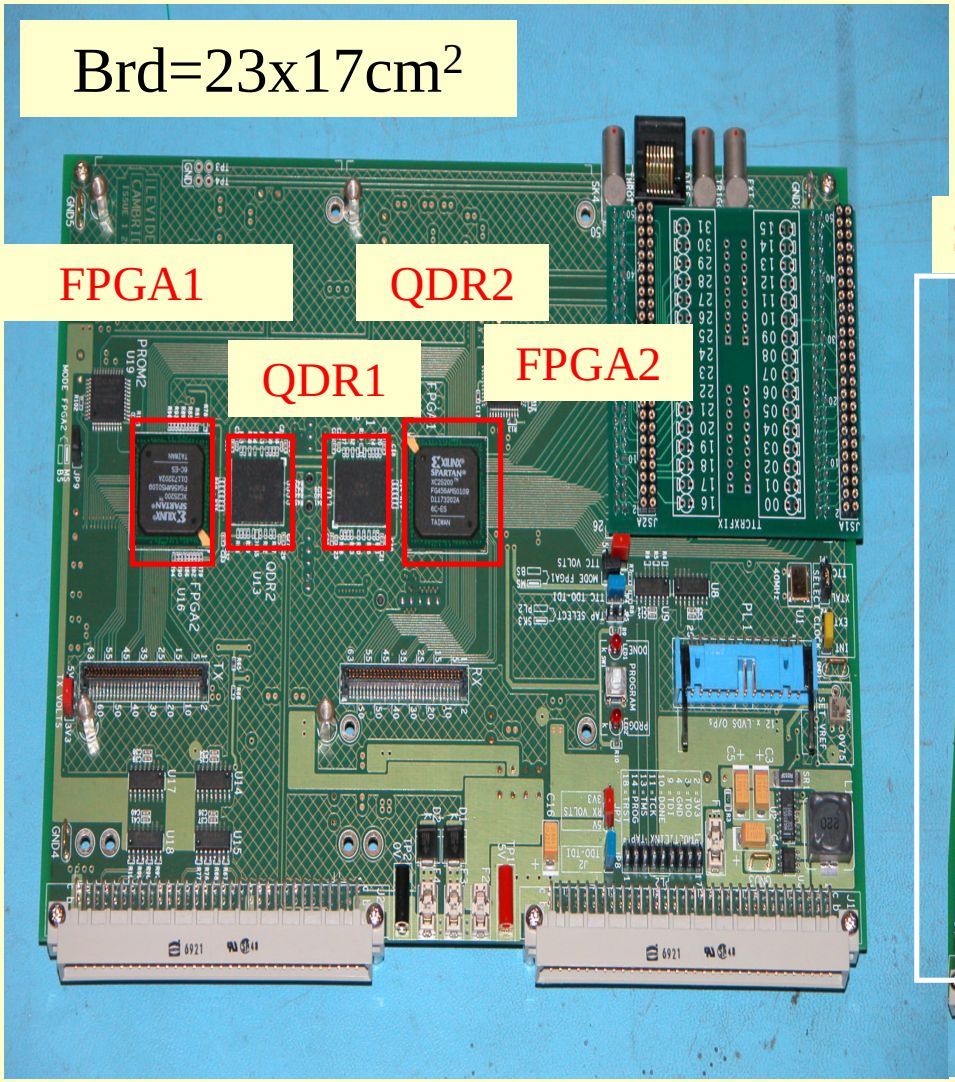
1st Prototype Level_0 brd For One HPD, 2 Fibres



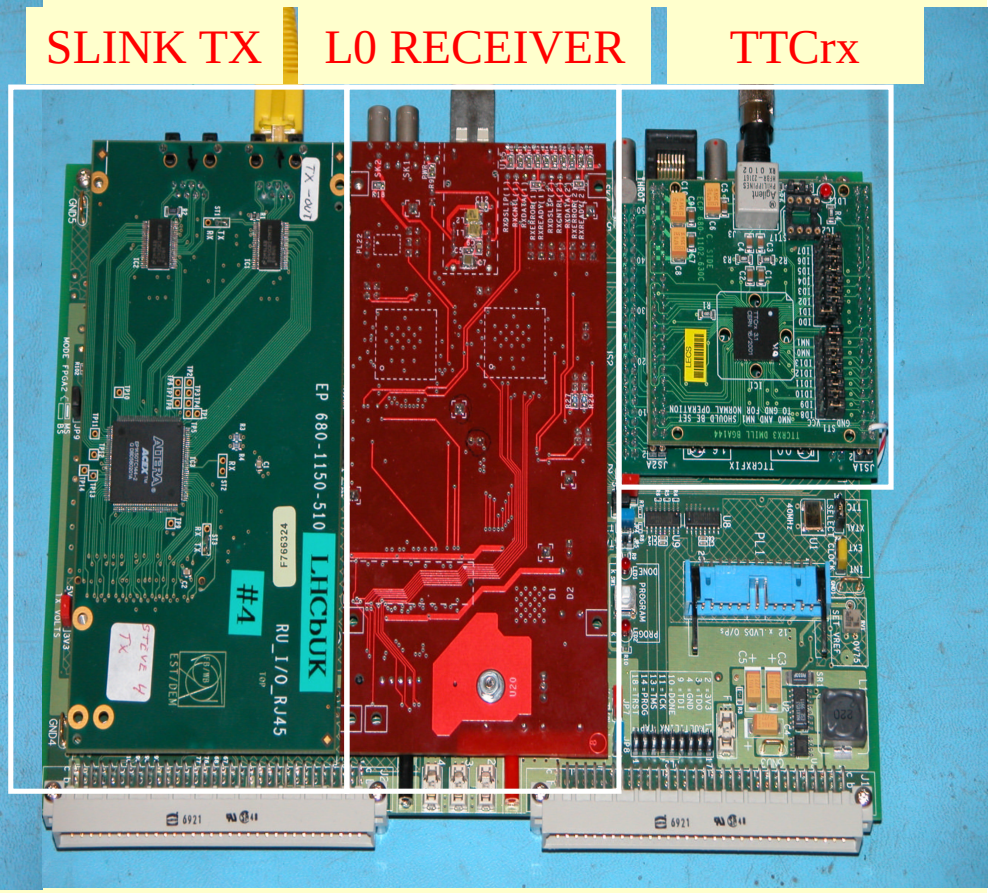
Back side



1st Prototype Level_1 brd; Able To Interface To One Level_0 Brd



Loaded with sub modules

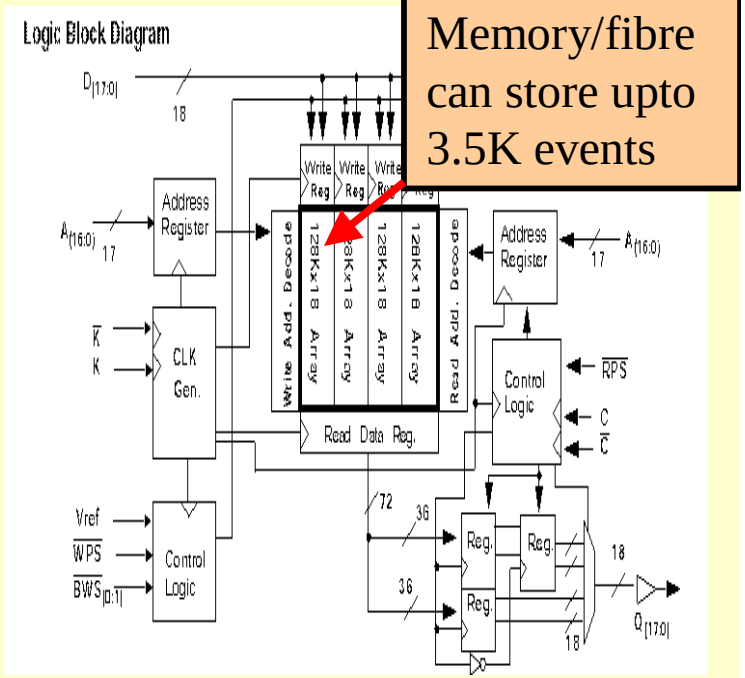


Choice Of FPGA'S

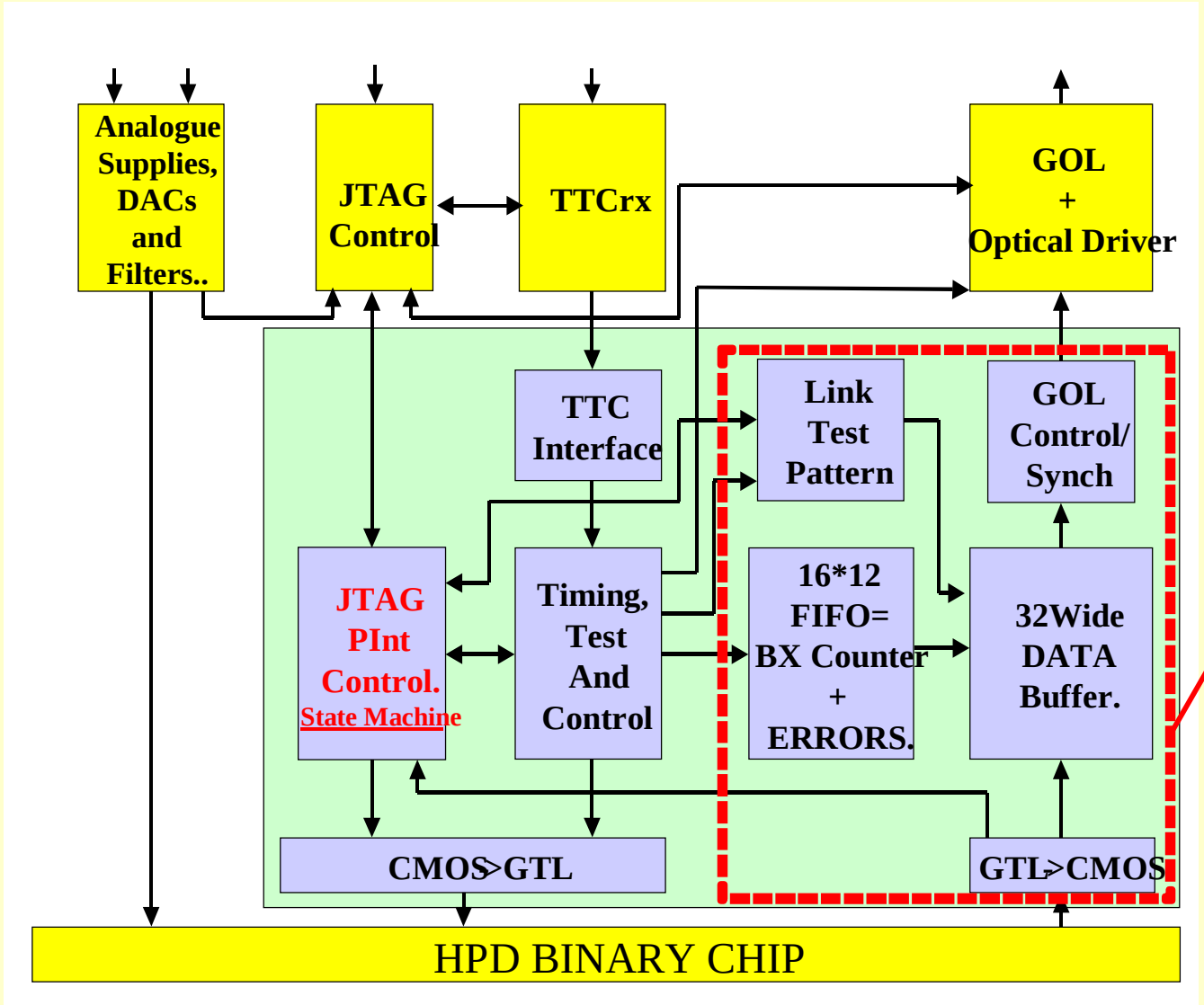
- Currently using the Spartan II XC2S200 FG456 as a solution to the QDR controller and PInt
- The Spartan II offers 200,000 system gates, >5000 logic cells.
- 284 I/O and 16 selectable I/O standards.
- Internal system performance of 333MHz and I/O at 200MHz.
- A unit cost of < £40.
- Work is now ongoing to port the PInt algorithms into a anti-fuse ACTEL AX1000 for radiation qualification. The general specs are the same as the Spartan although the AX1000 has more I/O.

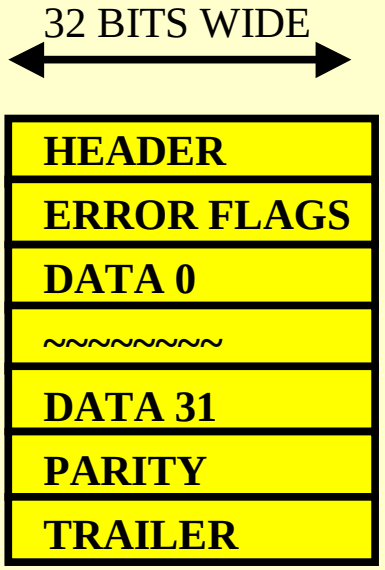
Choice QDR Memory

- 9-Mb Quad Data Rate Static RAM (18x512).
- SAMPLES FROM Micron. MT54V512H18EF
- 4-Word Burst for reducing address bus frequency
- 133MHz clock frequency (266 MHz data rate).
- Our use is 40MHz (80 MHz data rate) for 2 fibres.
- FBGA package (13x15mm^2 1mm pitch).
- Larger devices are now available, possibly up to 72 Mb. This will be considered now there has been an increase in L1 latency.
- A design exists for using a QDR at 80MHz (160 MHz data rate) and four fibres, but this is not being used at this stage of testing.



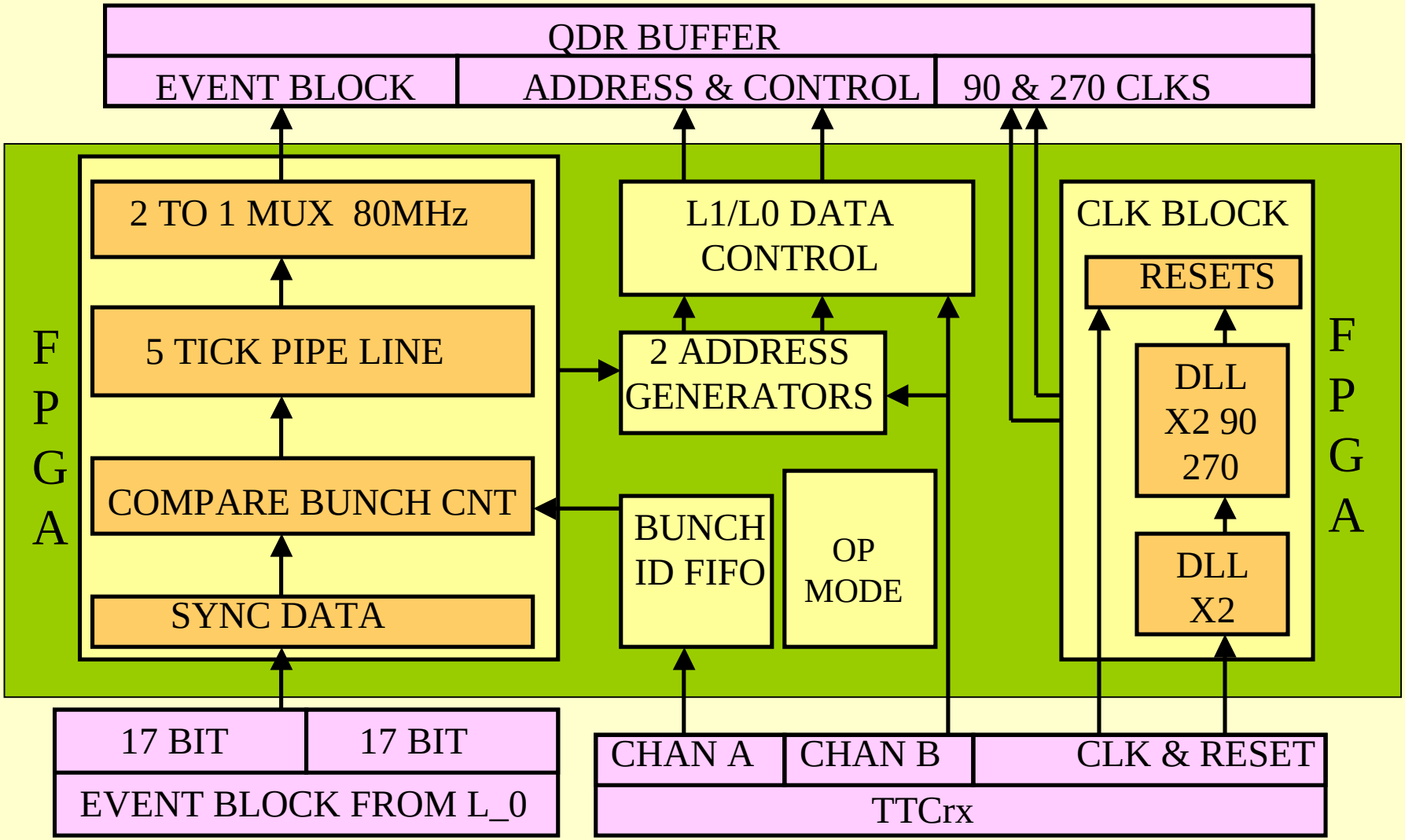
Proof Of Principle Functionality Of The PInt





All logic has been implemented with triple redundant cells.

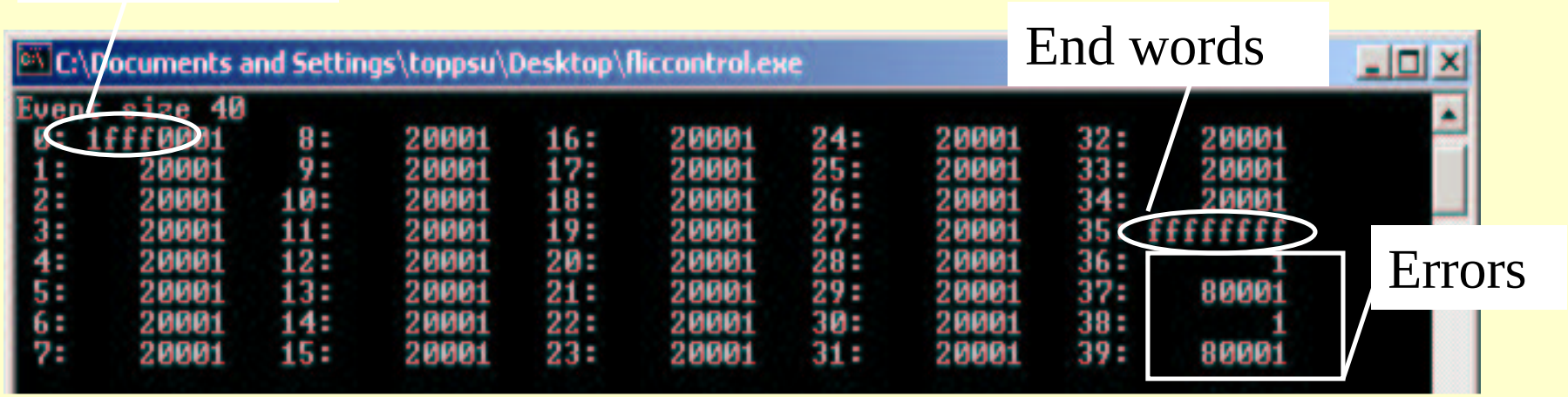
Proof Of Principle Functionality Of FPGA 1



Proof Of Principle Functionality Of FPGA 2, Designed Simply To Interface To The SLink

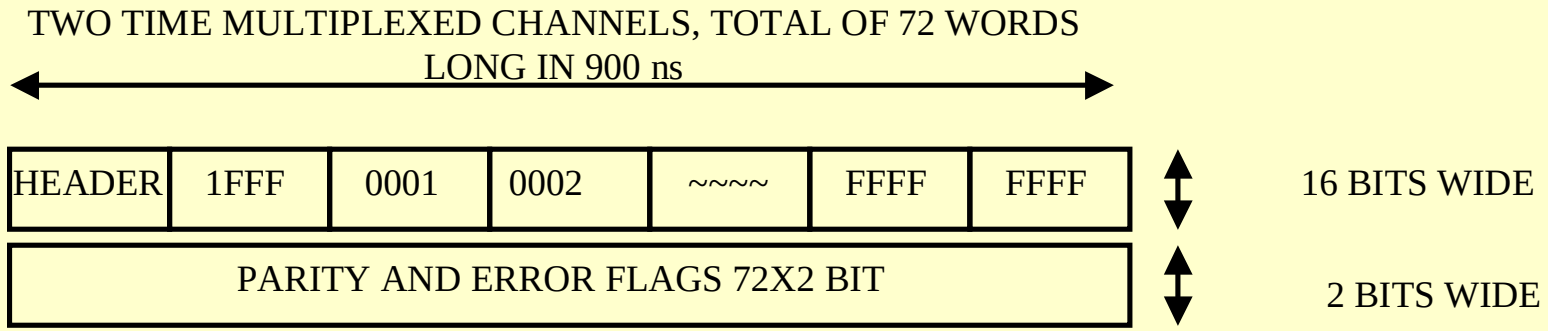
- Accepts event blocks from the QDR @ 1.44 Gbits/S. This is two event blocks at double data rate.
- Strips the 17^{th} bit (parity) and 18^{th} bit (error code) and formats them into end words
- Concatenates the two 16 bit data words into a 32 bit word.
- Generates all the necessary control and clocks for the SLink.
- Clocks out the data to the Slink at 20 MHz.

Test Data Readout Using Slink

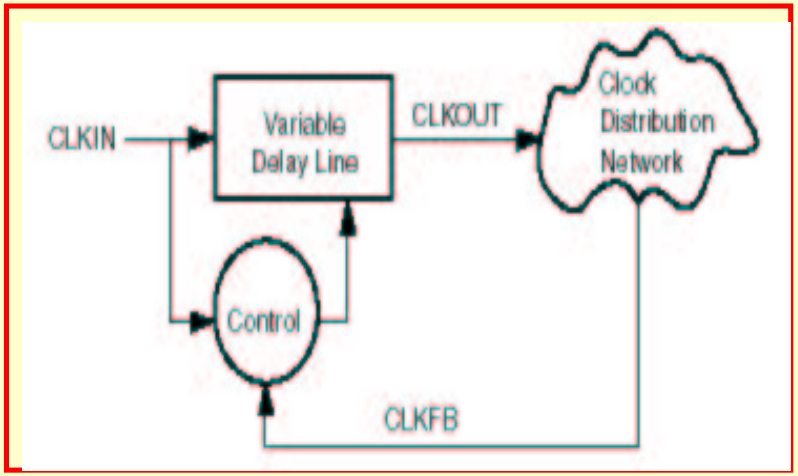


FPGA2 CONCATENATES THE 2X16 DATA INTO A 32 BIT WIDE WORD. THE 2 EXTRA BITS ARE STRIPPED AND ADDED AS WORDS AT THE END. FLIC IS READ OUT AT 20 MHz

DATA FROM QDR1 TO FPGA2



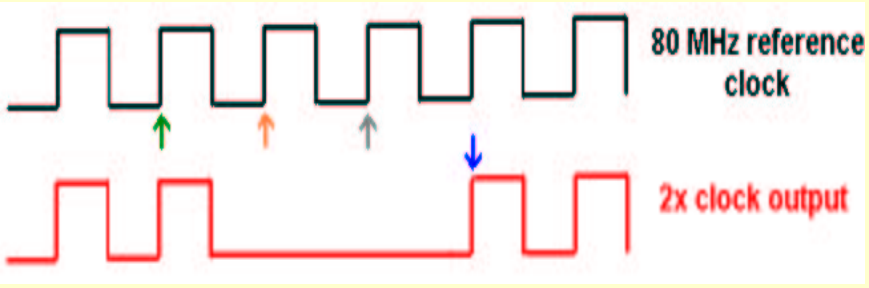
DLL, Delay Locked Loop



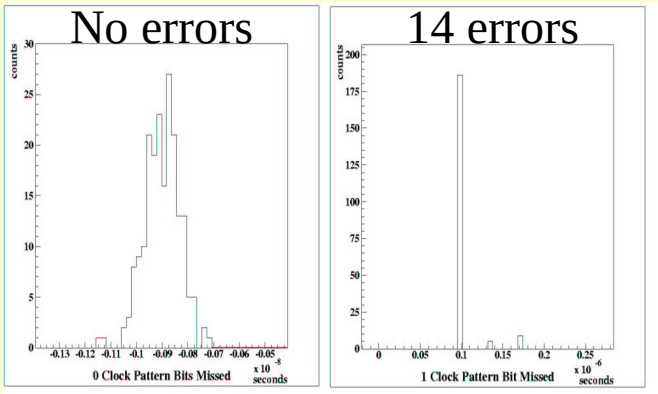
DLLs offer a locked signal and clock management: doubling, dividing and delay compensation.

Questions?

1) Can the lock signal be used to indicate missing input clock pulses.
2) How does a 2x output respond to a missing input clock pulse.
3) Can the DLL stand the jitter from a TTCrx. TTCrx version 3 was found to have a long term jitter, or drift of 400ps and a cycle to cycle jitter of +/-300ps. New TTCrx chips are now available with improved jitter.



When 1 input clock pulse is missed there are three peaks due to the three possible intervals the oscilloscope could sample.



Histogramming the time between reference clock and the 2x clock the errors can be counted.

Conclusion:

1) There was no degradation found with the operation of the DLL with TTCrx.
2) 14 out of 16 input clock pulses can be missing before the out of lock signal is given.
3) A continuous no input clock situation can have a duration of 100 us before lock is lost.
4) The Lock signal can be used for Locked-on but not loss of lock.

Summary

- A conceptual modular design for the RICH HPD is in place.
- Hardware and chip algorithms exist for a single HPD readout scheme.
- Both Level_0 and Level_1 basic functionality has been verified. The full readout of the proof of principle electronics is now being debugged.
- DLL-TTCrx compatibility has been shown. The lock signal can not be used to show loss of synchronisation.

Future Work

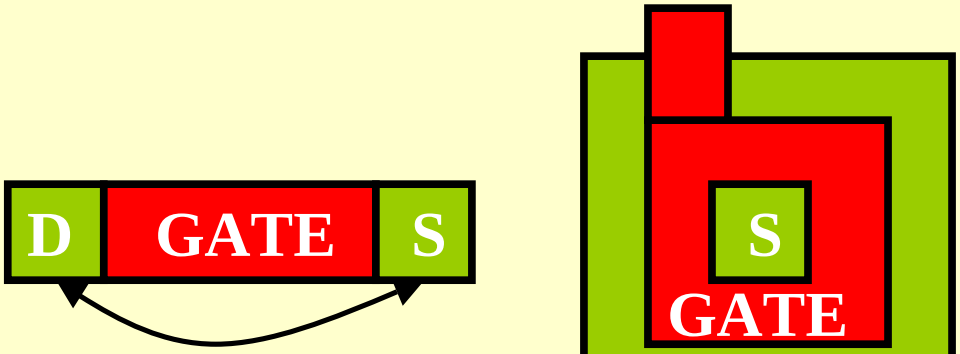
•The RICH detector baseline has changed from HPD to MAPmt. A redesign of the readout scheme is now in progress. An attempt to keep similar modularity, hardware and algorithms of the HPD scheme are being achieved.

•The buffer size of the Level_1 must be reconsidered. This may mean a different memory technology.

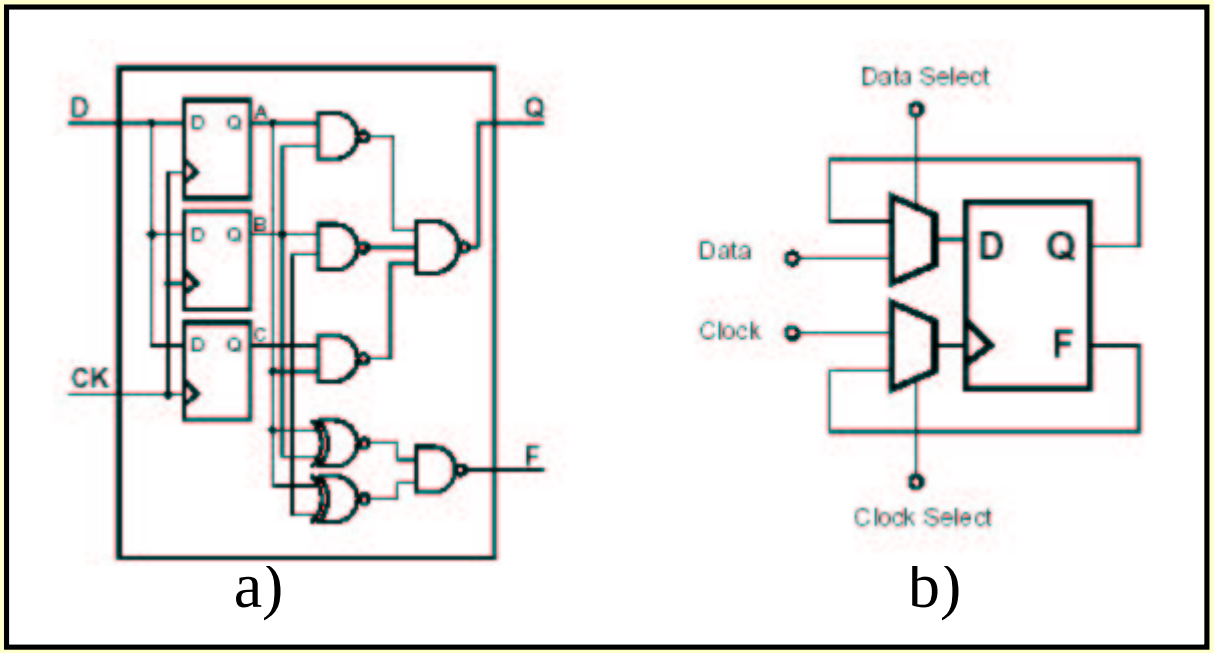
•Porting the PInt design from a Xilinx FPGA to an ACTEL has presented no problems so far. Radiation Qualification of the Level_0 system is in preparation.

•New proof of principle readout scheme with detector will be evaluated.

a) b)



a) b)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a) b)


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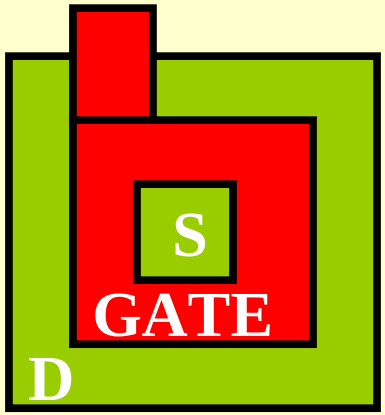
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a) b)

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management: doubling, dividing a
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