READOUT OF HIGH SPEED S-LINK DATA VIA A BUFFERED PCI CARD

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Abstract

The FLIC (Flexible I/O Card) is a general purpose PCI card with programmable logic, allowing the implementation of specific readout controllers with a large on-card data buffer. Mezzanine cards are used on the FLIC for signal or protocol adaptation to external systems. These mezzanines may comply with either the PMC standard or the CERN S-LINK convention, or they may provide implementation-specific circuitry. The first applications of the FLIC were PC-based data acquisition systems replacing CAMAC and VME controllers; the application discussed here is a high speed test system for pixel chips, where S-LINK is used to acquire data from a 40 MHz chip test station and store it at a high rate into the FLIC's local SDRAM buffer. From here it can be accessed at PCI bus speed by LabView-based analysis programs. Both the SDRAM controller and the S-LINK readout controller are implemented in a Lattice Field-Programmable System Chip (FPSC). The SDRAM is mapped via the PCI BAR mechanism into the host CPU's memory space and can hence be read out either under Linux, using the mmap() functions, or under Windows, using a specially developed DLL.

1 INTRODUCTION

The LHCBPIX1 chip is an 8,192 pixel silicon detector chip to be used in the HPDs (Hybrid Photon Detectors) currently being developed at CERN for the RICH (Ring Imaging Cherenkov) sub-detectors of LHCb. The latest version of the chip is designed to run clocked at 40MHz [1] (the proton-proton bunch-crossing rate of the LHC), reading out at 1MHz. A new test system was therefore required, since the existing system [2] works only at 10MHz (the heavy ion bunch-crossing rate of the LHC).

The 10MHz test system developed by members of the ALICE experiment was based on a number of modules. The pixel chip was wire-bonded to a carrier board, which plugged into a power and signal routing board that brought the lines for data output, control and JTAG configuration out to separate connectors. The data and control lines were connected to a 6U custom VME module known as the "Pilot" board, which supervised the readout of the chip, buffered and zero-suppressed the data. Finally, the zero-suppressed data was transferred to a PC via an MXI-II bus, using PCI-MXI-II and MXI-IIVME interface boards. LabView software running on the PC was responsible for configuring the pixel chip and the intermediate boards and for collecting and analysing data via JTAG or VME. A VME-based JTAG controller was used to configure the pixel chip and ancillary boards. A PC running custom LabView software controlled the DAQ system.

1.1 Readout System Requirements

Due to the modular nature of the test system, only those hardware components active in the readout chain needed replacing in order to upgrade the system to 40MHz operation. Notably, the power and signal routing board and the chip carrier board required no modification. The Pilot board was limited to 10MHz and needed replacing. The existing LabView control and monitoring software was adapted to the new readout system via a new driver.

2 NEW TEST SYSTEM

2.1 Introduction

Due to the 40MHz readout requirement VME and MXI-II bus solutions were rejected and a direct interconnection approach was adopted, avoiding intermediate interfaces. The PCI-FLIC card [3,4] developed at CERN was chosen as the readout electronics, interfacing the front-end electronics directly to the PC using the PCI local bus [5] as the interface.

At the physical layer, the S-LINK protocol [6] also developed at CERN was used, allowing standard mezzanine cards to be used at the FLIC end of the link. A custom interface to the existing front-end electronics, including a S-LINK transmitter, was also developed.

2.1 Hardware

The hardware for the new test system is rather simpler than that used previously. The front-end and biasing electronics are combined with a customised readout stage running at 40MHz, which transmits the data from the chip via its embedded S-LINK transmitter [fig.1].

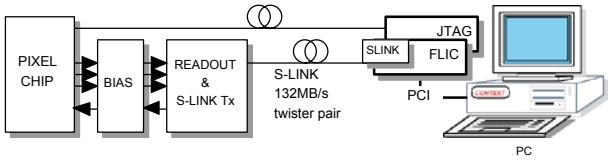

Figure 1 block diagram of the new test system

A Category-6 cable connects this card to the PC, where the readout controller (the FLIC) and a PCI JTAG controller run under the control of LabView software.

The FLIC is a general-purpose I/O card [fig.2] designed to allow commodity PCI-equipped PCs to replace VME-based DAQ systems such as that described here, using the FLIC as the readout controller. PCI has previously been used in VME systems in the form of mezzanine cards; the FLIC allows the re-use of such components, via either a custom connector or a PMC/CMC connector [7].

Figure 2 The PCI-FLIC card

As can be seen in fig. 3, the FLIC consists of a PCI-PCI bridge chip, 64MB of on-board SDRAM and a Lattice "ORCA" series Field Programmable System Chip (FPSC): a normal FPGA with an embedded PCI ASIC. Three PMC connectors and two custom connectors (for S-LINK and user signals) are available for interfacing to mezzanine cards. For controlling external systems, two coaxial LVDS inputs/outputs are available; used in this case for resetting and triggering the front-end electronics.

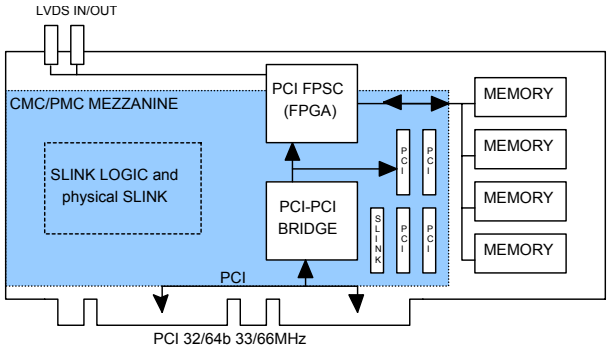

Figure 3 Block diagram of the FLIC card

The S-LINK receiver physical layer is implemented on a standard form-factor mezzanine card, using a CPLD and lost-cost interface technology, allowing data transmission at up to 132MB/s over a distance of 20 meters.

The S-LINK protocol carries control and error information with each data word transmitted across the link, allowing the receiving end to perform data identification and error handling. S-LINK control words frame the data blocks that contain the pixel data and this information is copied into SDRAM from where it is retrieved and analysed by the software. For this purpose the SDRAM is mapped into the PC memory address space. The S-LINK readout speed is 132MB/s but the PCI readout performance is often slower, since it depends on the PC's architecture, and on the software.

The readout control logic in the FPSC is an "S-LINK to PCI" buffered interface, implemented in VHDL [fig.4]. No on-board data processing is performed, since this can be done more flexibly in software.

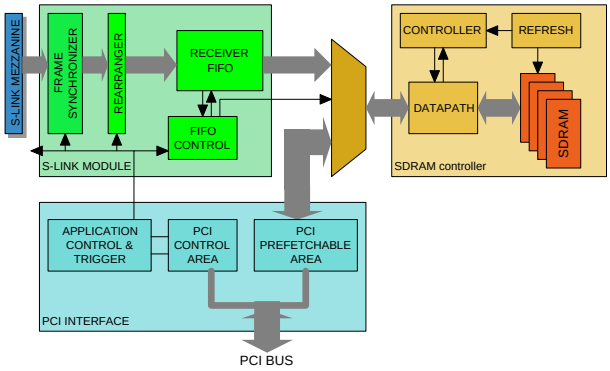

Figure 4 Block diagram of the HDL design

The event readout is controlled either by the FLIC or by an external controller; this maximises the flexibility of the test system. The trigger signal for the front-end electronics is transmitted via the LVDS I/O lines on the FLIC under LabView control.

The firmware (in VHDL) and PC drivers (in C) were developed simultaneously, using the PCI standard as the interface between hardware and software. In this way, the complete readout system was set up in only three months.

2.2 Software

The software environment from which the test system is controlled and monitored was chosen to be as similar as possible to the existing system, both to minimise operator retraining and to maximise code reuse. The original software was implemented in a highly modular form, and most of the work required to make it drive the new system consisted of writing a Windows device driver for the FLIC and LabView VIs to interface the new DAQ system to the existing control and monitoring VIs [fig.5].

2.3 Device Driver

The device driver portion of the software is a DLL written in C that interfaces to the runtime portion of Jungo Win-Driver [8]. The interfaces it provides are designed to keep the DLL as general as possible, encouraging its reuse in other FLIC applications. The essential functions it exports are as follows:

flicOpenBoard() opens the FLIC (a parameter allows the user to specify which one in a system containing several)

and returns an integer handle to it. The WinDriver handle (a pointer to a data structure containing information about the FLIC) is stored by the DLL in an array, the indices of which are the integer handles. This is done to work around the absence of pointer support in LabView. The function also sets the value of the CALN (CAche LiNe size) register in the configuration space of the FLIC's PCI-PCI Bridge to 0x10, the largest possible. Conversely, *flicCloseBoard()* closes the specified FLIC.

flicReadWriteBlock() reads or writes blocks of 32-bit words from a specified region of system memory to a specified PCI mapped memory area (identified by BAR, or Base Address Register), optionally plus a given offset. Similarly, *flicReadRegister()* and *flicWriteRegister()* read and write to the FLIC's memory mapped register space, addressed by BAR5. Finally, the functions *flicBridgeSetCALN()* and *flicGet-MemSize* are provided for the convenience of users: they set the value of CALN associated with the specified FLIC to a given value and return the size of the memory space associated with the given BAR respectively.

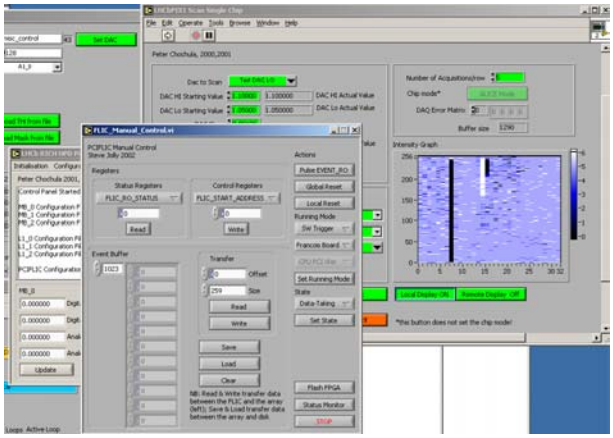

Figure 5 A screenshot of the user interface

2.4 Front End

To test the new DAQ chain and the Windows and LabView drivers, a FLIC control panel was created in LabView [fig. 5]. The panel controls all the functions of the FLIC, and interfaces to it using the same VIs (and DLL) as the data-taking and analysis VIs that form the rest of the test suite software. It allows all parts of the system to be tested for basic readout functionality, from the chip to the software.

Control of the FLIC takes place via the FLIC's memory-mapped register space. Sixteen registers are available, although several are reserved for compatibility with other FLIC applications. Some registers are counters, recording the number of events received via S-LINK, the number of triggers that the FLIC has sent or received, and statistics: the numbers of raw data words and errors received.

In addition, a status window monitors the five status registers of the FLIC, showing the values of the counters, and flagging memory overflows and other errors related to the PCI and S-LINK interface management

The FLIC control panel offers additional functionality: reading and writing to the memory is possible, as is flashing the FPSC on the FLIC with a new configuration. The ability to flash the FLIC via PCI without special hardware or mechanism is extremely convenient when updating FPSC code or exchanging cards between different hardware systems that share the FLIC as the readout controller.

3 CONCLUSIONS

A very compact test system capable of running at the 1MHz event rate of a 40MHz pixel chip has been developed, reusing as many as possible of the components from its predecessor, a VME-based system. Furthermore, the readout chain and analysis were simplified, increasing the system performance.

Using the combination of FPGA technology together with the PCI bus and mezzanine standards has allowed a readout system to be built rapidly and at very low cost. The use of PCI as the main backplane bus provides high performance and portability between different architectures and operating systems.

4 ACKNOWLEGMENTS

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