LHCb Vertex Detector Electronics Timing and Synchronization

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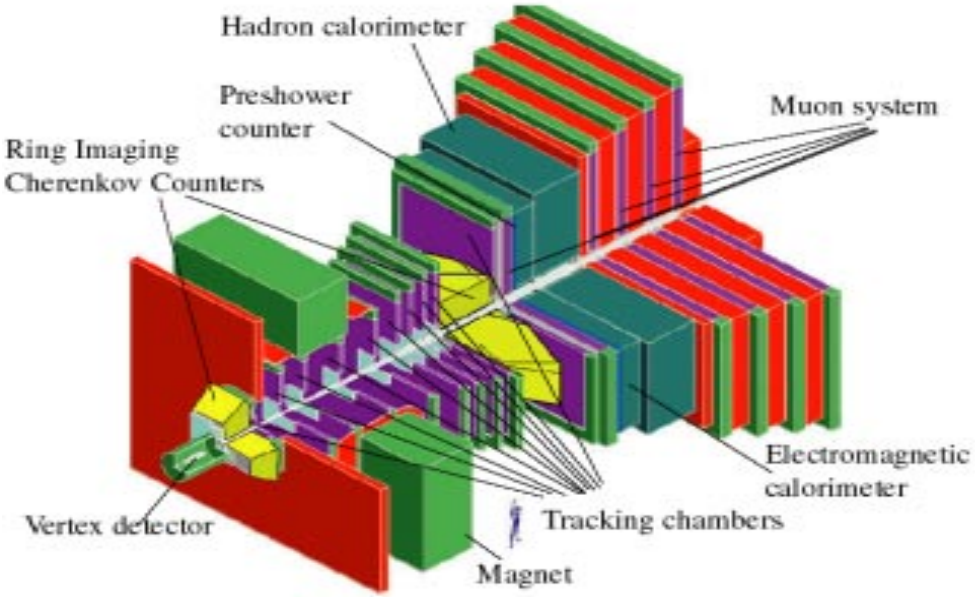
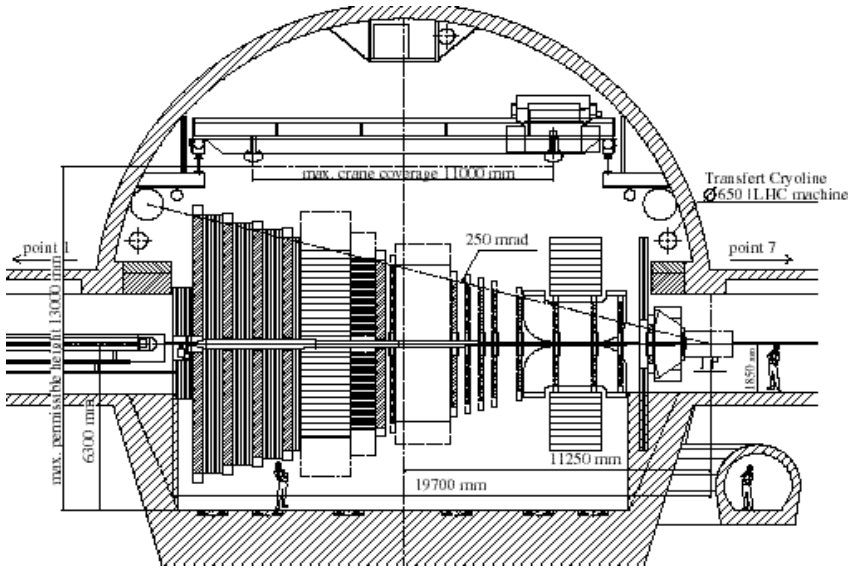
LHCb Detector

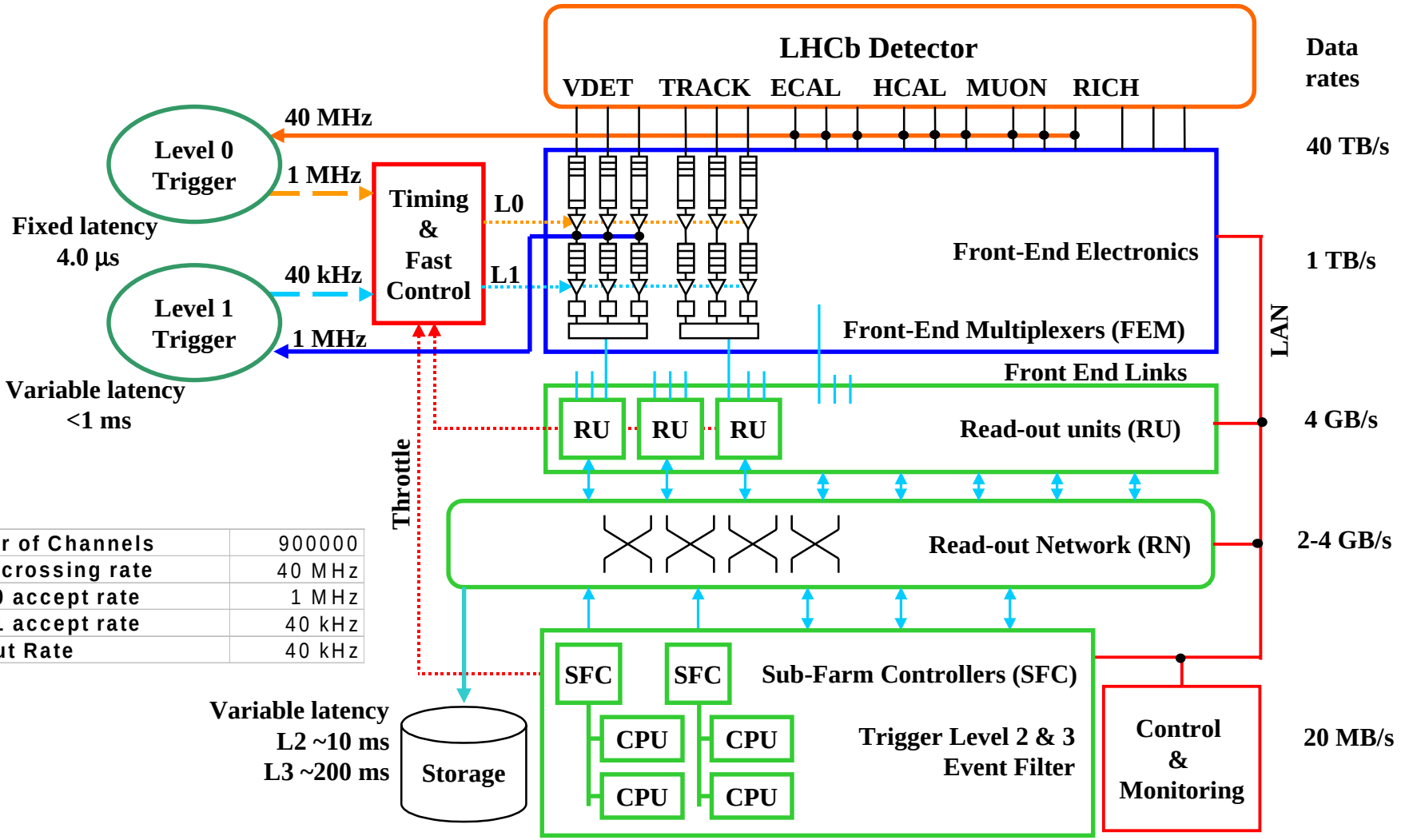


- CP Violation Experiment at the LHC
- Searches for rare B decays
- Single arm spectrometer



- Good decay time resolution
- Particle identification capability
- Good invariant mass resolution
- Flexible and optimized trigger

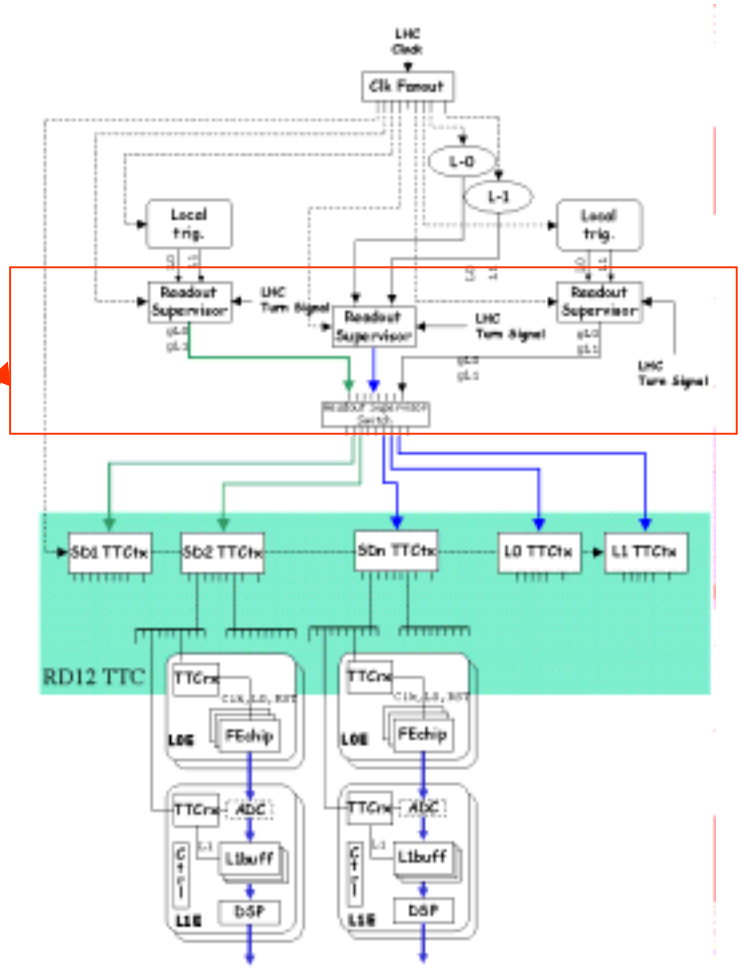
Trigger/DAQ Architecture



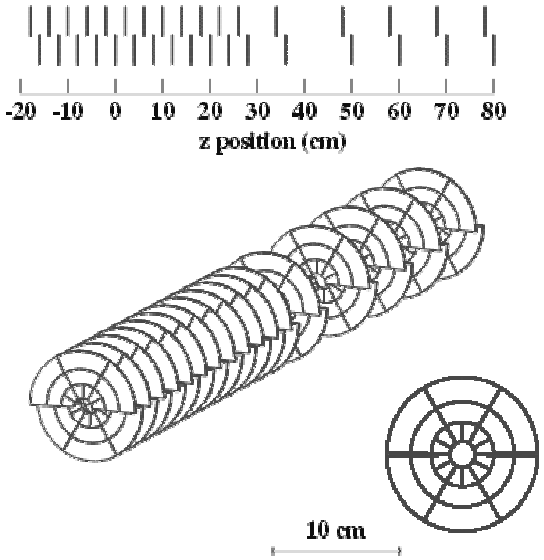
Number of Channels	900000
Bunch crossing rate	40 MHz
Level-0 accept rate	1 MHz
Level-1 accept rate	40 kHz
Readout Rate	40 kHz

Timing and Fast Control

- Provide common and synchronous clock
- Provide Level-0 and Level-1 trigger decisions
- Provide commands synchronous in all components (Resets)
- Provide Trigger hold-off capabilities in case buffers are getting full
- TTC (CERN/RD-12) as a backbone
- LHCb specific Readout Supervisor and Readout Supervisor Switch

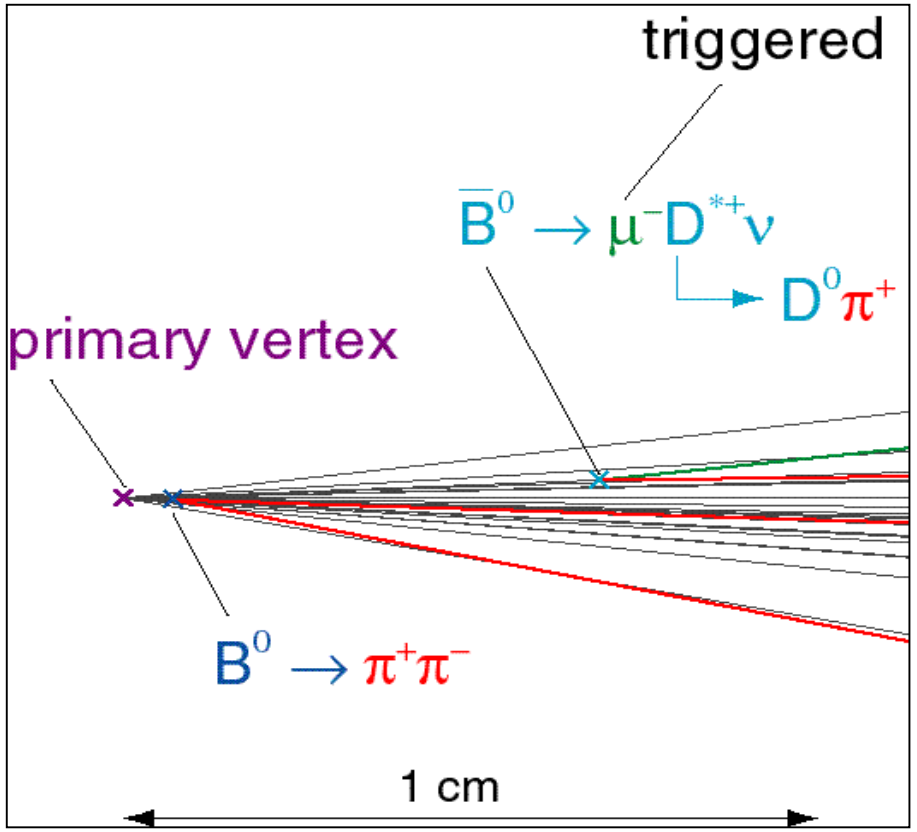


VELO - VErtex LOcator



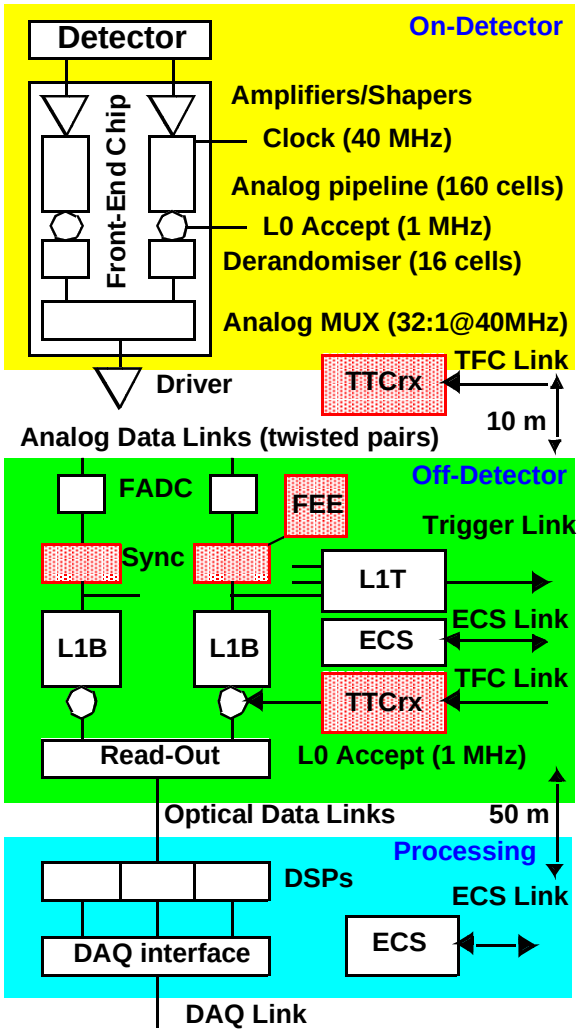
- 17+2 stations, top/bottom module, r+phi
- 220K detector channels in total
- Radiation harsh environment
- Analogue readout, all strips
- Fast track reconstruction (L1 trigger)

Typical event



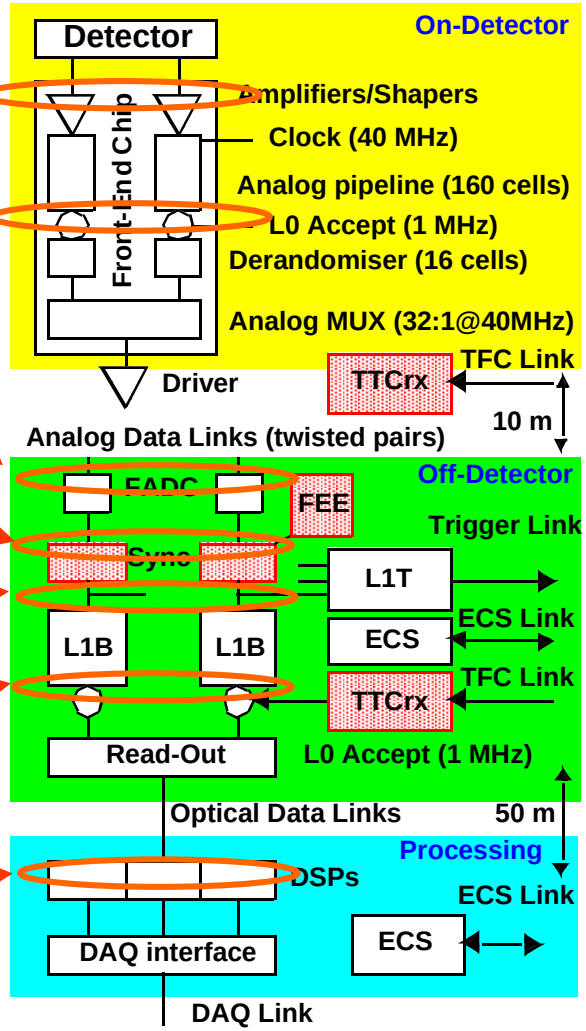
VELO Electronics

- **Front-End Electronics**
  - Radiation Hard (DMILL or deep sub-micron)
  - 128 ch read-out chip with 4 outputs (32:1)
  - 160 cells pipeline, 16 cells derandomizer
  - Analogue read-out at 40 MHz
  - Pipeline ID as Event ID, over 4 outputs
  - 900 ns read-out time (32+4)*25 ns
  - Clock, L0A, Reset from TTCrx
  - Control via I2C interface
- **Read-Out (Off-Detector) Electronics**
  - 64 channels module
  - 8-bit 40MHz FADC (adj. Clock & Vref)
  - Synchronisation tasks
  - L1T preprocessing
  - L1B for L1T latency (1000 events)
  - Read-out & transmission after L1A
- **Processing Electronics**
  - DSP farm for zero-suppression
  - Read-out electronics monitoring



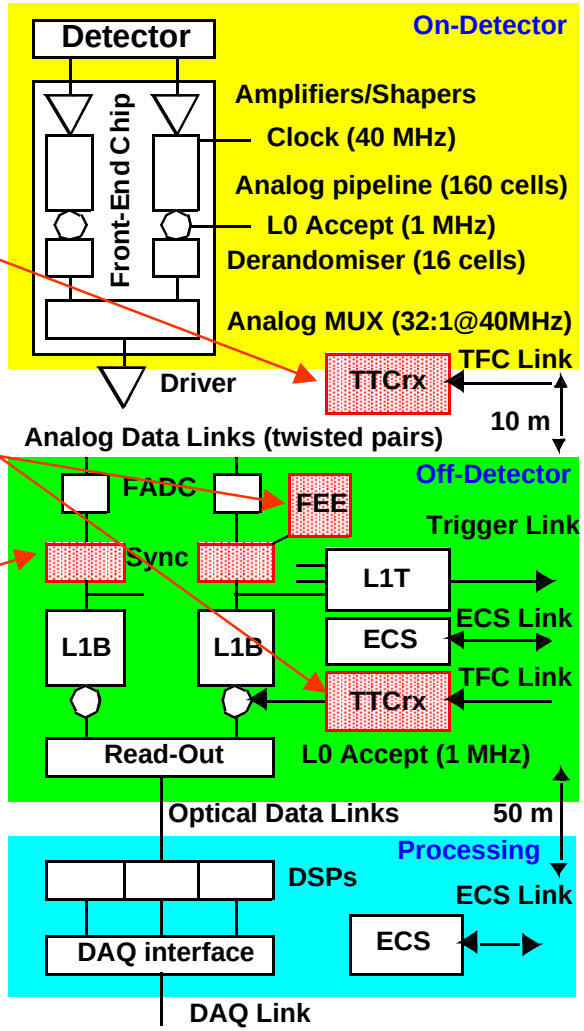
Synchronization Tasks

- **Sampling synchronization**
  - Clock phase adjustment
  - Set on signal model, adjuster on real
- **L0 Accept synchronization**
  - L0 Accept measurements
  - L0 Accept adjustment
- **Front-end data synchronization**
  - FE Emulator time prediction
  - FE data structure
- **Front-end error detection**
  - FE Event ID cross-check with ODE
- **L1 Accept synchronization**
  - Event ID + accept/reject
- **Event synchronization**
  - Additional DAQ event number



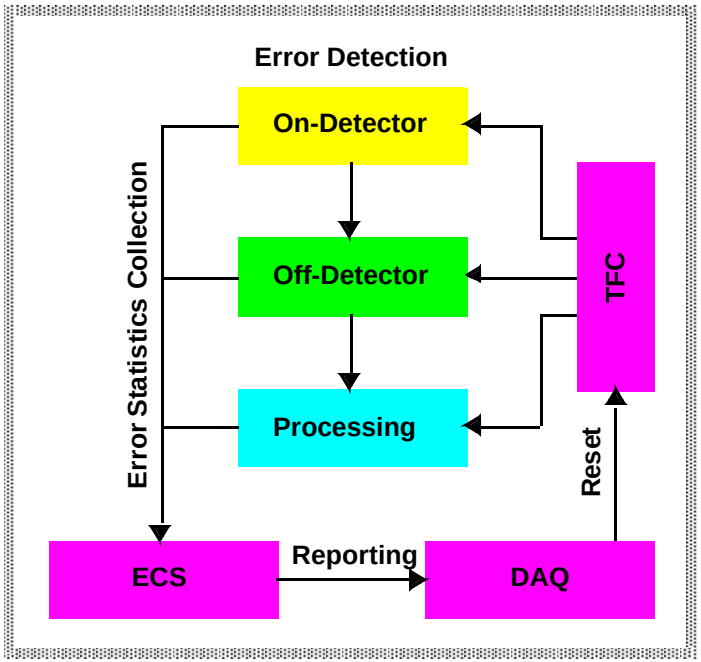
Synchronization Hardware

- **TTCrx receiver chip**
  - 0.1 ns clock adjustment
    - Detector signal sampling
    - FADC clock adjustment
  - 16 clock cycles L0 Accept delay
    - L0 Accept adjustment
  - Bunch-crossing ID, L0 and L1 Accepts
- **Emulator of the FE chip control logic**
  - Predict FE data arrival time
    - No need for separate strobe line
  - Generate FE pipeline ID for cross-check
    - FE chip error detection
  - Generate Event ID
- **Synchronization logic**
  - FE chip synchronization errors detection
    - Sets error flags for the L1 Buffer
    - Masks the data for the L1 Trigger
  - Event tagging in the L1 Buffer
  - L1 Accept synchronization
  - DAQ event number generation



Error Detection and Recovery

- Synchronization errors are detected at different locations in the VELO electronics
- Corrupted data are flagged or masked
- Error statistics are collected via the Experiment Control System (ECS) and reported to the DAQ
- The resetting frequency is calculated using observed error rate and different resetting scenarios are supported
- Resets are distributed to the VELO electronics using Timing and Fast Control system



Summary

- VErtex LOcator (VELO) is a vital part of the LHCb experiment and it's Level-1 trigger
  - Robustness is a major issue
- VELO electronics located in a harsh radiation environment
  - Errors are unavoidable
- Synchronization check and error detection must be performed along the data flow
  - Special hardware are included in the data flow
- Error recovery procedure involves periodical resets