The Serial Link Processor for the Fast TracKer (FTK) at ATLAS

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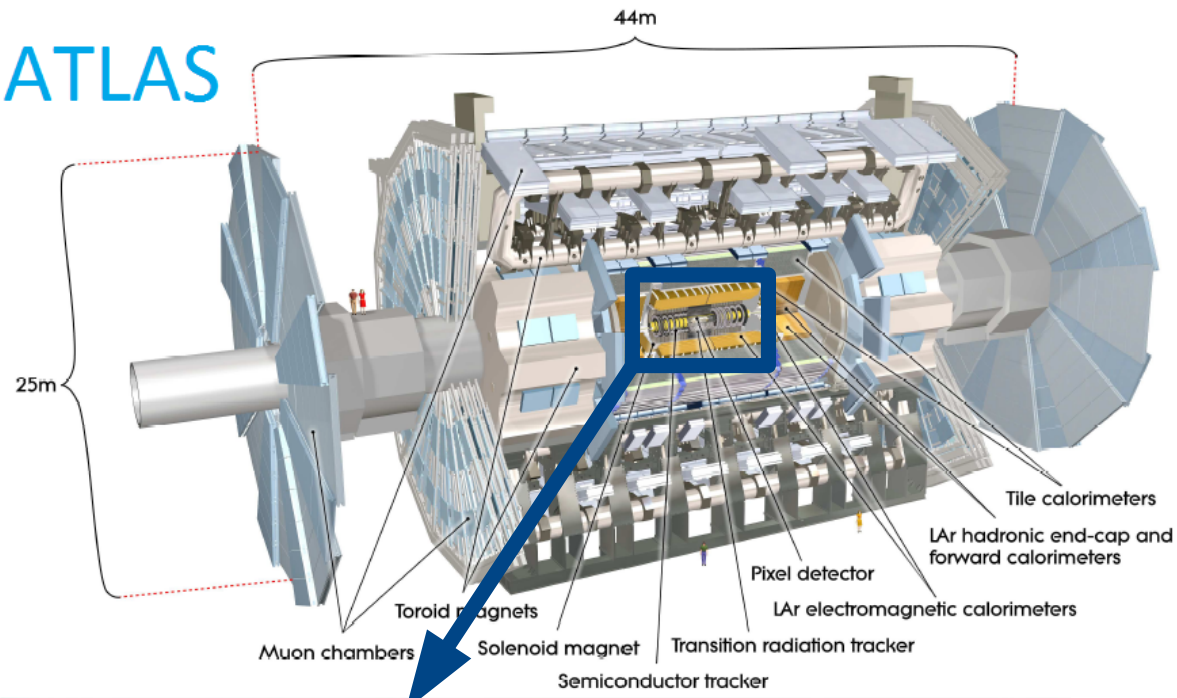
Outline

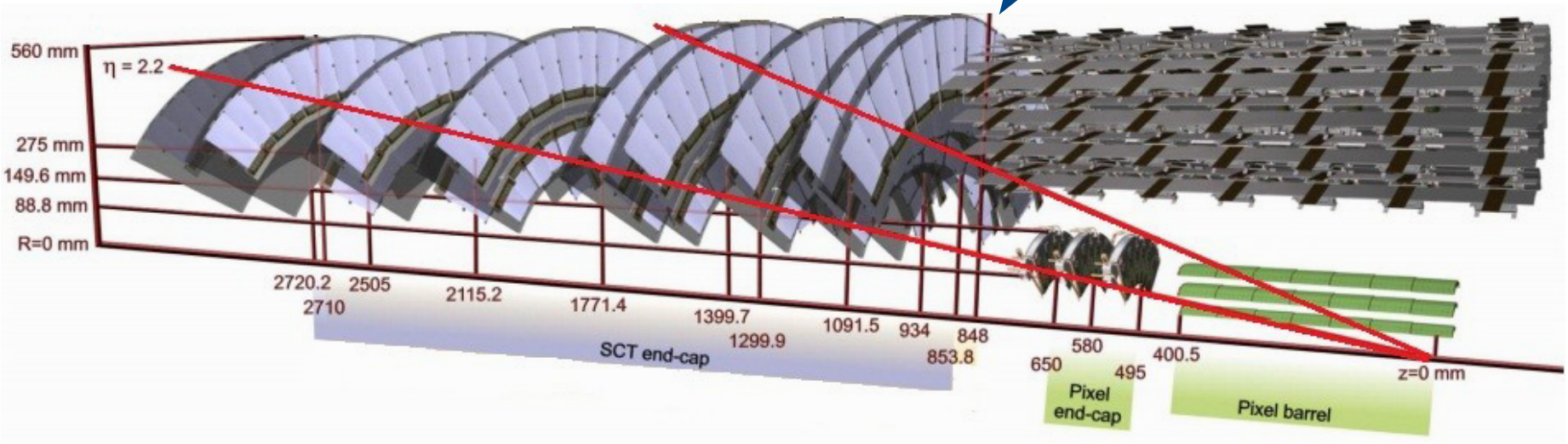
- Brief overview of ATLAS Tracking Detector.
- Where FTK is inserted in the baseline TDAQ.
- The FTK architecture and the Processing Unit.
- The Associative Memory chip.
- The boards to pack AMchips: AMBSLP and LAMBSLP.
- The tests of the integrated AM system.

FTK: the Online Silicon Detector Tracker for ATLAS upgrade

- FTK reconstructs charged particle trajectories in the silicon tracker (Pixel & SCT) at "1.5" trigger level.

- Extremely difficult task
  - 100 KHz input event rate
  - ~70 pile-up events at top luminosity.





An online silicon detector tracker for the ATLAS upgrade

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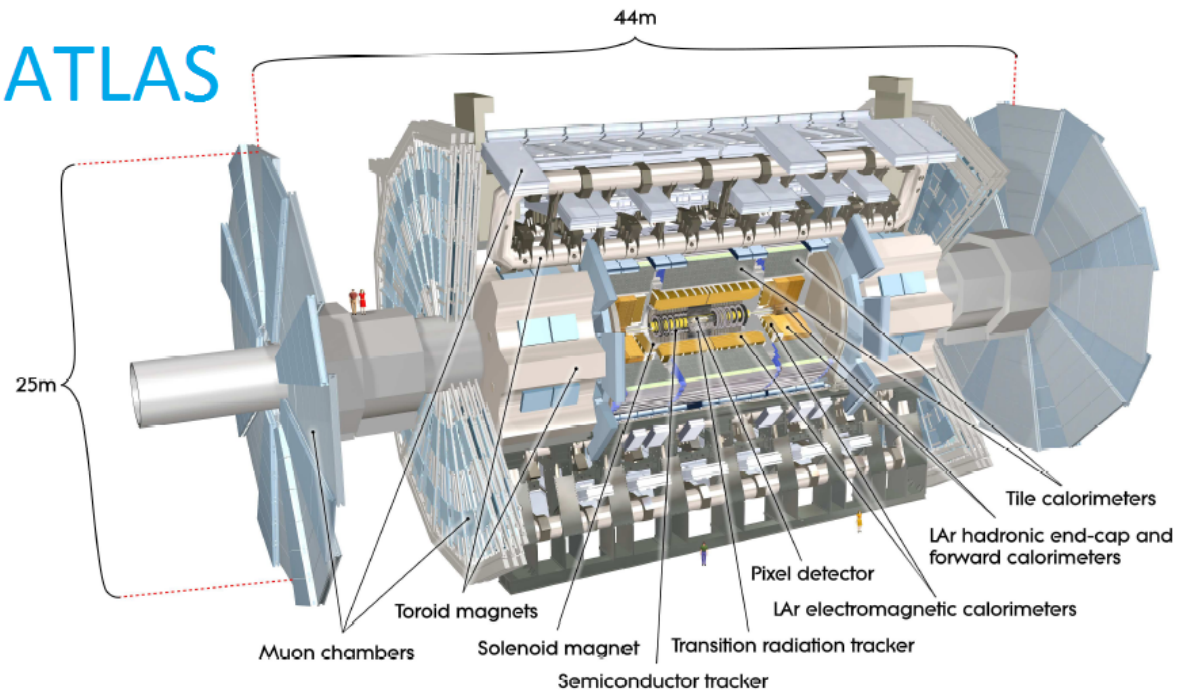
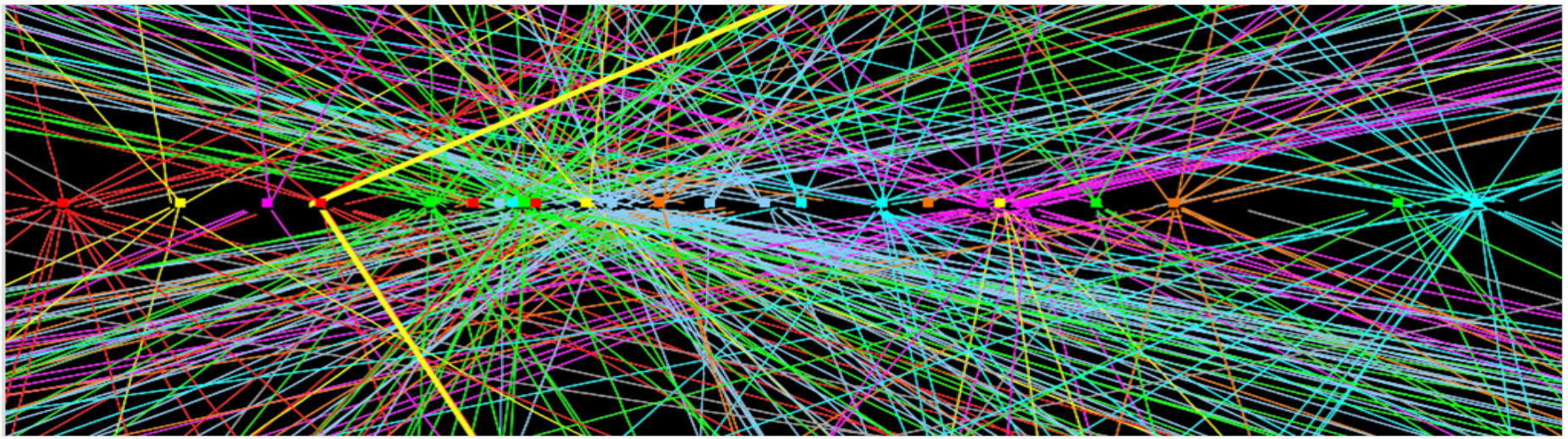
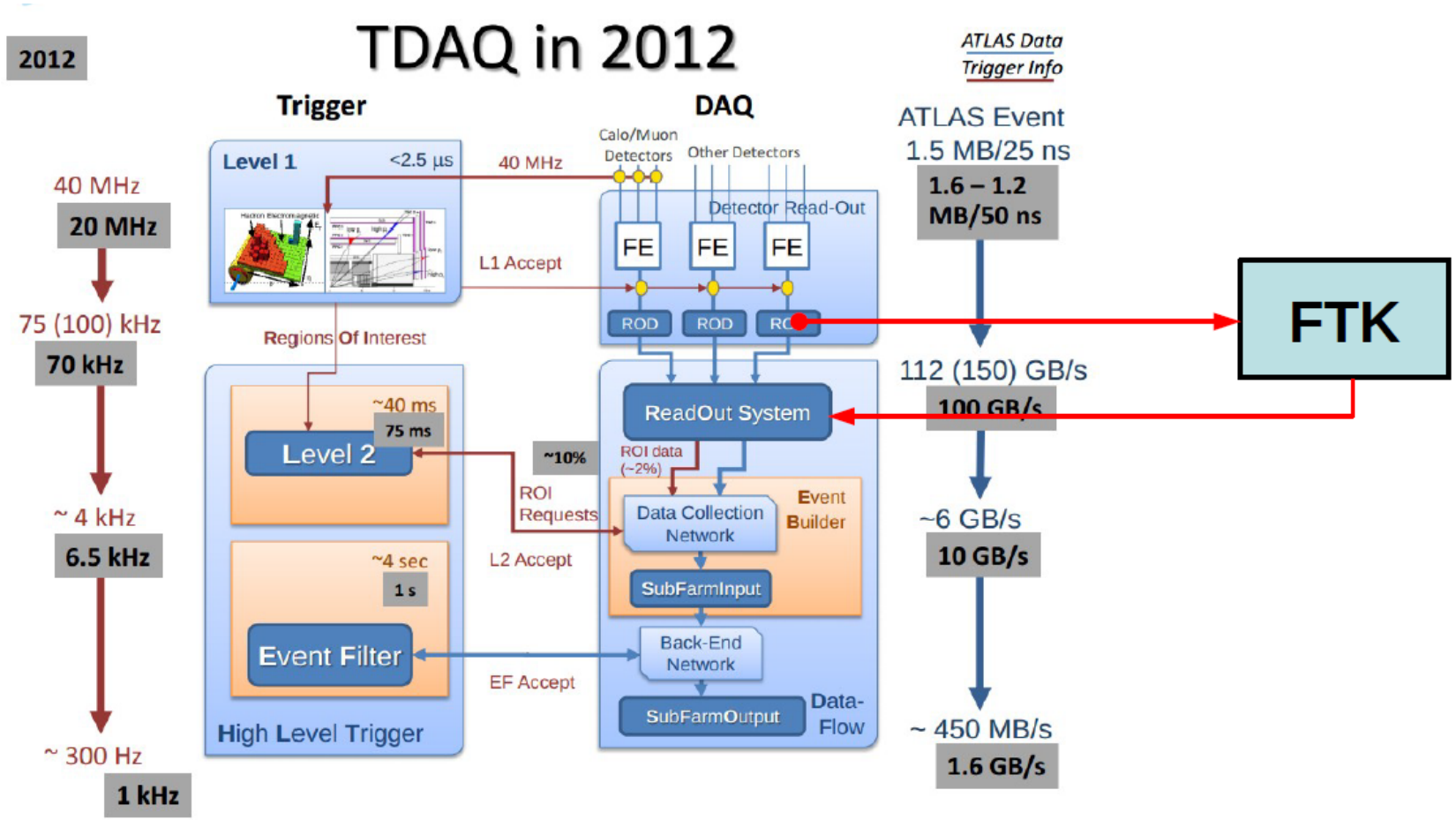




“1.5” Level Trigger processor



- Silicon data currently used only locally (ROI) and late in Level 2.
- FTK reconstructs all tracks with pT>1 GeV/c in time for Level 2.
- Track parameters are computed with full detector resolution.

FTK architecture

Follow Sotiropoulou's talk

Clustering

Data Formatter

ATCA

~380 ROLs
@2 Gb/s
100 GB/s

8x128 Slinks
@6Gb/s
~800 GB/s

Only here: 750 Slinks
~200 GB/s
Pattern Matching: ~25 TB/s

VME

Pattern Matching

Track Fitting

128 PU

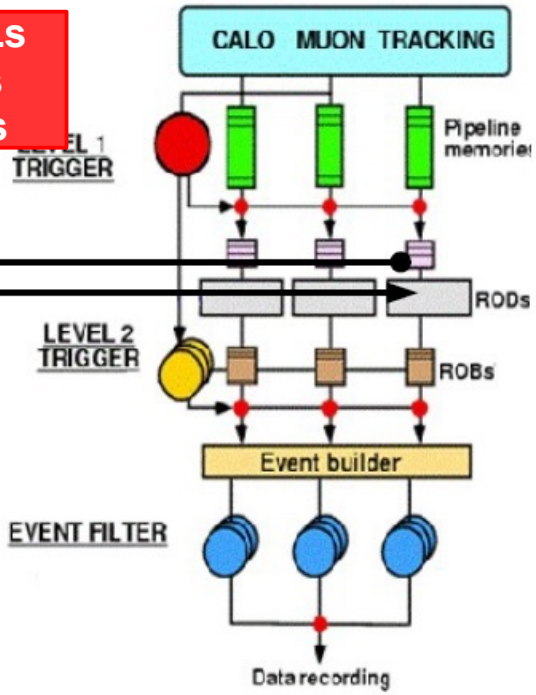
Processing Unit

Final Fitting

32 Boards

FTK to Level 2 Interface

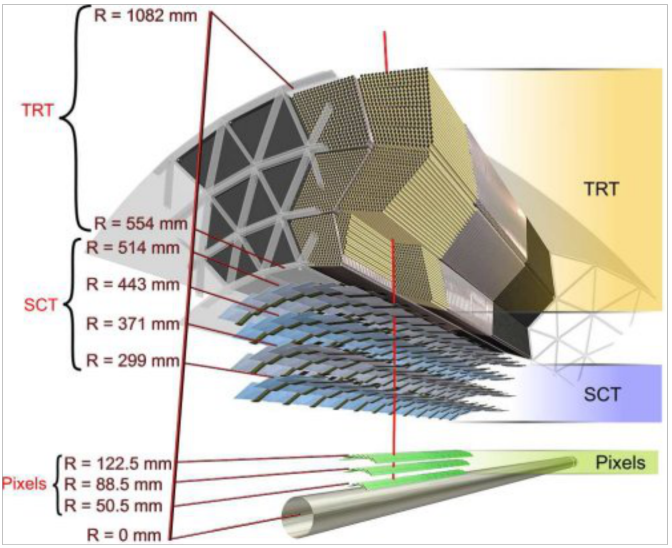
ATCA

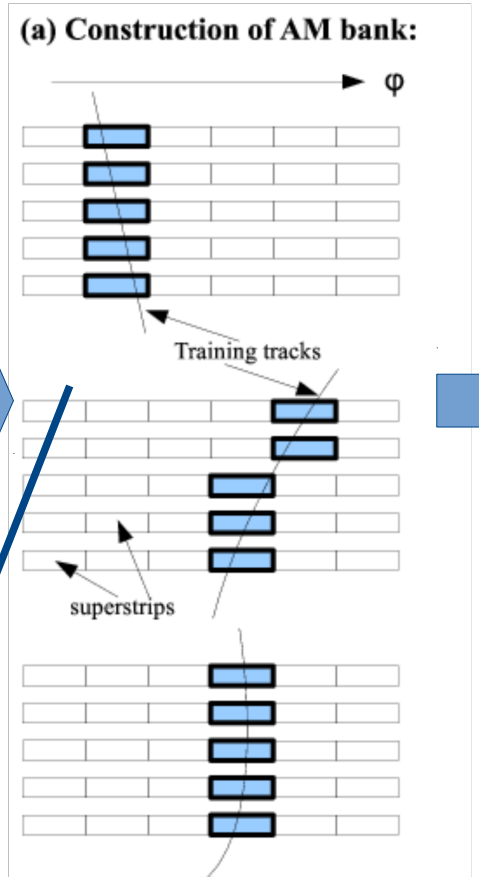


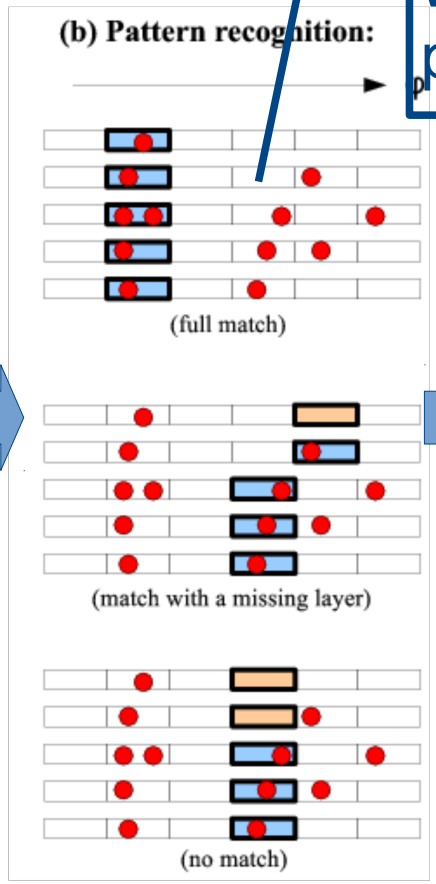
- 5 ATCA crates (HW clustering)
- 8 VME Crates:
  - 128 Processing Unit (track reconstruction)
- Total of ~1500 FPGAs, ~8200 AMChips

Processing Unit: Pattern Matching & Track Fitting

- The Processing Unit perform the track reconstruction algorithm in two sequential steps:
  →***Pattern Matching*** & Track Fitting.







The **input Hits** are compared with the pattern bank.

Roads: matched pattern

Definition of **pattern bank**: list of low resolution candidate tracks.

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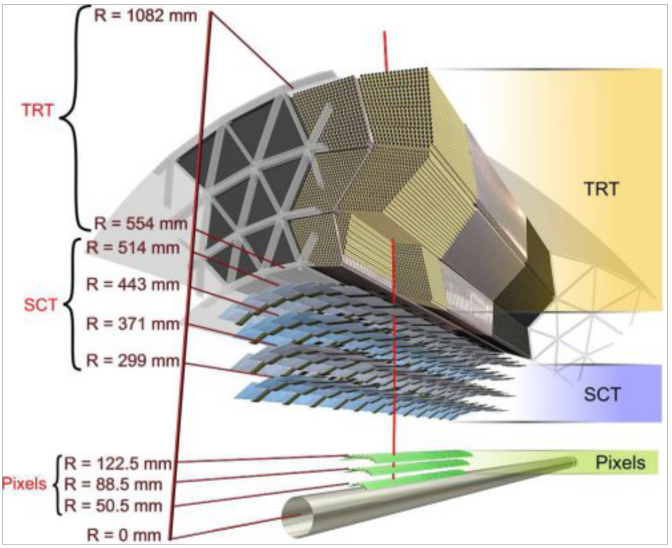
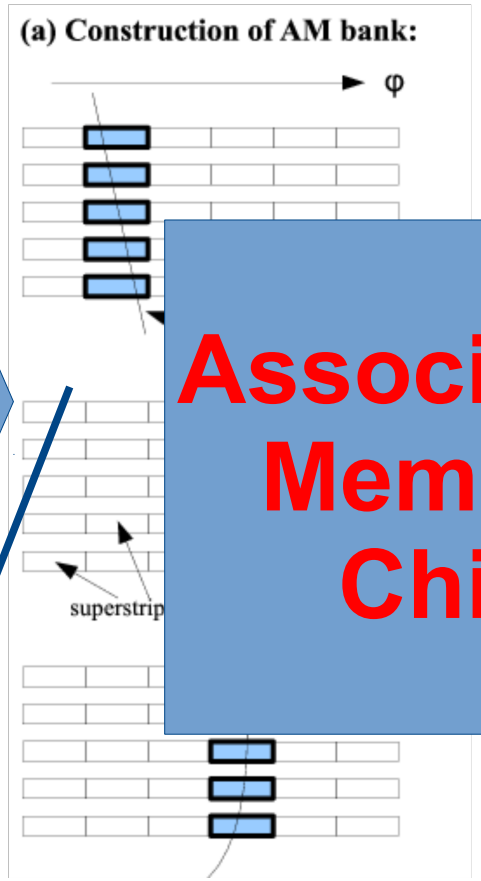
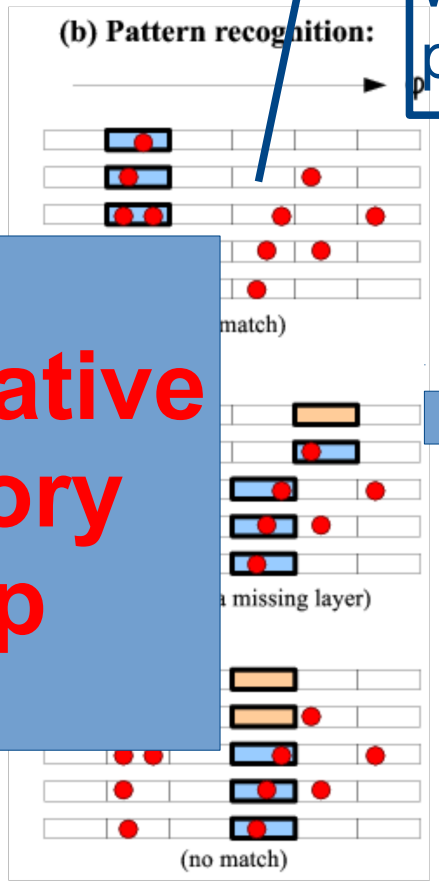






Associative Memory Chip

The **input Hits** are compared with the pattern bank.

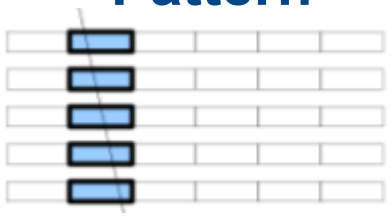
Roads: matched pattern

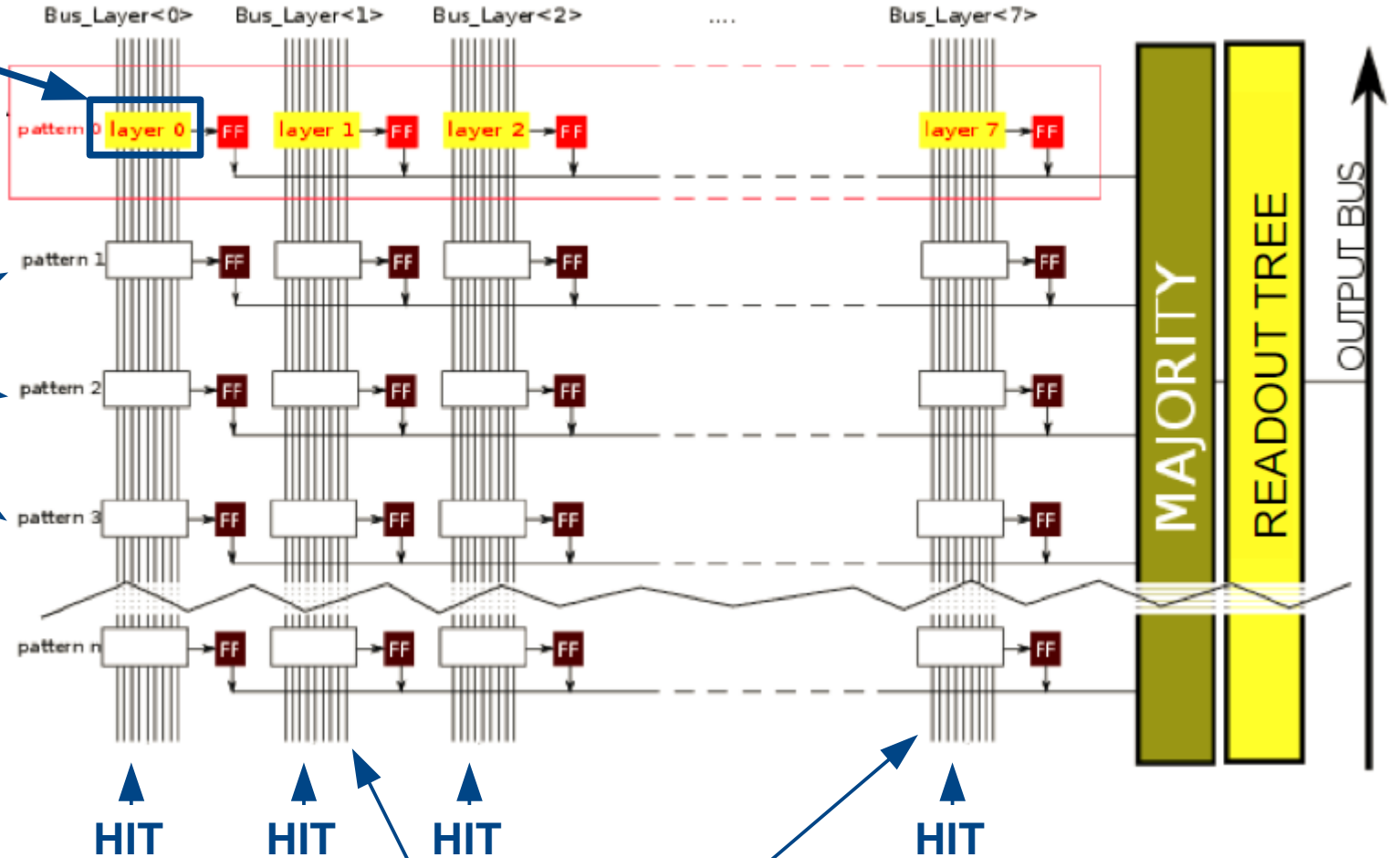
Definition of **pattern bank**: list of low resolution candidate tracks.

AM chip working principle

1 COMPARATOR Between the BUS & 1 stored 16-bits-WORD

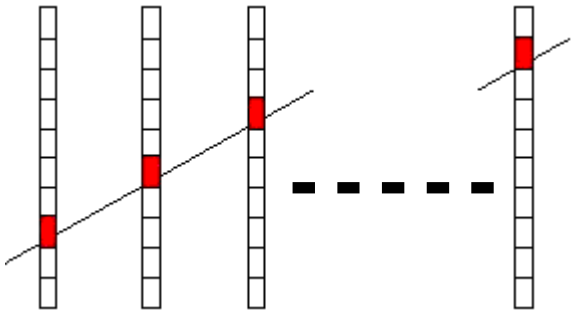
Pattern





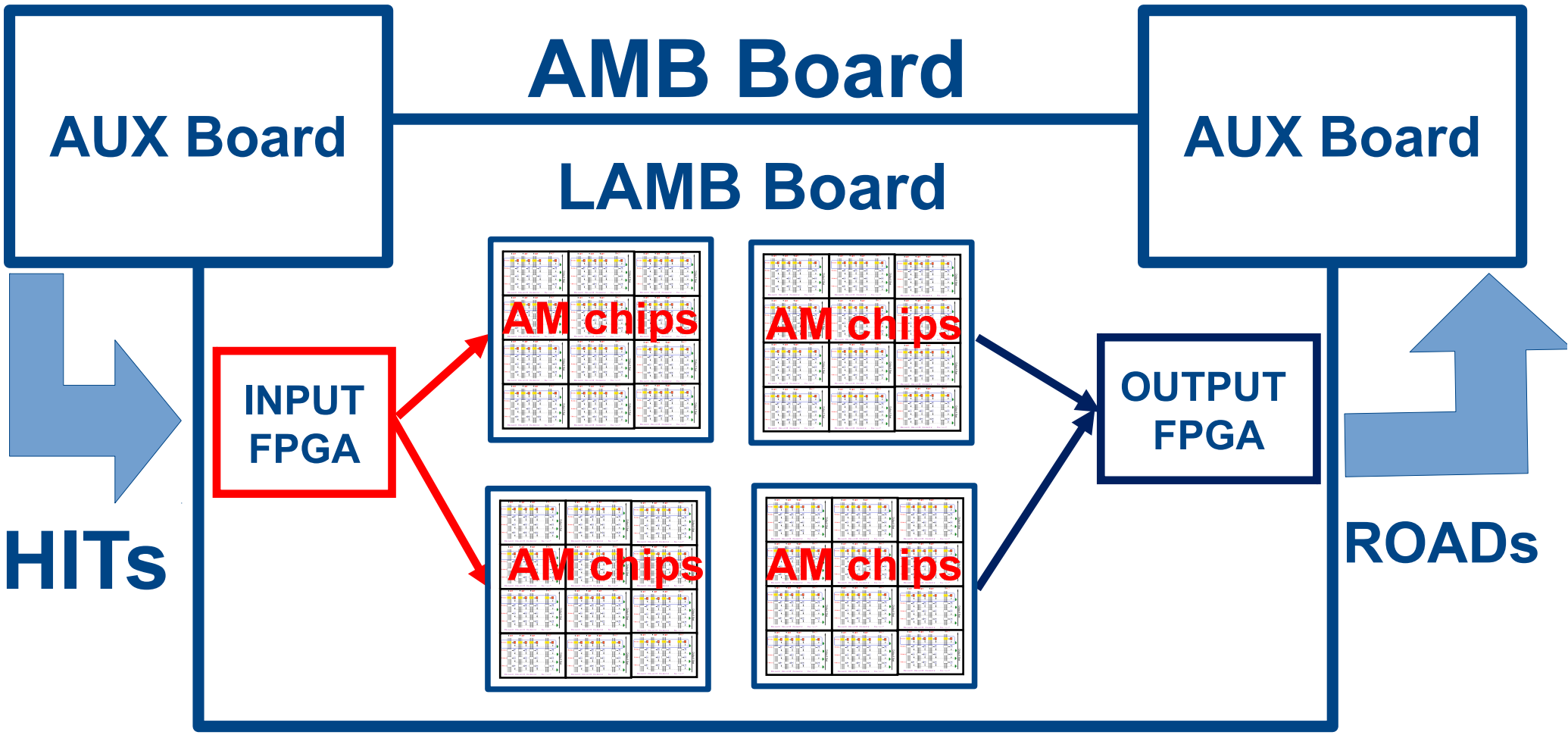
AM chip consumption:
~ 2.5 W for 128 kpatterns

AM computing power:
Each pattern:
4x32 bits comparators
Each 10 ns:
128 kpat x4 = 500 K instructions
→ 500 K x 100 M/s = 50×10^6 MIPs/CHIP
Only comparator instructions:
- 3.2×10^9 MIPs/AMB (64 chips)
- 4×10^{11} MIP in the whole AM system



AM Memory Accesses:
128 k x 4x32 bits x 100 M/s=
1.6×10^{15} accesses/s

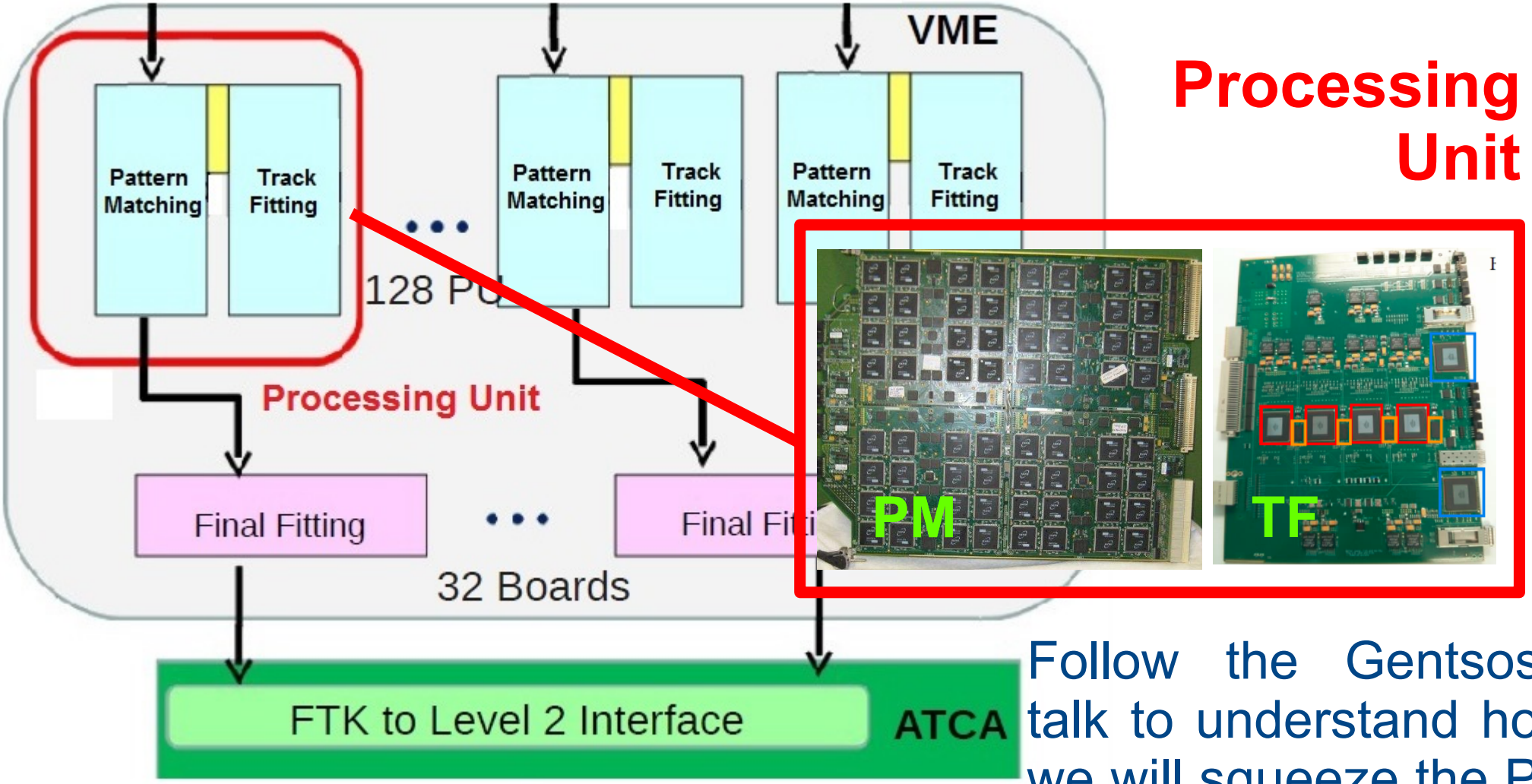
Associative Memory Board



- The **Input FPGA** distributes silicon **HITs** to the 4 **LAMBs.**

- The matched **ROADs** are collected from the **OUT FPGA.**

The Processing Unit architecture

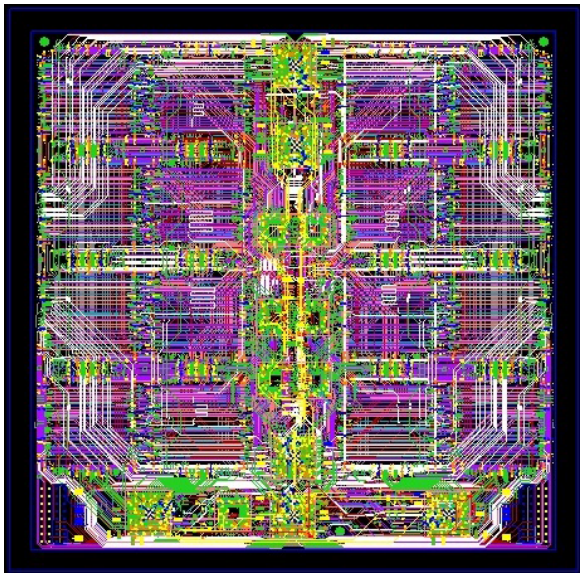


Follow the Gentsos's talk to understand how we will squeeze the PU different function in a single chip.

Recent developments of the Associative Memory chip

AM chip 04:

- Package: PQ208
- Parallel I/O interface
- 8k patterns
- Crazy routing of LAMB



More performance needed with the new AMChip06 (128 Kpatterns)

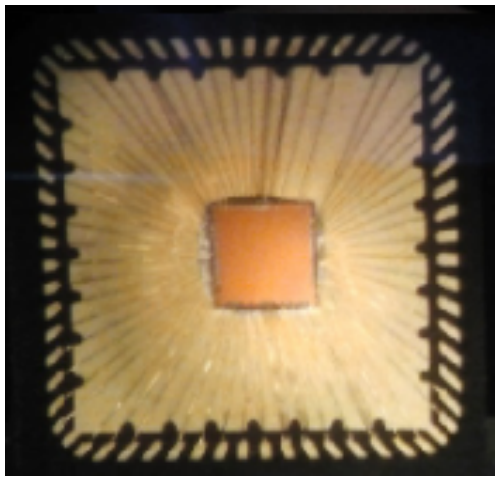
- Increase the number of pads.
- Use BGA package for more pins
- Simplify LAMB routing

Idea: **serial link** to transmit the data

Associative Memory Chip - Family 05

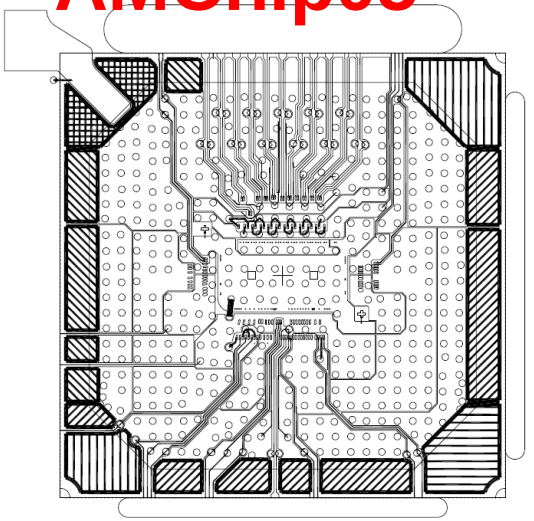
We bought a *IP-CORE* to provide the *chip* with serialisers and deserialisers.

MiniAMChip05



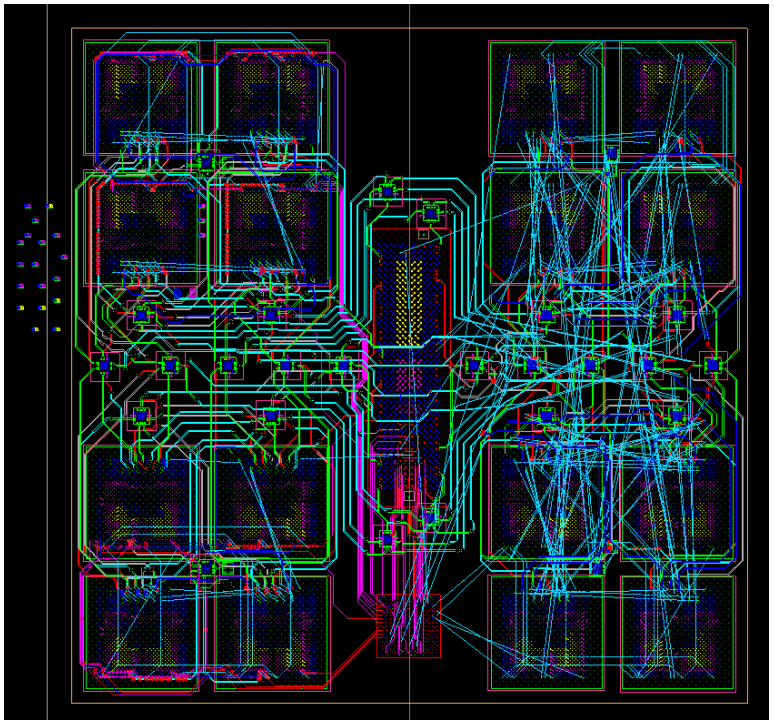
Package: QFN 64
Die: 3.7 mm^2
Board: MiniLAMB-SLP
Status: under test

AMChip05



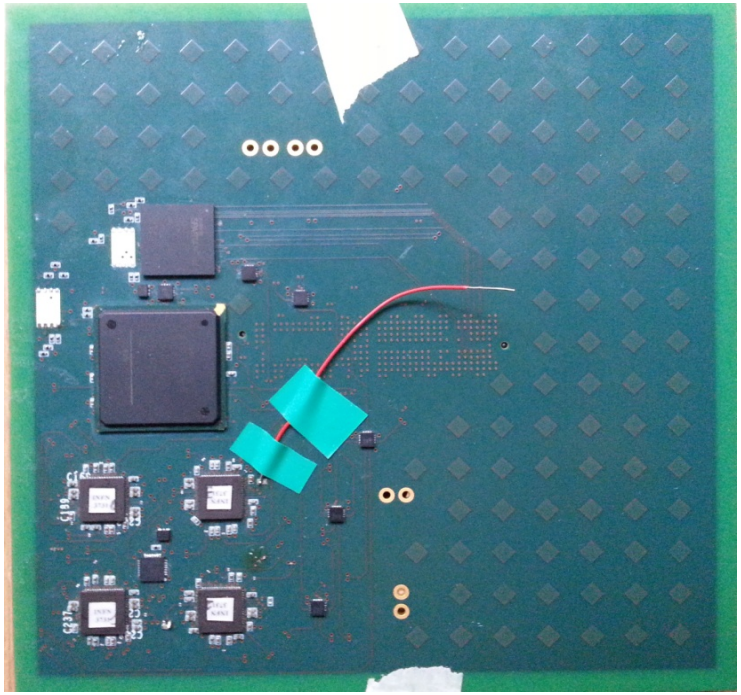
Package: BGA 23 x 23 mm
Die: 12 mm^2
Board: LAMB-SLP
Status: submitted

LAMB-SLP



- The final LAMB-SLP board will be ready in short time.
- In one LAMB-SLP board will have 16 Amchips.
  → for a total of ~2 M of **patterns**
- The routing is simplified.

- This is a prototype of **LAMB-SLP** board with 4 **MiniAM05 chips**.
  → This board is important to confirm our idea and our solution on **Serial Link**.



MiniLAMB-SLP & LAMB-SLP

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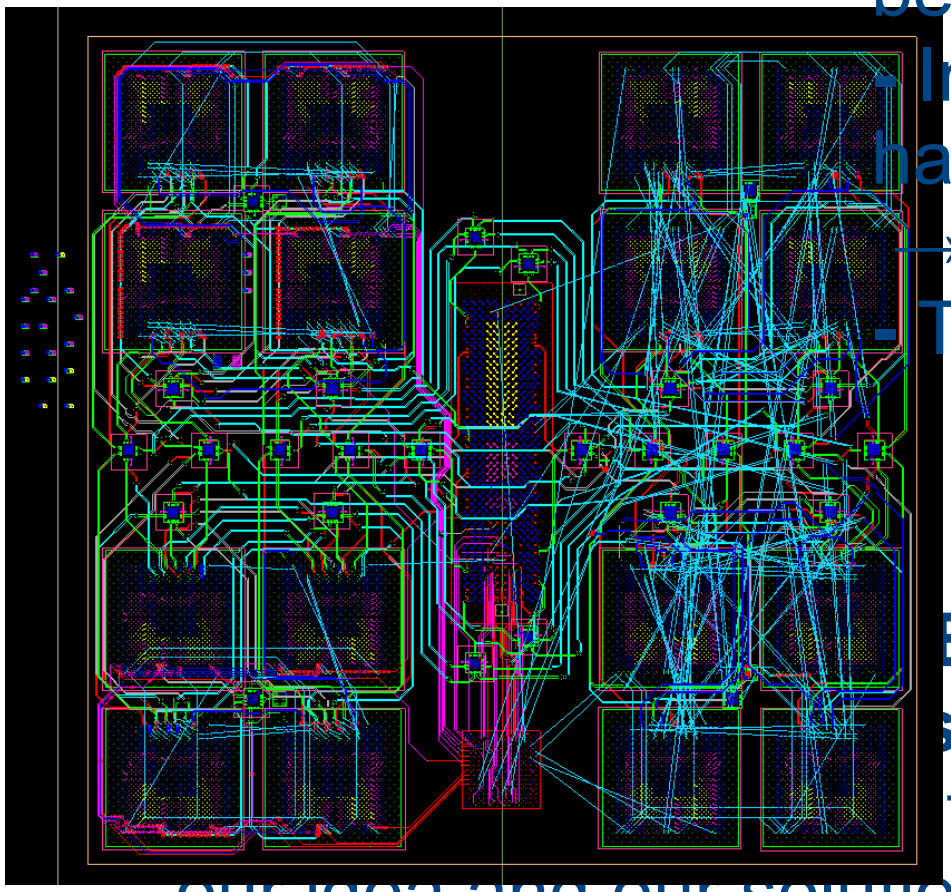

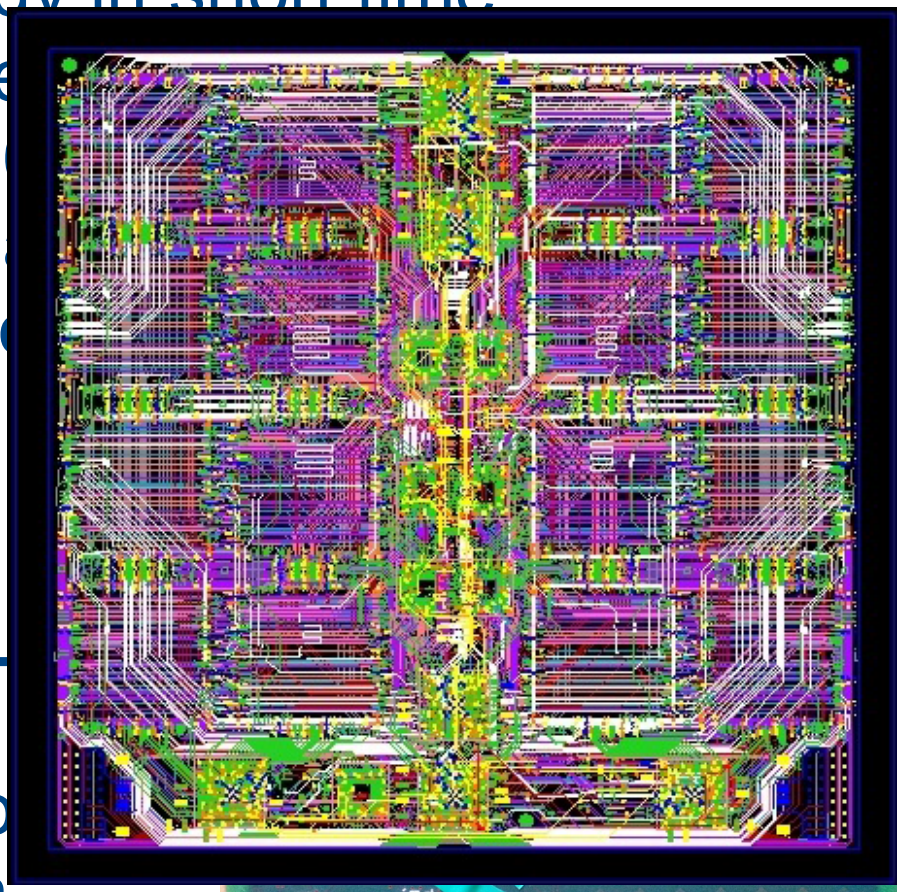

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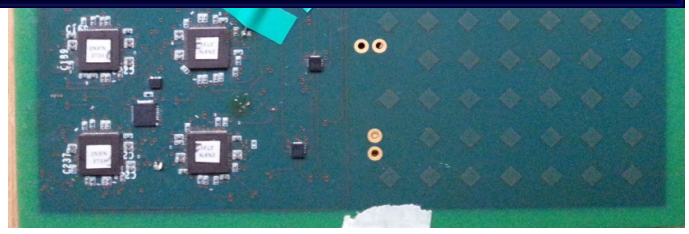
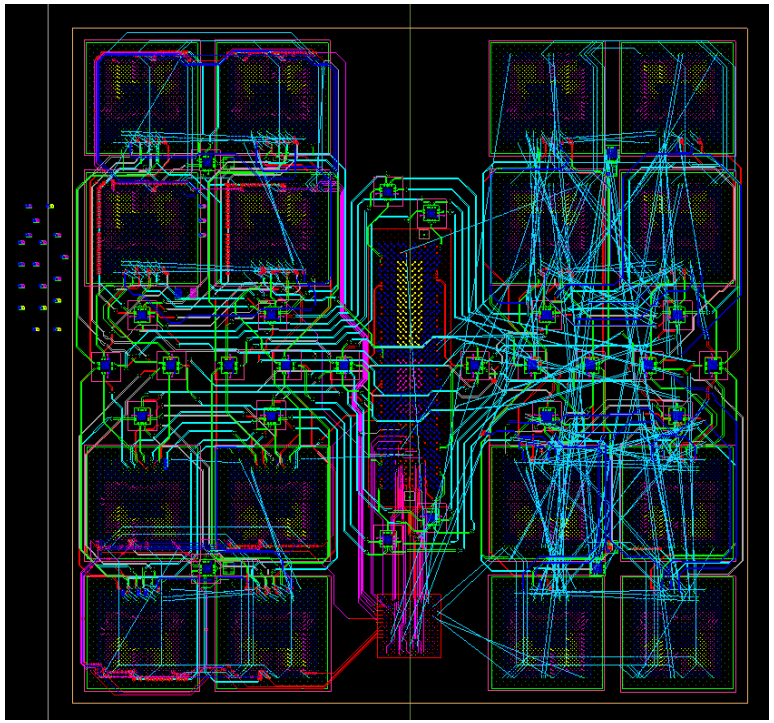


MiniLAMB-SLP & LAMB-SLP



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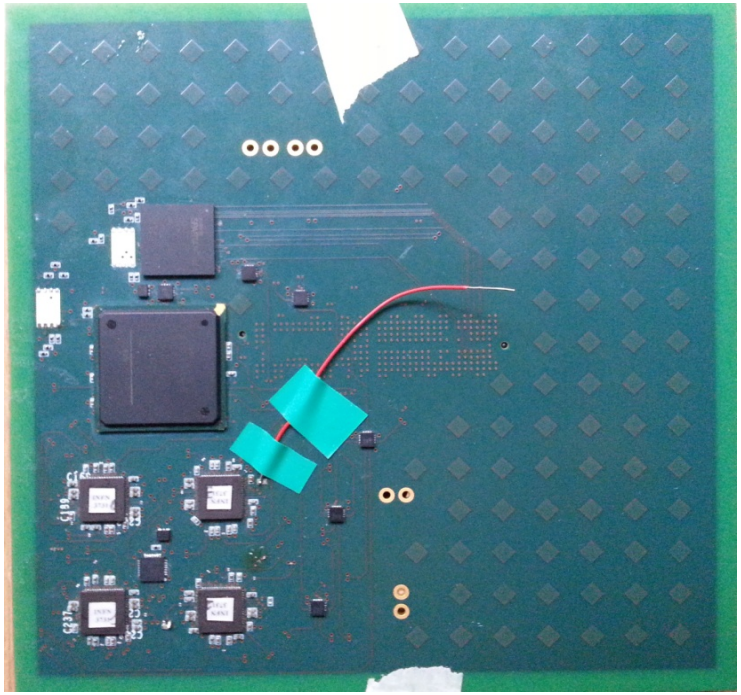
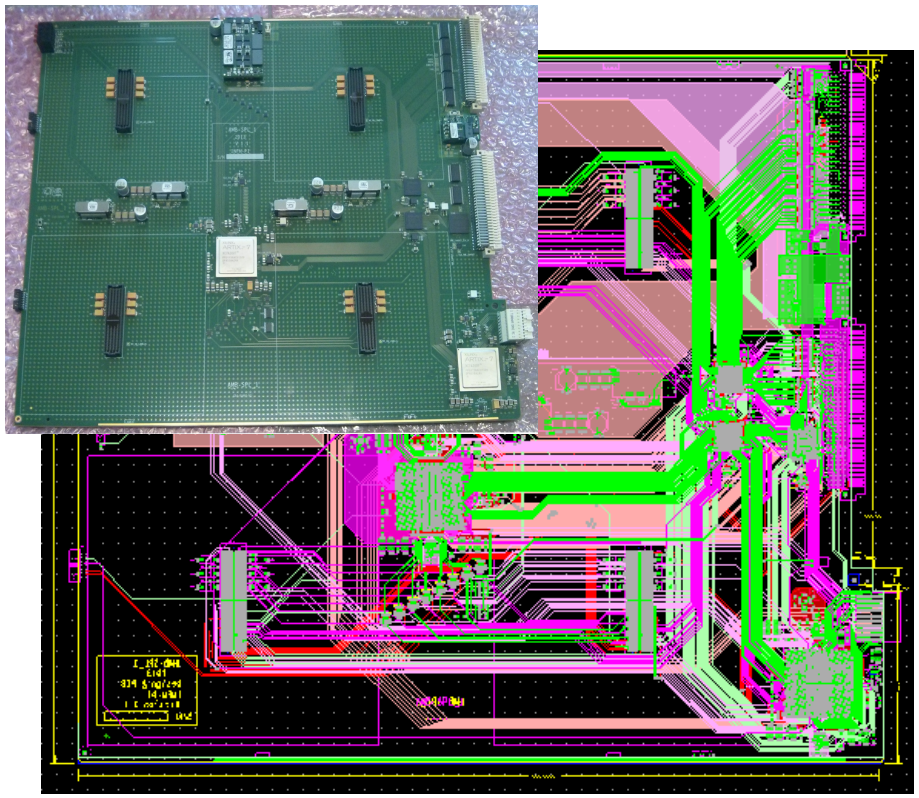


AMB-SLP board

The **AMBSLP** (Serial Link Processor) board design:



Interface:

- 12 input buses @ 24Gbps
- 16 output buses @ 32Gpbs

Three FPGA:

- 1 for the input data distribution (ARTIX-7)
- 1 for the output data distribution (ARTIX-7)
- 1 FPGA for the data control logic (SPARTAN 6)

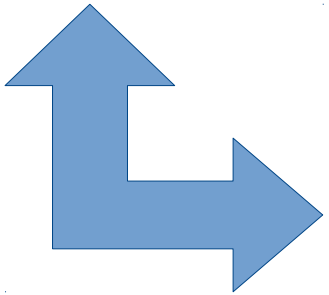
We used only serial standard for data distribution to and from the AM chips

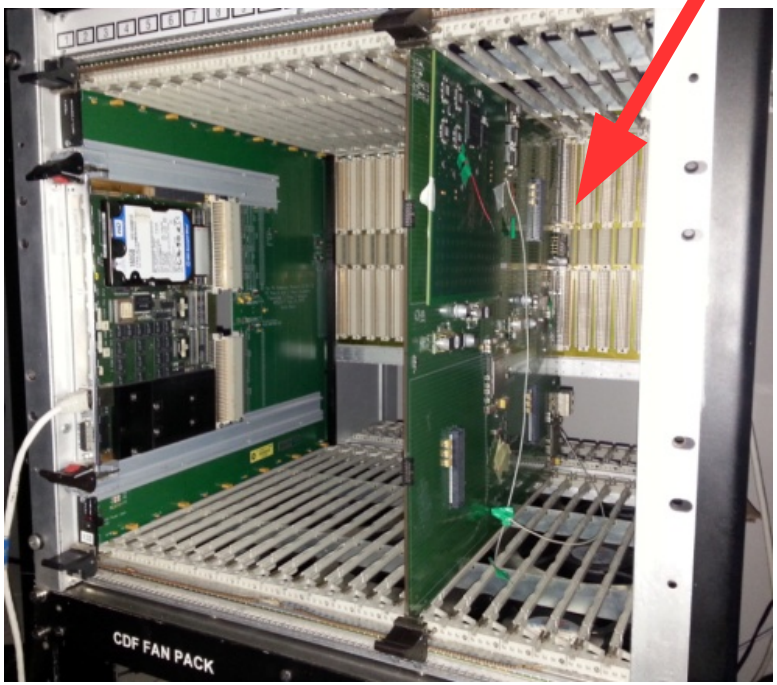
Test Stand

Complete test with:

- **AMB-SLP** board.
- **MiniLAMB-SLP** board.
- **MiniAMchip05**
- Crate VME.

Strobe

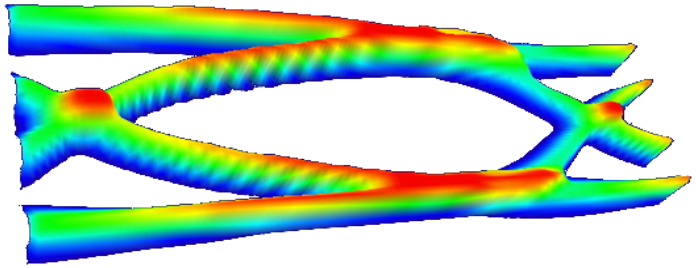




- We perform a Serial Link's test with a **PRBS Generator**.
- We used a **IBERT** core in Xilinx's ISE.

Serial Links

Both input and output serial links characterized for signal integrity.



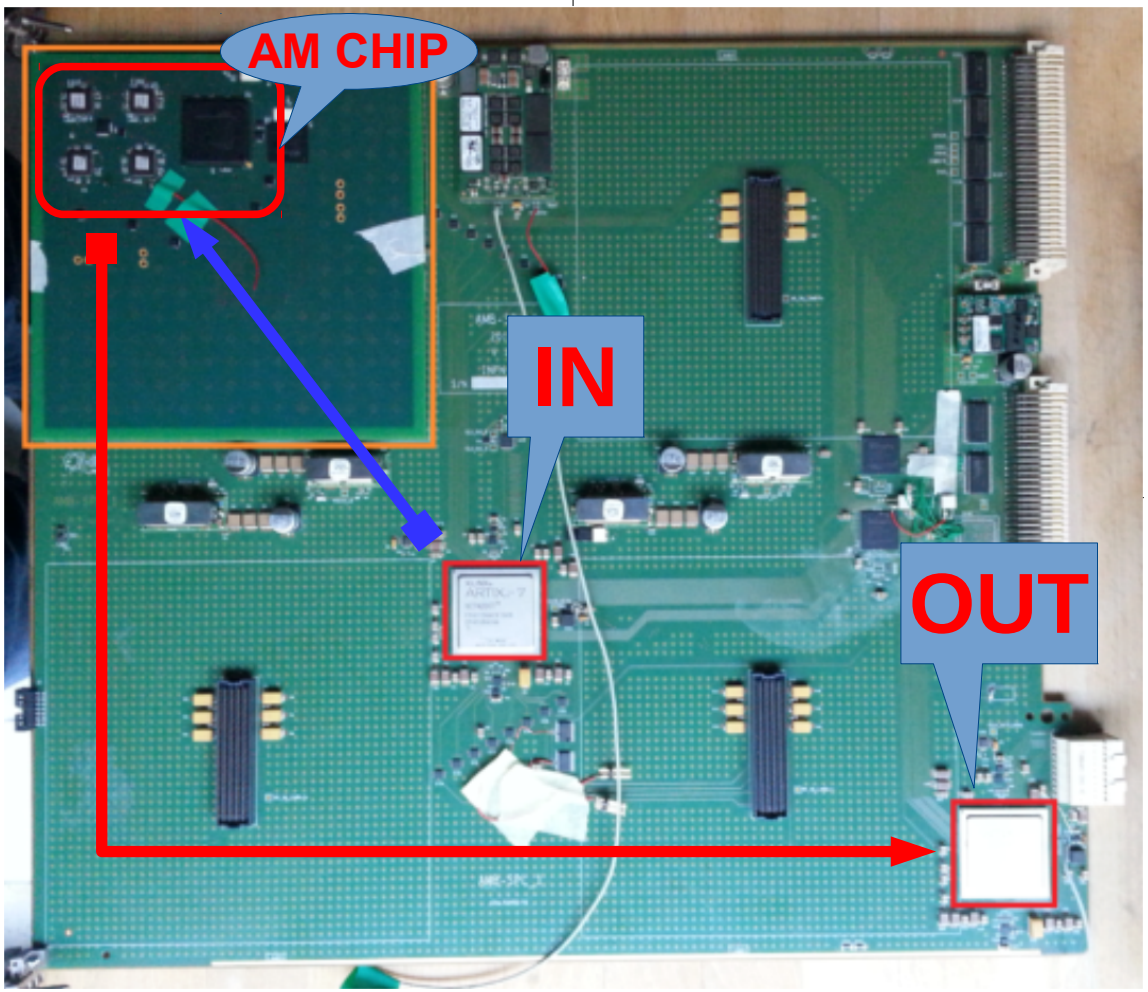
- Serial Link @ 2 Gb/s

→ Input path

- FPGA to FANOUT to AM Chip
- Intermediate buffers

→ Output path

- AM Chip to FPGA
- Intermediate repeater

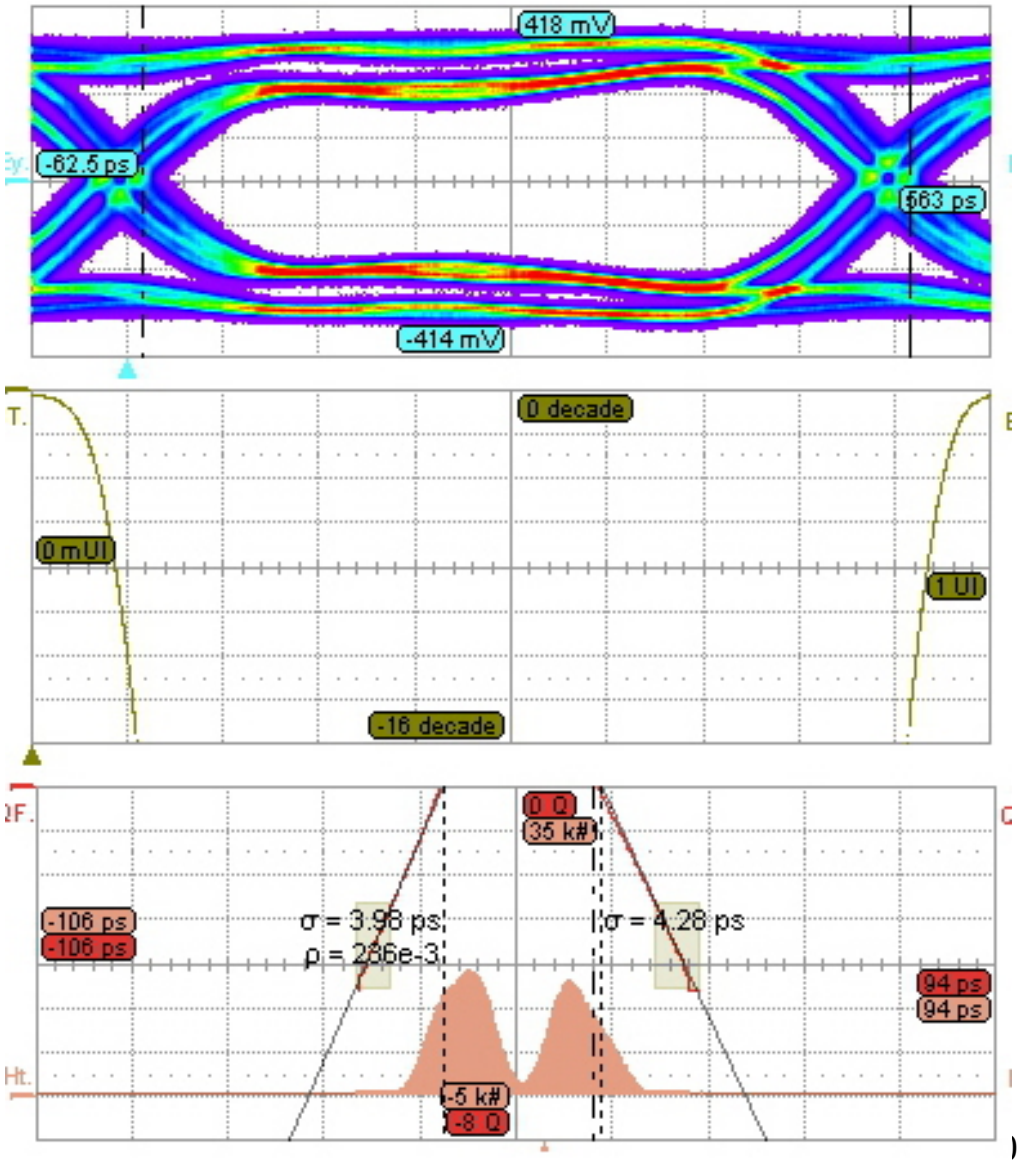


Result

- Types of measure:
  - Eye diagram
  - Jitter Analysis
  - BER

- Send **PRBS** data and check with **PRBS** checker:

BER < 10^{-14}



Conclusion

- FTK has a very large computing power and complex I/O network.
- The new AMchip serialized I/O simplifies substantially the board designs, AMBSLP and LAMBSLP.
- The AMBSLP and LAMBSLP contains hundreds of 2Gb/s serial links for a total traffic of 200 GB/s.
- The tests of the integrated AM system is successful and the performances are as expected.

Thank You!!