



# PROMETEO: A PORTABLE TEST-BENCH FOR THE UPGRADED FRONT-END ELECTRONICS OF THE ATLAS TILE CALORIMETER



D.BULLOCK<sup>A</sup>, F.CARRIO<sup>B</sup>, I.HOFSAJER<sup>C</sup>, M.GOVENDER<sup>C</sup>, B.MELLADO<sup>C</sup>, P.MORENO<sup>B,C</sup>, R.REED<sup>C</sup>, X.RUAN<sup>C</sup>, C.SANDROCK<sup>C</sup>, C.SOLANS<sup>D</sup>, R.SUTER<sup>C</sup>, G.USAI<sup>A</sup>, A.VALERO<sup>B</sup> {<sup>A</sup>UTA, <sup>B</sup>VALENCIA, <sup>C</sup>WITS, <sup>D</sup>CERN},

ON BEHALF OF THE ATLAS TILE CALORIMETER SYSTEM

## INTRODUCTION

Prometeo is the portable test-bench for the full certification of the front-end electronics of the ATLAS Tile calorimeter designed for the upgrade phase-II. The design inherits features from the presently-used MobiDICK4<sup>1</sup> test-bench.

Prometeo must:

- analyze data from 12 PMTs at the LHC bunch crossing frequency
- assess the quality of the data in real-time and diagnose malfunctions
- be self-contained and portable for maintenance inside the detector
- be low-cost and scalable for network usage

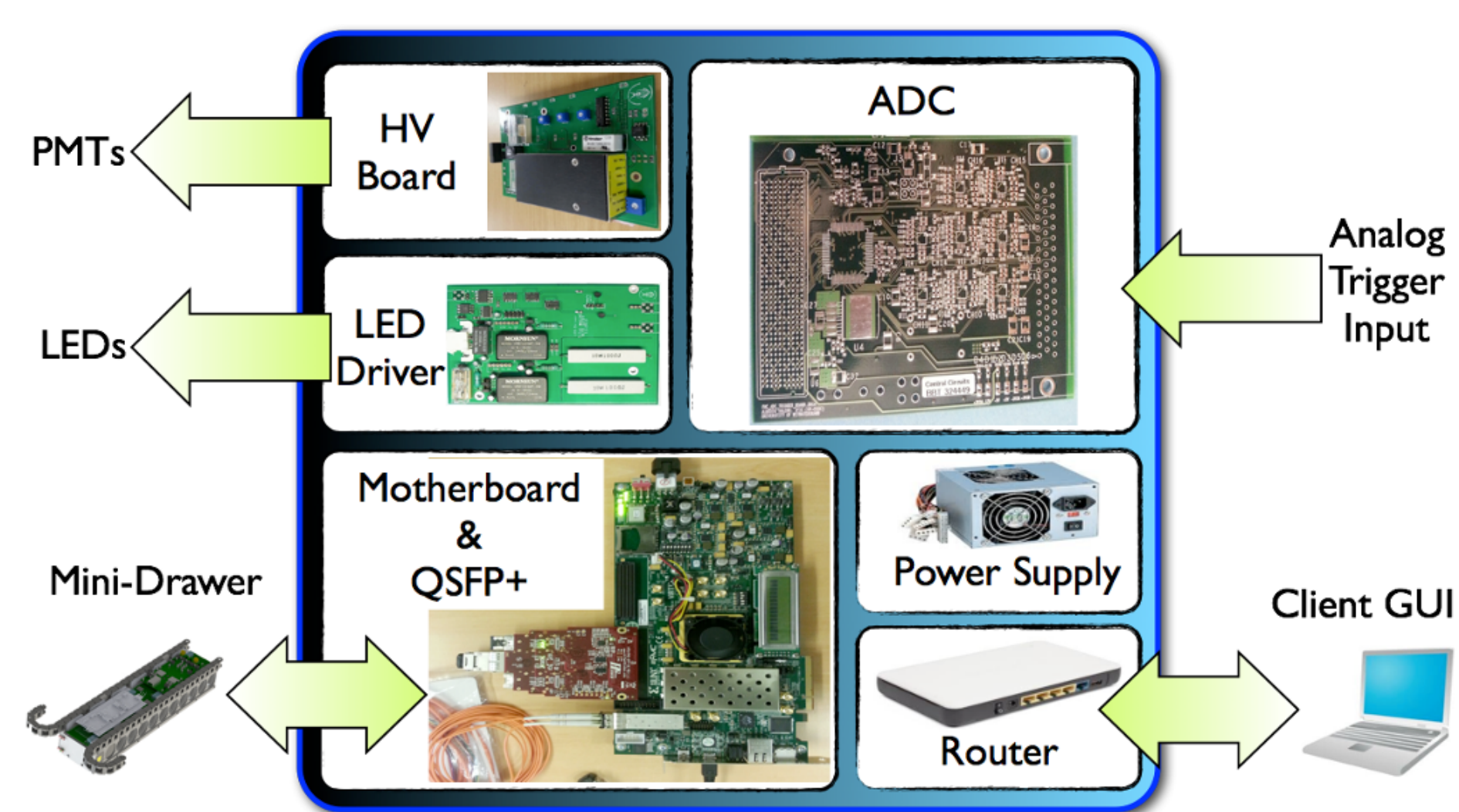


Figure 1: Prometeo block diagram

## PHASE-II UPGRADE

The HL-LHC upgrade is planned for LS3 (~2024). This upgrade represents a major replacement of both on- and off-detector electronics to facilitate several requirements on the future of the detector:

- improved radiation tolerance
- smaller independent modules to reduce consequences of malfunctions
- an increase in the number of links with the front-end electronics (point-to-point)
- a digital trigger for precise measurements
- higher read-out bandwidth (165 Gb/s → 40 Tb/s ; 80 Tb/s with redundancy)
- higher  $\sqrt{s}$  energy, luminosity, and more pileup
- more data by several orders of magnitude

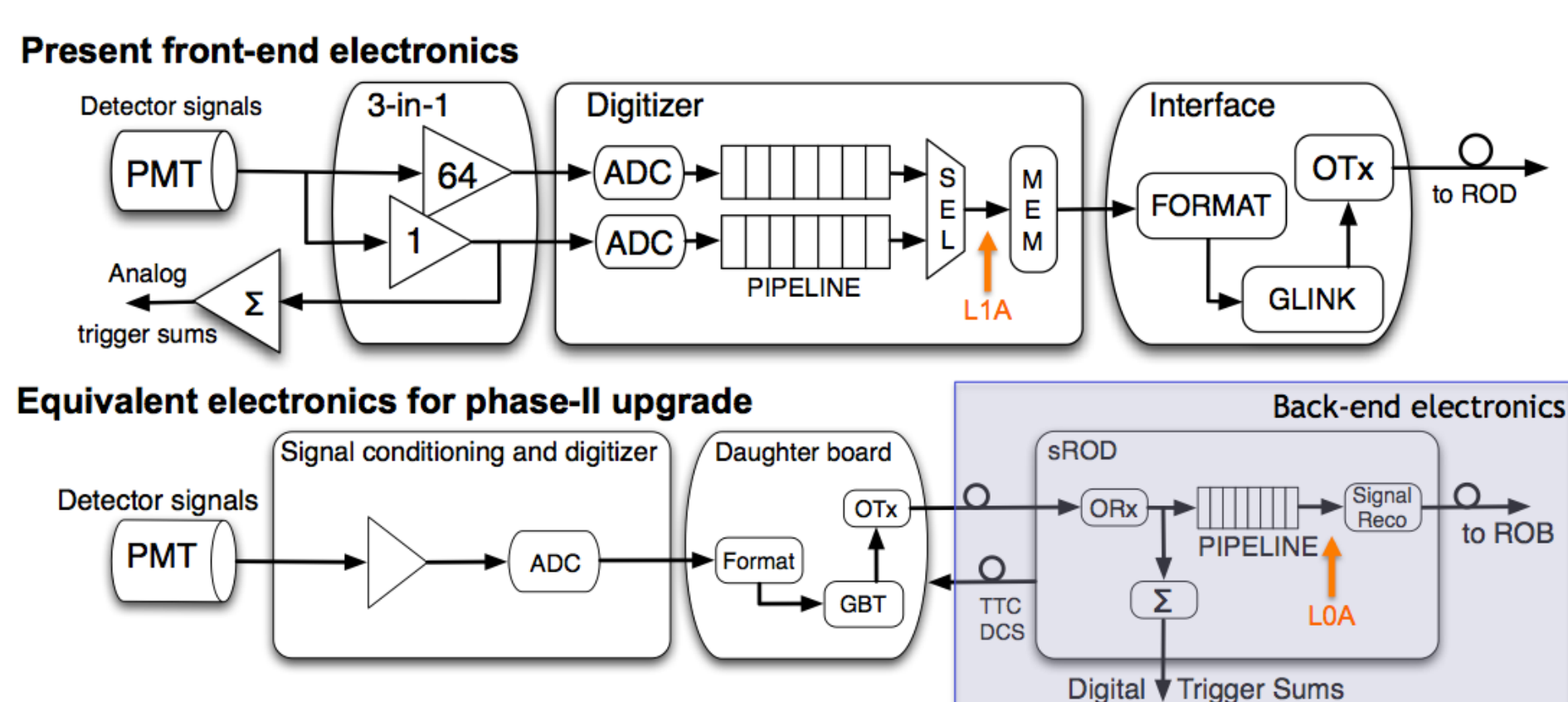


Figure 5: Phase-II upgrade

## REFERENCE

[1] Design of an FPGA-based embedded system for the ATLAS Tile Calorimeter front-end electronics test-bench, F.Carrío, H.Y.Kim, P.Moreno, R.Reed, C.Sandrock, A.Shalyugin, V.Schettino, J.Souza, C.Solans, G.Usai, A.Valero, ATL-TILECAL-PROC-2013-017, Nov 2013.

## MOTHERBOARD

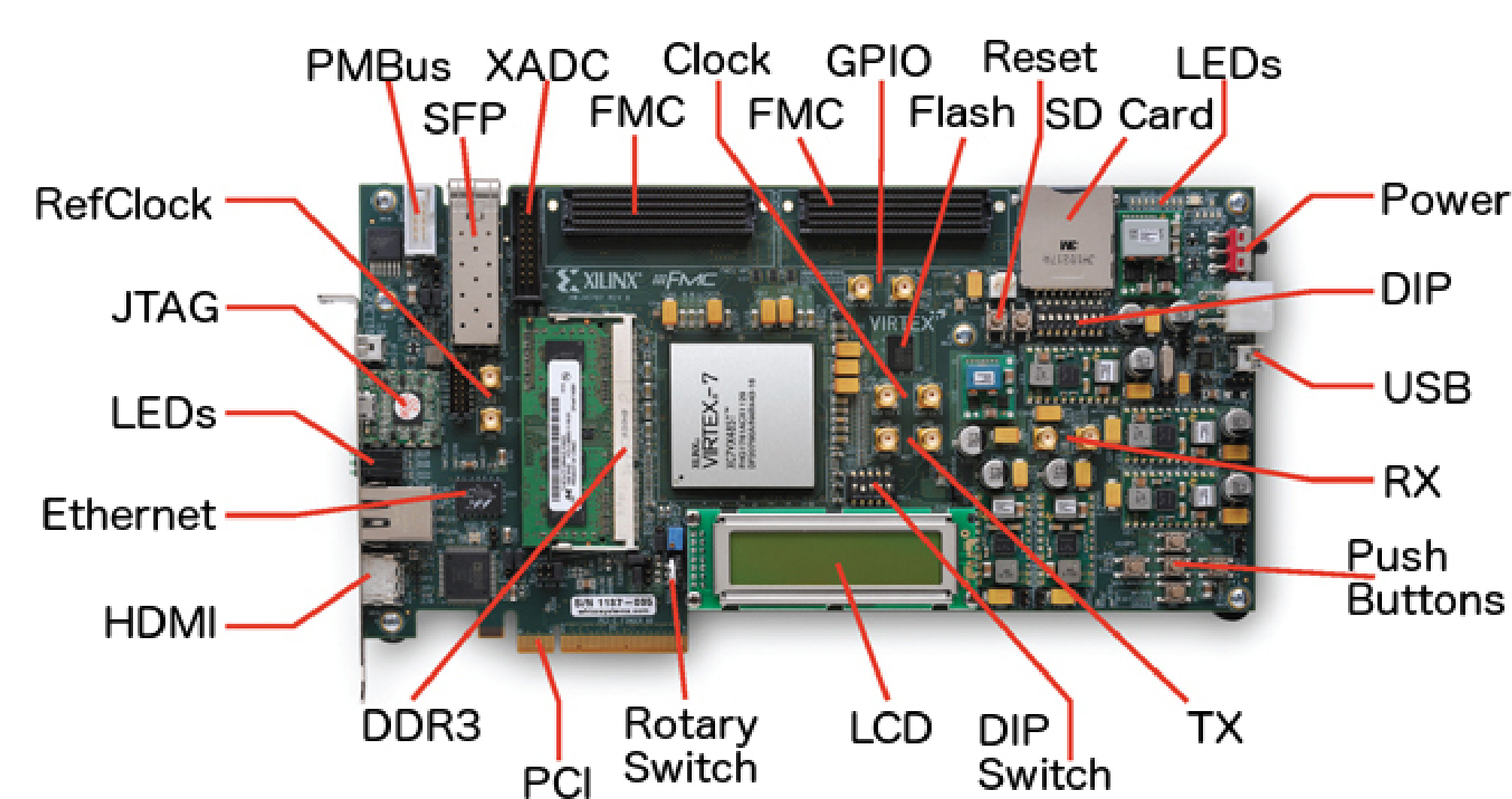


Figure 2: VC707

The core of the system is a Xilinx Virtex7 VC707 evaluation board with a XC7VX485T-2FFG1761 FPGA and extended with a dual QSFP+ FMC module (model HTG-FMC-X2QSFP+) to read-out and control the front-end boards. An on-board flash contains an IPbus protocol to read and write values directly to memory. This implementation bypasses the need for an on-board operating system and has been adapted from the CMS IPbus suite to streamline its performance.

## COMMUNICATION

A bi-directional optical transceiver module in QSFP+ format is used for digital communication with each mini-drawer daughterboard. One cable latch connects the receiver section (RX) and another connects the transmitter section (TX). An ethernet port allows the user to communicate with Prometeo over a network to a client platform. The IPbus latency motivates the need to keep a low profile on network communication for scalability during regular maintenance in ATLAS.

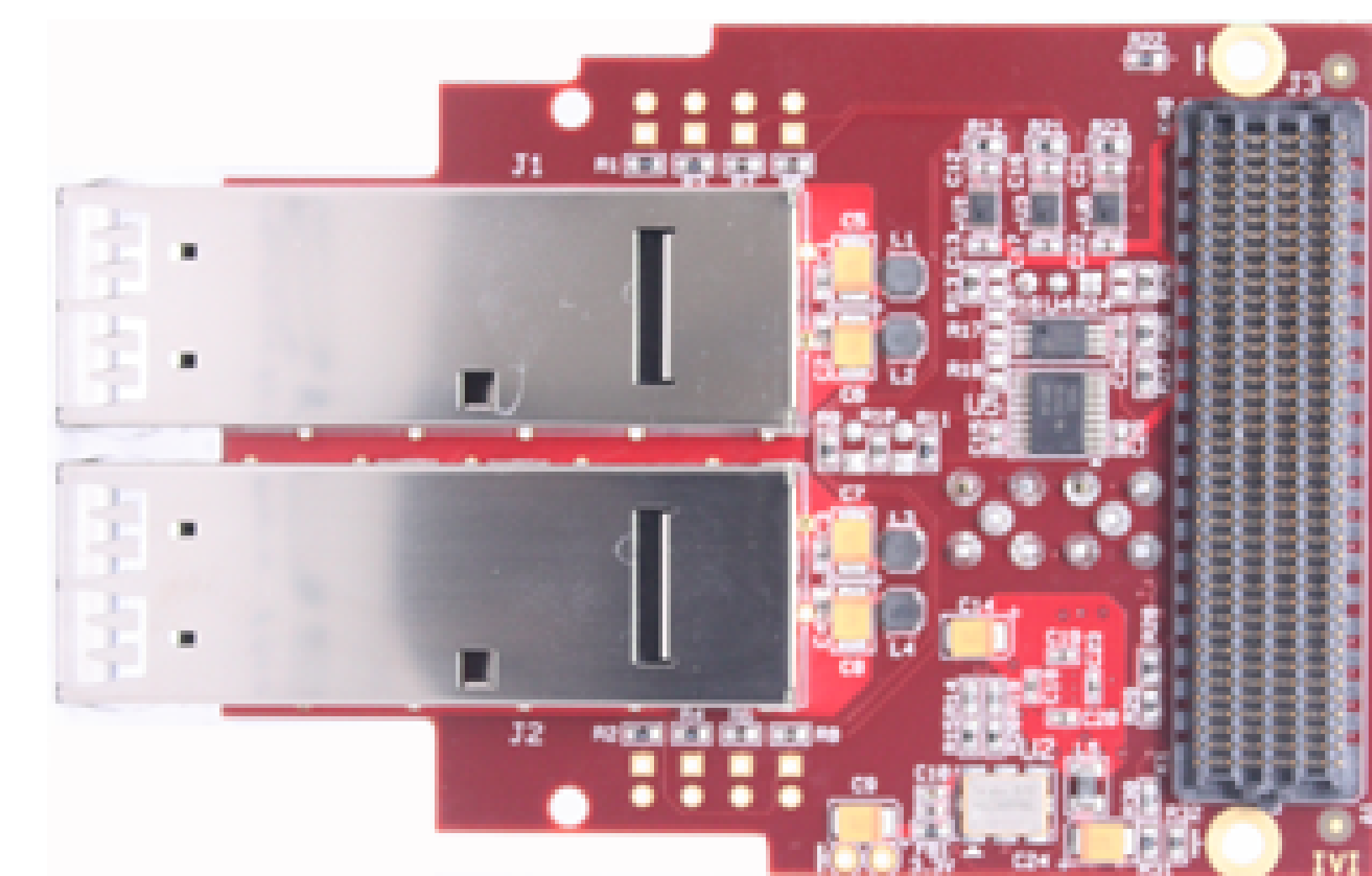


Figure 3: QSFP+

## PMT CONTROL

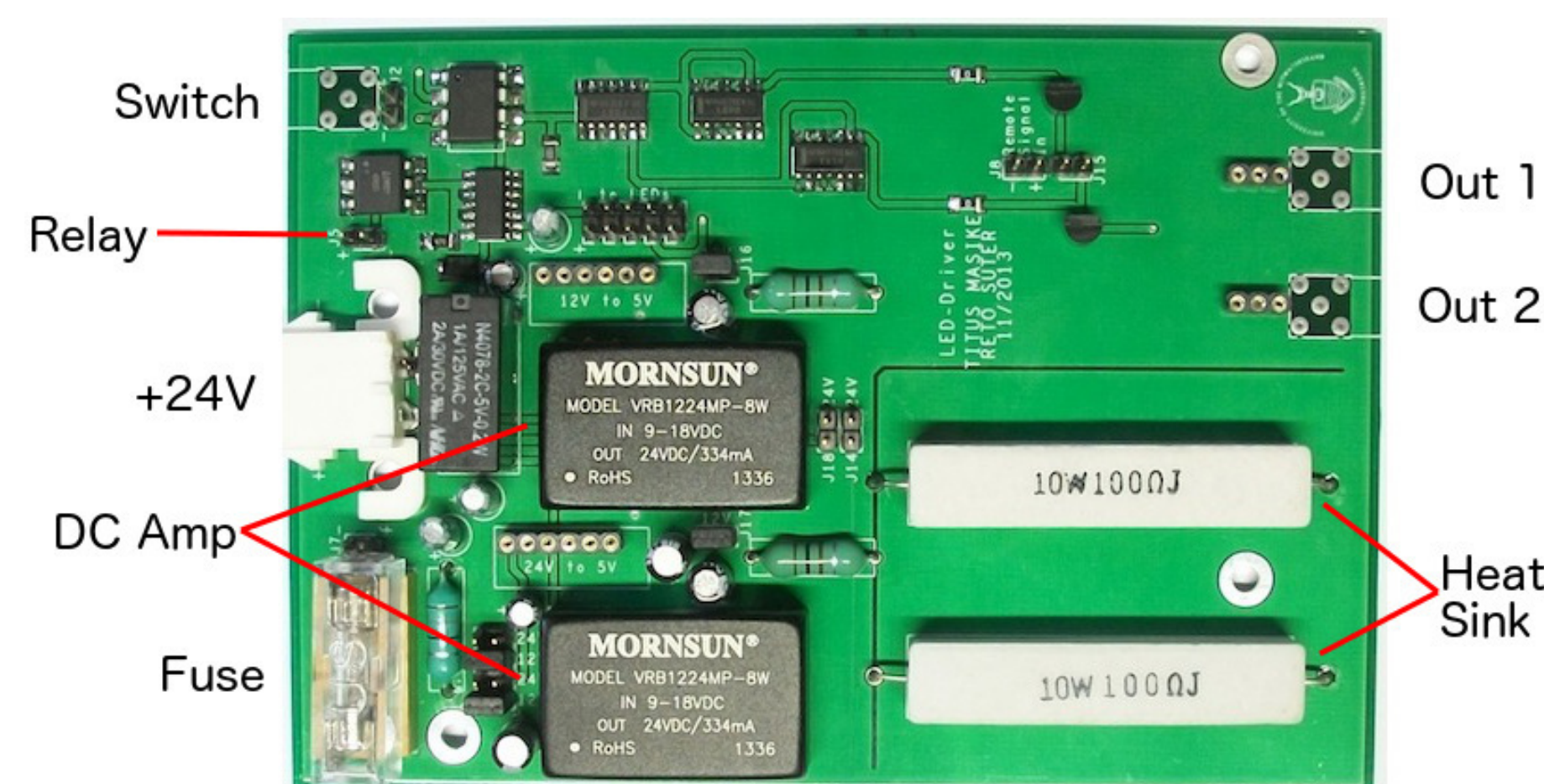


Figure 4: LED driver

The PMTs require a high, stable voltage to amplify pulses in the scintillators. A HV mezzanine board turns on the gain of the PMTs via dedicated cards and controls the bias voltage. The LED driver provides a sharp voltage peak to a passive LED device that illuminates the PMTs, and is controlled by the rising edge of a pulse from the VC707. Two negative pulses (for two sides of the mini-drawer) are generated with an amplitude of 17 V and a width of 20 ns at the orbit frequency.

## FIRMWARE AND SOFTWARE

The system is based on a client-server architecture, where the server communicates via ethernet through a VHDL module with an IPbus implementation and the client connects via UDP protocol. The client is a modular framework with plug-ins for each test. The system performs several tests aimed at diagnosing faulty components:

- Bias test: ADC threshold of the digitizer
- Memory test: diagnose stuck bits in digitized data
- DAC test: linearity check of the digitizer
- Config test: digitizer high and low gain
- Pulse test: pulse shape and ADC stability

These tests provide cross-checks to isolate each subsystem for identifying faulty DACs,

clock-drivers, LVDS-drivers, ADCs, connections, and power supplies.

The on-board flash contains an IPbus protocol to act as the server for the system. Samples are stored by address and retrieved upon trigger request. A python extension has been written to support a user-friendly scripting environment. The results are displayed in a Java GUI for a compile-once, run-everywhere capability. Overall, this architecture is compatible with any operating system.

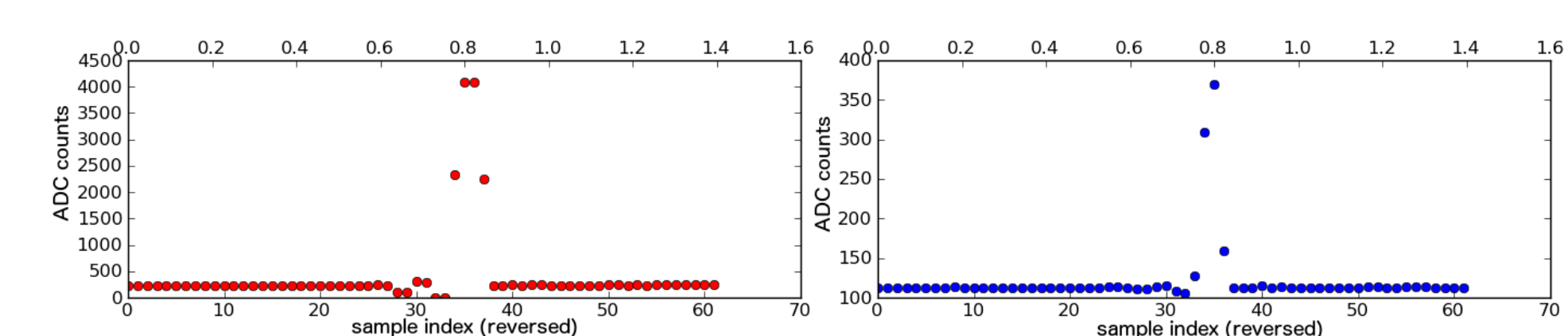


Figure 6: CIS pulse shapes (high and low gain)

## PROSPECTIVE

Prometeo is in a prototyping phase as a hybrid demonstrator. All components are in-hand and undergoing tests as they are added to the system. Charge-injection tests have been successful and pulses have been measured.

## CONTACT INFORMATION

**Daniel Bullock:** daniel.bullock@cern.ch  
The University of Texas at Arlington  
CERN ATLAS TileCal Prometeo