AIDA-PUB-2013-013

AIDA

Advanced European Infrastructures for Detectors at Accelerators

Journal Publication

Achievements of the ATLAS Upgrade Planar Pixel Sensors R&D Project

Calderini,G (LPNHE, UNIPI)

21 October 2013

The research leading to these results has received funding from the European Commission under the FP7 Research Infrastructures project AIDA, grant agreement no. 262025.

This work is part of AIDA Work Package **9: Advanced infrastructures for detector R&D**.

The electronic version of this AIDA Publication is available via the AIDA web site <http://cern.ch/aida> or on the CERN Document Server at the following URL: <http://cds.cern.ch/search?p=AIDA-PUB-2013-013>

Achievements of the ATLAS Upgrade Planar Pixel Sensors R&D Project

G. Calderini
(on behalf of the ATLAS Planar Pixel Sensors Collaboration)

Laboratoire de Physique Nucléaire et des Hautes Energies (LPNHE) Paris, France
Dipartimento di Fisica E. Fermi, Universitá di Pisa, Pisa, Italy

Abstract

This paper reports on recent accomplishments and ongoing work of the ATLAS Planar Pixel Sensors R&D project. Special attention is given in particular to new testbeam results obtained with highly irradiated sensors, developments in the field of slim and active edges and first steps towards prototypes of future pixel modules.

Keywords: Planar Silicon radiation detectors, tracking detectors, fabrication technology

1. Introduction

To extend the physics reach of the LHC, accelerator upgrades are planned which will increase the integrated luminosity to beyond 3000 fb^{-1} and the pile-up per bunch-crossing by a factor 5 to 10. To cope with the increased occupancy and radiation damage, the ATLAS experiment plans to introduce an all-silicon inner tracker with the HL-LHC upgrade. To investigate the suitability of pixel sensors using the proven planar technology for the upgraded tracker, the ATLAS Upgrade Planar Pixel Sensor R&D Project (PPS) was established comprising 19 institutes and more than 80 scientists. Main areas of research are the performance assessment of planar pixel sensors with different designs and substrate thicknesses up to the HL-LHC fluence, the achievement of slim or active edges to provide low geometric inefficiencies without the need for shingling of modules and the exploration of possibilities for cost reduction to enable the instrumentation of large areas. This paper gives an overview of recent accomplishments and ongoing work of the R&D project.

2. The planar pixels sensor technology

Planar pixel sensors are widely used since many years in the tracking detectors of many high-energy experiments. This is now a mature and sound technology, allowing to reach a very high production yield at a limited cost. The experience achieved in the construction and in the many years of operations of detectors equipped with planar pixel sensors represent a guarantee for future trackers. At the same time, a few axes of development can be followed to achieve further improvements. Radiation hardness has been increased, currently allowing good operation conditions even after a fluence of a few $10^{15} n_{eq}/cm^2$ which is what is expected for the non-innermost pixel layers during the Phase-II of the LHC upgrade. Special processes are under study to allow an increased geometrical efficiency by reducing the size of the dead region at the edge of the sensors. This is critical in the assembly of the staves, where the modules are tiled, or for layers in which there is not enough room to stagger the staves in the $r-\phi$ plane to allow an overlap of the corresponding active regions. A few options, as larger wafers, multi-sensor modules or processes as the n-in-p, are also being developed to further reduce the cost of the productions.

3. Development of active-edge sensors

The need to reduce as much as possible the size of the dead region at the border of the sensors has driven the planar pixel community to use intensely the device simulation tools available and optimise the sensor layout. Good results have been achieved by reducing the guard ring region, which represents a low-efficiency portion of the sensor due to the lower electrical field and the distance from the first row of pixels. Already for the design of the ATLAS Insertable B-Layer sensors, preliminary simulations (see for instance [1]) had indicated that the number of guard rings could be reduced and the n-in-n nature of the sensors, in which pixels and guard rings are on opposite faces, could allow to push the first row of pixels inside the guard-ring area. Beam-test analysis showed that some charge collection efficiency was still possible for particles crossing the detector in this region (Fig. 1), thus allowing an improvement of the geometrical acceptance. The solution has been indeed adopted for the ATLAS IBL sensors.

More recently, further optimisation in the number of the guard-rings has been achieved in both n-in-n and n-in-p productions, allowing to reduce the size of the inefficient region down to a typical scale of $300-400\mu m$ (see for example [2]). In addition, an alternative approach based on the use of DRIE (Deep Reactive Ion Etching) and SCP (Scribe, Cleave, Passivate) techniques has allowed the construction of active-edge devices. In the first case the method consists in producing sensors with an edge doping of the same type with respect to the back-side. The net result is to have the cut-line inside an equipotential region, where the absence of electrical field prevents the generation of

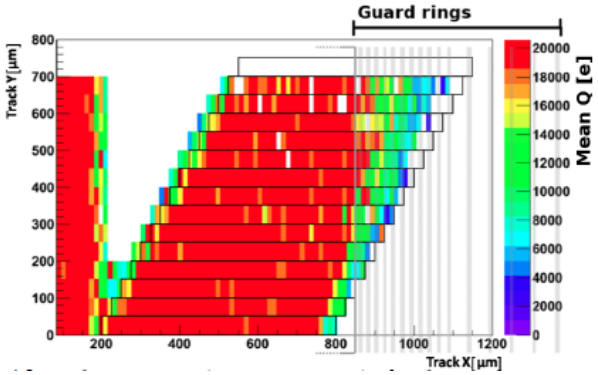

Figure 1: Beam-test analysis of special sensors developed to study the layout optimisation for the ATLAS IBL. Each horizontal rectangle represents a block of pixels and each block is pushed at different positions below the guard rings, which are implanted on the opposite face.

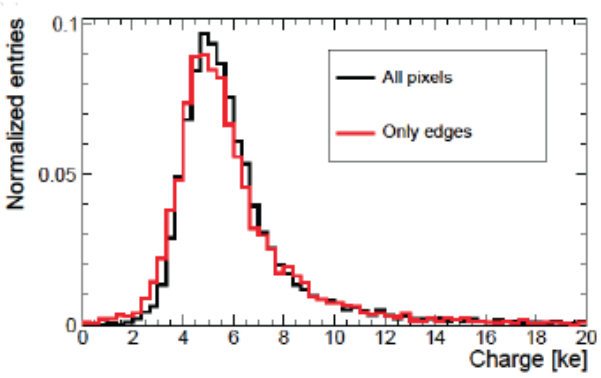

Figure 3: Beam test analysis of collected charge for VTT active-edge sensors. The inclusive distribution and the one for the pixels of the first row are very similar.

edge surface current. Different processes allow this result. A production of n-in-p devices at VTT [3, 4] uses DRIE to excavate a deep and large trench in order to expose the side. A lateral implantation is then started so that the doping of the vertical region becomes similar to that of the backside (see Fig. 2).

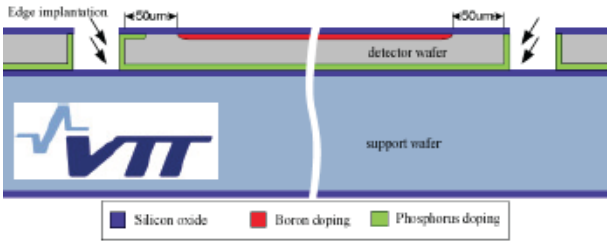

Figure 2: Sketch of the VTT process to achieve active-edge sensors

Using this technique, 100 μm and 200 μm-thick n-in-p sensors are produced in collaboration with MPP Munich, with a distance of the first pixel from the edge of the order of 50 and 125μm. Beam test results indicate that the collected charge distribution is identical for the pixels of the first row and the others, thus showing that the concept works (see Fig. 3).

The beam-test analysis indicates that a hit efficiency of $84^{+9}_{-14}\%$ is achieved in the last 50 μm of the sensor edge, beyond the last pixel implant.

A similar method is used in the FBK (Fondazione Bruno Kessler) [5] process. In this case, the deep trench is again excavated by DRIE, but the lateral doping is obtained by diffusion instead of implantation. The doped trench is finally filled with poly-silicon [6, 7]. The uniformity of the poly-silicon filling is a critical phase of the process. Residuals of air in the 200 μm-deep and 4.5 μm-wide trench (Fig. 4) could severely damage the device during the high-temperature phases of the process.

Using this technique, 200 μm thick n-in-p sensors are produced by FBK in collaboration with LPNHE Paris. ATLAS FE-I3 and FE-I4 designs [8] are used, with different guard-ring numbers and edge distance configurations. The distance of the first row of pixels from the cut-line is typically of the order of $100 - 200\ \mu m$ (Fig. 5).

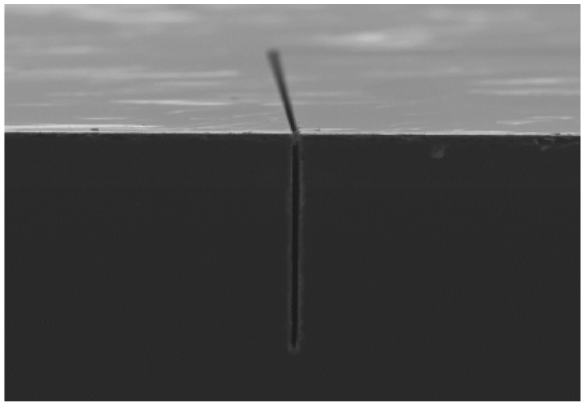

Figure 4: Detail of a deep trench produced by DRIE on a test bulk at FBK

Baby-detectors with a reduced number of pixels but the same guard-ring and edge configuration as the main structures are also produced on the same wafers for test purpose. Measurements show a breakdown voltage exceeding the 100V (even 200V for sensors with more than 1 guard ring), in excellent agreement with simulations (see Fig. 6).

Simulations indicate that even at a dose of $10^{15} n_{eq}/cm^2$ the charge collection efficiency of the pixels of the first row is still significant with respect to the pixels of the central region, provided that a bias voltage exceeding 2-300V is applied (see Fig. 7).

The sensors are presently being bump-bonded to ATLAS FE-I4 chips to be analysed at beam-tests.

A different approach to the problem of edge current has been tested by SCIPP (UCSC) [9] in collaboration with U.S. Naval Research Lab (NRL) [10]. A Scribe-Cleave-Passivate (SCP) technique has been used to block the edge current in the sensors [11, 12]. In this approach the detector is scribed along the edge by laser or XeF_2 etching and cleaved. Once the edge is exposed, the sensor undergoes a passivation phase via plasma-enhanced CVD or alumina deposition (see Fig. 8).

The fixed interface charge determined by the passivation pro-

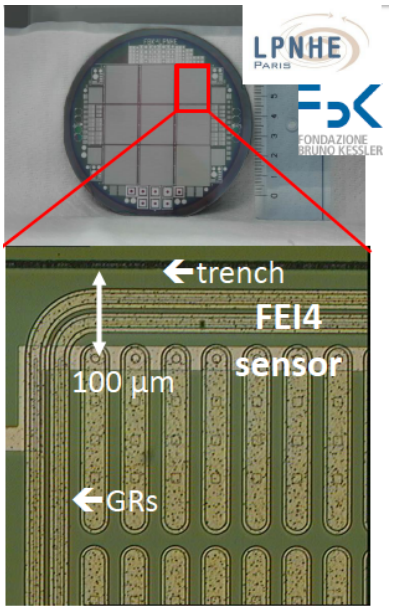

Figure 5: Detail of the edge region of a 2-guard-ring FE-I4 geometry pixel sensor.

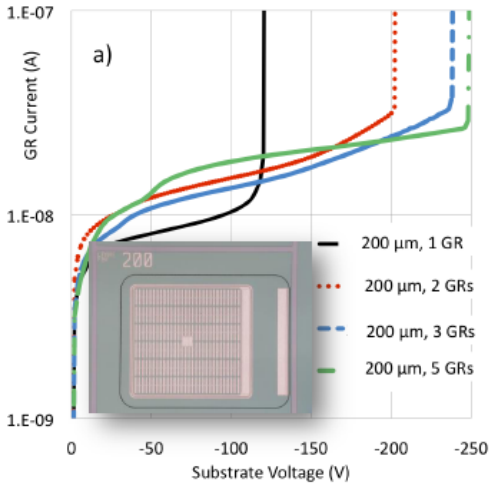

Figure 6: Typical IV behaviour of IV curves for baby detectors with 1, 2, 3, and 5 guard rings. The curves are in very good qualitative agreement with simulations.

cess allows to control the potential across the sidewall, minimising the edge current (see Fig. 9) [13].

Further investigations are under way to determine the behaviour of the sensors treated with SCP after radiation damage.

4. Reducing the costs

One of the key activities in the recent development of planar pixel sensors has been the attempt to reduce the cost of productions. This is critical whenever the use of planar pixels is targeted for middle- and large-surface detectors, as is the case for the external layers of a tracker. Several axes of research have been developed.

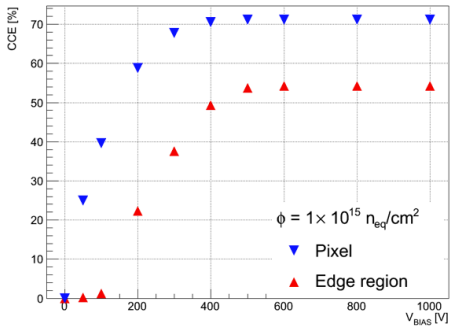

Figure 7: Expected charge collection efficiency after a $10^{15} n_{eq}/cm^2$ dose as a function of bias voltage for central and edge pixels (simulation) .

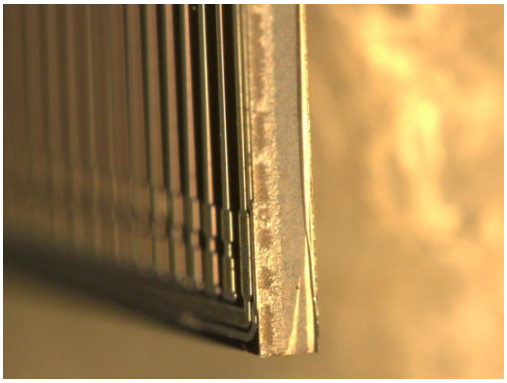

Figure 8: Photo of the sensor sidewall after cleaving and passivation phase.

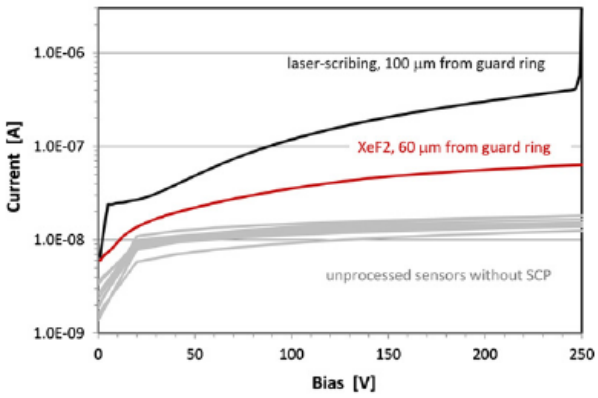

Figure 9: Leakage current behaviour for sensors scribed with a laser (more damaging) at a distance of $100\mu m$ from the guard ring and with XeF_2 PECVD (less damaging) at a distance of $60\mu m$. In the second case, in spite of the reduced distance, the current is lower due to the better quality of the scribing

4.1. Cheaper interconnections

Significant R&D has been devoted to reduce the price of sensor-FEE interconnections per unit area, by replacing the standard bump-bonding by cheaper technologies. In the framework of the ATLAS PPS project, MPP Munich in collaboration with Fraunhofer EMFT [14] has investigated the possible use of Solid-Liquid Inter-Diffusion (SLID) process [4]. The smaller number of process steps with respect to bump-bonding could

translate in reduced cost. In addition, the limitations on the geometrical pitch are less severe in this technology. Wafer to wafer as well as chip to wafer connections are feasible. SLID-based modules are expected to be delivered by the end of 2013 and they will be characterised with beam-tests.

Alternative low-cost bonding technologies as the IBM C4NP [15] are also being evaluated by the ATLAS PPS Collaboration.

4.2. Multi-chip modules

An effective solution to achieve lower-cost productions is the development of larger sensors, which is made possible by the use of larger wafers by foundries, and the assembly of multi-chip modules. Many sensor providers recently moved their productions to 6-inch and even 8-inch wafers. This allows the optimisation of the wafer layout and the presence of more large-area sensors on the same wafer, features which translate globally into a significant cost-reduction. On the other hand, the larger size of the sensors allows the assembly of multi-chip modules, with a consequent reduction of the number of handling operations per unit of area and a significant cost reduction. These larger sensors can fit well the specifications for outer layers and the side end-cap regions. In the framework of the ATLAS PPS Collaboration, recent productions of large "quad" sensors on 6-inch wafers have been done at CiS [16], HPK (see Fig. 10) [17] and Micron (see Fig. 11) [18]. Some of the multi-chip modules have already been measured at beam-tests and the analysis of the results is underway.

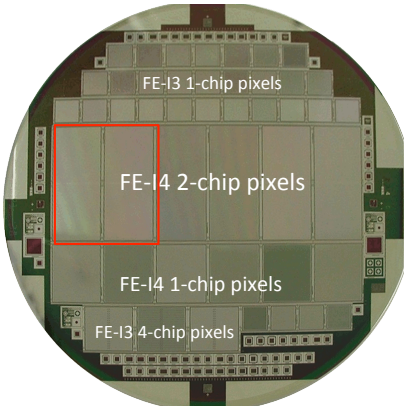

Figure 10: Layout of a recent 6-inch production by Hamamatsu Photonics KK, in collaboration with the ATLAS Japan Silicon group. The large 2x2 FE-I4-design sensors are visible in the central part of the wafer, together with FE-I4-design and FE-I3-design single sensors.

5. Design improvements

In addition to the cost reduction, an important line of research consists in the further optimisation of the sensor design to achieve the best possible performance even after heavy irradiation and years of operation in a high-energy physics experiment. One of the critical issues with the punch-through structure of the biasing system is a certain loss of efficiency in the dot region after irradiation. An effort has been made to provide different biasing schemes in order to avoid such a problem. The

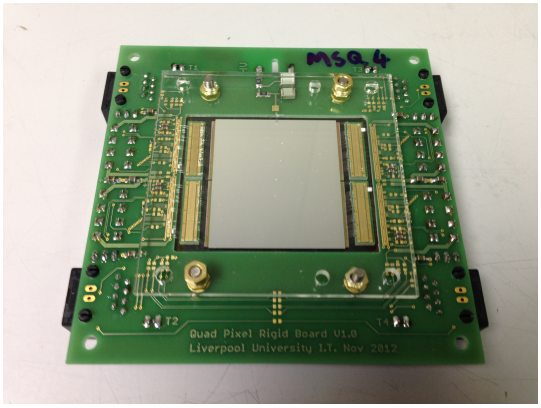

Figure 11: Detail of a large 2x2 sensor produced by Micron in collaboration with the ATLAS Liverpool and Glasgow groups. The sensors is already bump-bonded and mounted on the periphery card to be read-out and installed in the beam-test.

design of bias paths with poly-silicon structures has been studied by the ATLAS Japan Silicon group, which has proposed a number of solutions over the years. The position of the poly-silicon line inside the pixel is of great importance since it can affect the charge collection efficiency. A new design has been recently proposed in which the line runs along the inner part of the pixel edge, which seems to optimise the hit efficiency, even after radiation damage. In addition a new proposal of biasing scheme for $25x500\mu m$ pixels has been proposed. In this design the bias lines are staggered on alternating pixels (see Fig. 12).

Figure 12: Detail of the poly-silicon biasing scheme for a sensor with $25x500\mu m$ pixels designed by the ATLAS Japan Silicon group and produced by Hamamatsu Photonics KK. The biasing lines are staggered on neighboring pixels.

A different technique has been proposed by the ATLAS group of Dortmund, which studied a distribution scheme obtained by bias rails, narrow metal strips running over the oxide layer and providing the electrical network to the pixels. Also in this case the geometrical configuration can influence the hit efficiency and several different concepts have been tested (see Fig. 13).

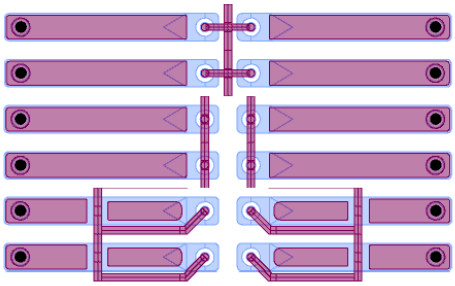

Figure 13: Detail of the metal biasing scheme for a sensor with $50x250\mu m$ pixels designed by the ATLAS Dortmund group and produced by CiS. Different geometry designs have been tested to optimise the sensor performance.

6. Bulk materials

Special mention needs to be done for a recent study by the ATLAS Dortmund group, which is trying to improve the radiation hardness of n-in-n sensors by the use of a MCz bulk. The intermediate layers of the upgraded ATLAS tracker will be exposed to a mix of ionising and non-ionising radiation. MCz material is expected to have a better performance with respect to standard DOFZ bulk under these conditions [19]. For this reason, MCz FE-I4-design prototype sensors have been produced and irradiated with protons at the CERN PS up to three different fluences (0.8, 1.6 and 3.0 $10^{15} n_{eq}/cm^2$. After this first phase they have been tested with a ^{90}Sr source and at a beam-test at CERN, showing a good residual charge collection efficiency, at least for the first two irradiation samples.

They are presently undergoing the second phase of irradiation, the one involving neutrons, at the Ljubljana reactor. The plan is to test them again in one of the next PPS beam-test.

7. Conclusions

Planar pixel sensors represent a sound and well-established technology for the tracking detectors of high-energy physics experiments. Many activities are developed in parallel in the framework of the ATLAS PPS Collaboration to improve the sensors performance, even after the heavy irradiations expected in the Phase-II of LHC, and to reduce the costs of productions. New developments in techniques of fabrication of active-edge sensors have been presented. Progress in interconnection technology allows to reduce the cost of module productions, as well as the use of larger sensors and multi-chip modules. New solutions for the biasing schemes have been presented.

8. Acknowledgements

This work has been partially performed in the framework of the CERN RD50 Collaboration. Some of the irradiations and the beam test measurements leading to these results has received funding from the European Commission under the FP7 Research Infrastructures project AIDA, grant agreement no. 262025. The edgeless sensor production at FBK was supported in part by the Autonomous Province of Trento, Project MEMS2.

References

References

[1] G. Calderini *et al.*, Nucl.Instrum.Meth. A636 (2011) S37-S41.
[2] G. Casse *et al.*, DA AGGIUNGERE
[3] VTT Technical Research Centre of Finland, P.O. Box 1000, FI-02044 VTT, Finland; http://www.vtt.fi
[4] A. Macchiolo *et al.*, "Thin n-in-p pixel sensors and the SLID-ICV vertical integration technology for the ATLAS upgrade at the HL-LHC", Proceedings for Pixel 2012 Conference, Nucl. Instr. and Meth. A, in press, http://arxiv.org/abs/1210.7933
[5] Fondazione Bruno Kessler, Centro per i Materiali e i Microsistemi (FBK-CMM) Povo di Trento (TN), Italy. http://www.fbk.eu
[6] M. Bomben *et al.*, Nucl. Instrum. and Meth. A 712, 41 (2013).
[7] G. Calderini *et al.*, Development of edgeless Silicon pixel sensors on p-type substrate for the ATLAS High-Luminosity upgrade, Proceedings for 9^{th} HSTD Hiroshima 2013 Conference, Nucl. Instrum. and Meth. A, in press, http://arxiv.org/abs/xxxx.xxxx
[8] M. Garcia-Sciveres, D. Arutinov, M. Barbero, et al. The FE-I4 pixel readout integrated circuit - 2011. Nucl.Instrum.Meth., A636, 155
[9] Santa Cruz Institute for Particle Physics (SCIPP), University of California Santa Cruz, USA.
[10] U.S. Naval Research Laboratory, 4555 Overlook Ave., SW Washington, DC 20375, http://www.nrl.navy.mil
[11] M. Christophersen et al., Nucl. Instrum. and Meth A 699 (2013) 14
[12] M. Christophersen et al, Solid-State Electronics 81 (2013) 8.
[13] V. Fadeyev, et al., Nucl. Instrum. and Meth. A (2013), http://dx.doi.org/10.1016/j.nima.2013.03.046
[14] Fraunhofer Research Institution for Modular Solid State Technologies EMFT, Hansastrasse 27d, 80686 Muenchen, Germany, http://www.emft.fraunhofer.de/
[15] C4NP Lead Free Solder Bumping and 3D Micro Bumping, 2008 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp 333-339.
[16] CiS Forschungsinstitut für Mikrosensorik und Photovoltaik GmbH Konrad-Zuse-Strae 14, 99099 Erfurt, Germany; http://www.cismst.org
[17] Hamamatsu Photonics KK, Japan; http://www.hamamatsu.com
[18] Micron Semiconductor Ltd. 1 Royal Buildings, Marlborough Road, Lancing Business Park, Lancing, Sussex, BN15 8SJ, England; http://www.micronsemiconductor.co.uk
[19] Kramberger *et al.*, Nucl.Instrum.Meth. A609 (2009) 142-148