THE CMS TRACKER FOR HL-LHC

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The planned upgrades of the LHC and its injector chain are expected to allow operation at luminosities around or above $5 \cdot 10^{34}$ cm$^{-2} \cdot$ s^{-1} sometimes after 2020, to eventually reach an integrated luminosity of 3000 fb^{-1} at the end of that decade. In order to fully exploit such operating conditions and the delivered luminosity, CMS needs to upgrade its tracking detectors and substantially improve its trigger capabilities. To achieve such goals, R&D activities are ongoing to develop solutions that would allow including tracking information at Level-1. Some of the options considered are reviewed, discussing their potential advantages and disadvantages.

1. INTRODUCTION

The increase of the LHC luminosity above its original design figure of 10^{34} cm$^{-2} \cdot$ s^{-1} requires a substantial upgrade of the CMS tracking system, to cope with much more demanding requirements and to implement additional functionality.

The pixel detector is the first part of the tracker that will show limitations in high-rate and therefore will be upgraded already in the middle of this decade. The new detector [1] will feature 4 barrel layers and 3 forward discs, yielding on average one more spatial point measurement per track compared to the present system, in the whole acceptance range. Optimized engineering of mechanics and services, together with two-phase CO_2 cooling, will provide a substantial reduction of material in the tracking volume, while upgraded front-end ASICs will enhance the robustness of the system at high rate. The new pixel detector together with the outer strip tracker will provide optimal tracking performance to CMS through 2020.

After the upgrade of the accelerator complex foreseen for the beginning of the next decade, the LHC is expected to produce an instantaneous luminosity of $5 \cdot 10^{34}$ cm$^{-2} \cdot$ s^{-1}, that will be sustained for a large fraction of each fill through luminosity levelling. The quoted luminosity corresponds to approximately 100 pileup events per bunch crossing if the operating frequency is 40 MHz [1]. For such a scenario, CMS will eventually collect up to 3000 fb^{-1}, after several years of operation, and its tracking system will have to be improved in terms of radiation resistance,

[1] The number of pileup events would be larger than 200 if the same luminosity was achieved with 20 MHz operation, which represents a much more demanding condition for the detectors.

readout granularity and ability to contribute information to the Level-1 trigger. The whole tracker will have to be replaced at the beginning of the next decade: this upgrade ("phase-2" upgrade) will involve the outer strip tracker, as well as a further upgrade of the inner pixel detector.

This paper describes the main R&D lines for the development of the upgraded tracker, with particular focus on the options considered for the implementation of the trigger functionality. Some basic requirements and possible features of the phase-2 pixel upgrade are also mentioned.

2. REQUIREMENTS FOR THE STRIP TRACKER UPGRADE

The upgraded tracker will have to provide improved tracking performance in a more challenging environment, while producing at the same time fast information for the Level-1 trigger. The basic requirements can be summarized as follows:

(i) Robust tracking in operation with up to 200–250 collisions per bunch crossing in the worst-case scenario of 20 MHz operation (to be compared to the original LHC design figure of 20 collisions per crossing); this can be achieved by maintaining the occupancy at the level of a few percent, which requires increased granularity.

(ii) Ability to provide satisfactory performance up to an integrated luminosity of about 3000 fb^{-1}, to be compared with the original figure of 500 fb^{-1}; this requires the selection of more radiation hard silicon sensor material, especially for the innermost regions, as well as more stringent criteria in the qualification of electronics and mechanical assemblies.

(iii) Reduced material in the tracking volume; the material is the most severe limitation on the performance of the present tracker [2], and it is dominated by electronics and services (notably in the region between barrel and end-cap).

(iv) Ability to contribute information to the Level-1 trigger decision, in order to hold the overall rate below 100 kHz, without compromising the physics performance of CMS. The trigger requirement is discussed in more detail below.

2.1. Tracking Information at Level-1

The event filtering at Level-1 becomes substantially more challenging at high luminosity, not only because the rate of events passing a given selection scales with the instantaneous luminosity, but also because the performance of selection algorithms degrades with increasing pile-up. For example, the single muon Level-1 rate has an irreducible tail due to poorly measured tracks that are compatible with straight trajectories, and are therefore not removed even by increasing the p_T threshold: such an effect is aggravated at high luminosity by accidental coincidences.

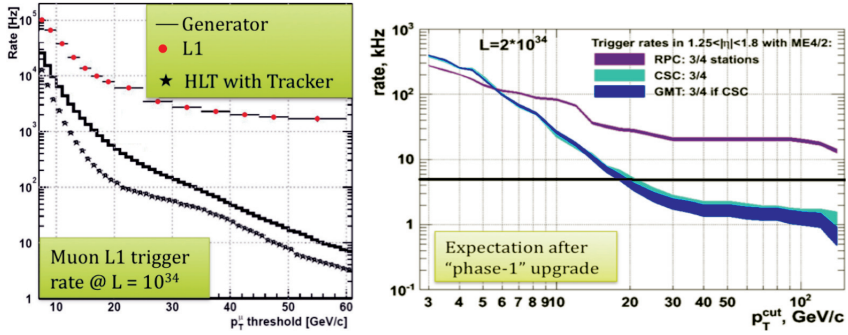

Fig. 1. Expected Level-1 single muon rate (left) as a function of threshold for a luminosity of 10^{34} cm$^{-2} \cdot$ s^{-1}, in the present system; the rate becomes almost flat for high p_T cuts, due to poorly reconstructed tracks. The High-Level Trigger rate, instead, follows closely the generator rate, thanks to the use of tracking information. With the planned "Phase-1" upgrade of the trigger system (right), the performance of the Global Muon Trigger will be improved, achieving a rate of 5 KHz for a target threshold of 20 GeV/c at $2 \cdot 10^{34}$ cm$^{-2} \cdot$ s^{-1}. At higher luminosities further improvements are needed

In the High-Level Trigger (HLT), where the information from the tracker is also added, the reconstruction is substantially improved and the rate of muon candidates follows closely the generator rate. Some improvements are expected with the "Phase-1" trigger upgrade (e.g., including the 4th RPC and CSC stations, now under construction, will allow one to request 3 out of 4 points for a muon candidate), which will yield an acceptable rate for luminosities up to about $2 \cdot 10^{34}$ cm$^{-2} \cdot$ s^{-1}, but the rate will saturate again the available quota for higher luminosities (see also Fig. 1). Hence, an option to investigate is to anticipate the use of tracking information in the Level-1 selection, along the lines of what is presently done in the HLT. A similar problem is present in the single electron trigger, where high pile-up reduces the rejection power of isolation cuts on the calorimeter clusters.

3. MAIN R&D ACTIVITIES

This section describes briefly the main on-going R&D activities, except the development of the trigger functionality that is the subject of the next section.

3.1. Silicon Sensors R&D

A vigorous R&D program is being carried out, to identify the most suitable sensors for the tracker upgrade. A large sample of more than 150 wafers has been procured from Hamamatsu Photonics, with a

combination of materials (Float-zone, Magnetic Czochralski, Epitaxial) and technologies (n-bulk, p-bulk with p-spray and p-stop isolation), and different thicknesses. The samples are studied with an extensive program of successive proton and neutron irradiations, interleaved with detailed laboratory characterizations. The tests are complemented with device simulations. Such detailed work on a homogeneous, high-quality sample of wafers is providing an unprecedented understanding of material properties and process details, which will be crucial to select the most appropriate option for the outer tracker upgrade. At the same time, the study of the pixelated structures present on those wafers will allow one to define and characterize a solid baseline for the phase-2 pixel upgrade in planar technology, to be compared with more exotic options such as 3-d silicon or diamonds, which are also being studied. More details can be found in [3].

3.2. Data Links, Power and Cooling

The auxiliary electronics will rely on the ongoing developments for data links and front- end powering.

A bi-direction data link integrated at the module level will carry all signals for readout, control and monitoring. A further development of the GigaBit Transceiver (GBT) [4], in 65 nm CMOS technology will provide substantially reduced power consumption for the same bandwidth ("Low Power GBT") of 5 Gbs per link. The design effort has recently started.

The powering system will exploit on-board DC-DC conversion, to reduce the cross-section of the power lines inside the tracking volume, and of the cables bringing the current from the back-end. Each module will be powered through a buck converter, also integrated at module level. The current developments [5], aiming at the powering system for the phase-1 pixel upgrade, will also serve as basis for the phase-2 upgrade.

For the cooling, the baseline is a two-phase CO_2 system, similar to the one developed for the pixel upgrade [6]. Two-phase CO_2 provides substantial advantages in terms of lightweight cooling pipes and heat exchangers inside the tracking volume, and is suitable for low-temperature operation. The large size of the tracker system, compared to the pixel system, will require a significant further R&D effort, that will start as soon as the pixel system is finalized.

4. IMPLEMENTATION OF THE TRACKING TRIGGER

The concept chosen is based on modules that provide at the same time selected information for the Level-1 processing, at the bunch crossing rate of 40 MHz, and all the recorded signals upon reception of a Level-1 trigger signal, at the foreseen rate of 100 kHz.

The signals sent out to the Level-1 processing will then be combined with calorimeter and muon trigger data (with finer granularity than

presently employed) to form improved "physics objects" that are transmitted to the Global Trigger.

This option requires that rejection of low-p_T tracks be performed locally in the module front-end, to limit the bandwidth on the 40 MHz stream. Possible implementations of local data reduction follow the lines of what was originally proposed in [7], and take advantage of the strong CMS magnetic field, as discussed in more details below.

4.1. Modules with p_T Discrimination

The requirement for the module design is to reject locally signals from low-p_T particles, which are not interesting for the Level-1 reconstruction: rejecting particles with p_T below 1–2 GeV reduces the bandwidth requirements by one order of magnitude or more.

The basic concept consists of correlating signals in two closely-spaced sensors: the distance between the hits in the $x-y$ plane is correlated with the particle p_T, allowing the p_T discrimination to be made. A pair of hits that fulfils the selection cut is called a "stub", and its coordinates are sent out for the Level-1 processing (see sketches of Fig. 2). For a given p_T, the distance between the hits forming the stub is larger at larger radii; moreover, if the module is placed in end-cap configuration, the same discriminating power is obtained with a larger spacing between the two sensors, compared to a barrel module placed at the same radius. The effective p_T cut provided by the modules in the different locations can be optimized by tuning both sensor spacing and acceptance window. The options under study to realize modules with p_T discrimination capability ("p_T modules") are discussed below interface.

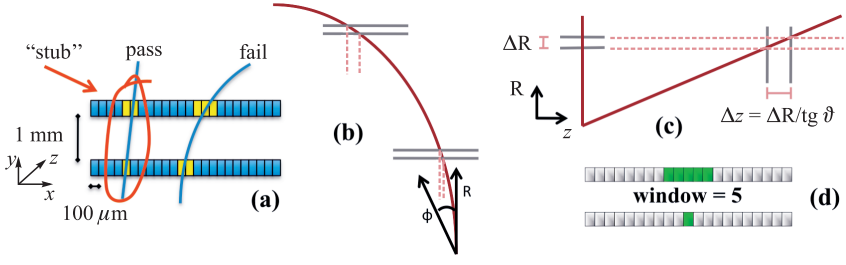

Fig. 2. Correlation of signals in closely-spaced sensors allows one to reject low-p_T particles (*a*). The same transverse momentum corresponds to larger distance between the two signals at large radii, for same sensor spacing (*b*). In end-cap configuration, a larger spacing between the sensors is needed to achieve the same discriminating power as in the barrel at the same radius (*c*). The acceptance window (*d*) can therefore be tuned at the same time as the sensors spacing to achieve the desired p_T filtering in the different regions of the detector

4.1.1. The "2S" module. The simplest p_T module type is an assembly of two strip sensors read out at the edges by the same set of front-end ASICs that implement the correlation logic. In the model shown in Fig. 3 two sensors of about 10×10 cm are mounted on a mechanical structure that provides support and cooling, and connected at the edges on the two sides of a high-density substrate carrying the ASICs. Sensors and substrate are connected with wirebonds, while the ASICs can be bump-bonded onto the substrate. The strip length has to be half of the module size, hence about 5 cm, and a suitable pitch is 90 μm, corresponding to 2×1024 channels per sensor.

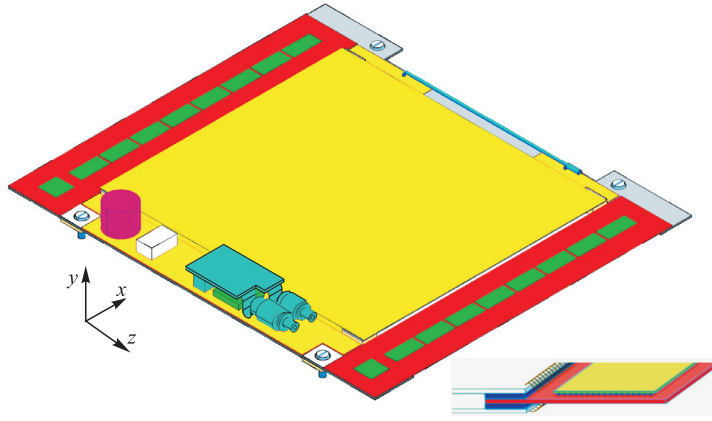

Fig. 3. Model of a "2S module", made of 2 Strip sensors read out at the edges by a common set of ASICs. A lightweight frame provides support and cooling to sensors and electronics, including a "service hybrid", carrying the auxiliary electronics for power and readout. The connection between the sensors and the substrate carrying the ASICs is implemented through wirebonds (sketch in the bottom-right corner)

This concept results in a lightweight assembly that can be realized with commercial interconnection technologies. The estimated power consumption for the readout electronics, including the correlation logic, is below 2 W, comparable to the lowest values in the present tracker. The main limitation of this type of module is the lack of segmentation in the z direction: in order to implement effective isolation cuts on calorimeter clusters, the Level-1 tracks must also have a reasonable precision in the z coordinate. In addition, the relatively long strips limit the use of this module in the radial region above 50 cm, because of occupancy.

4.1.2. The "PS" module. To overcome the limitations of the 2S module, another p_T module concept is under study, based on the assembly of one strip and one pixel sensor. The module has an area of approximately 5×10 cm. The strip sensor is segmented into 2×1024 strips, making

them approximately 2.5 cm in length. The individual pixels on the pixel sensor are approximately 1.5×0.1 mm in size (see Fig. 4). The shorter module dimension along the z coordinate is driven by the need to cover the entire length with two pixel chips, and at the same time the shorter strips make the module suitable for operating in regions with higher particle densities. As for the 2S module, strips are read out at the edges, and the connectivity between the top and bottom sensors is realized through wirebonds on the two sides of the substrate. The chosen dimensions allow one to obtain two sensors from a 6″ silicon wafer, while the 100 μm pitch in the pixel sensor ensures compatibility with large-volume industrial bump-bonding. In this case, the correlation logic is implemented in the pixel ASIC. The auxiliary electronics is also implemented at the module level, on two "service hybrids" located on the short sides of the sensor. One service hybrid carries the DC-DC converter providing power to the module, the other carries the readout electronics and the optical converter. A detailed discussion of this module can be found in [8].

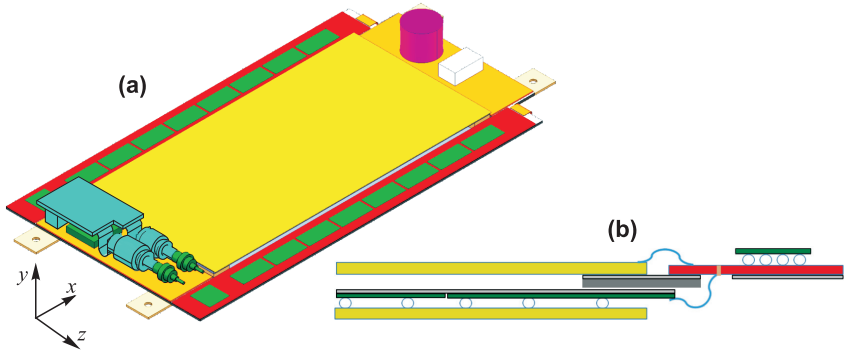

Fig. 4. Model of a "PS module". Overall view of the assembly (*a*), and sketch showing the interconnectivity (*b*); strips are oriented along the z axis. The auxiliary electronics is integrated on two "service hybrids" located on the short sides of the sensor

Compared to the 2S module, this concept offers a sufficiently precise measurement of the z coordinate from the pixellated sensor, while the 2.5 cm long strips allow the module to be used down to 20–25 cm radius. On the other hand, the power consumption is expected to be about 5 W, dominated by the pixel ASICs: a four-fold increase in power density compared to the 2S module, which translates to a higher estimated density of material.

4.1.3. The "VPS" module. A different approach to the construction of a pixel/strip p_T module is based on vertical interconnections. One 3-d chip reads out both the pixellated sensor and the short-strip sensor, connected by analogue paths through an interposer [9], and implements the

correlation logic. The use of vertical connectivity removes all constraints between module dimensions and sensors segmentation: such a module can in principle be made in 10×10 cm size, and, if needed, the strip length can be reduced to further reduce the occupancy (e.g., about 1 cm).

Since there is no connectivity between modules, a larger module size offers advantages for the integration of hermetic surfaces, reducing the need of overlaps. On the other hand, feasibility, reliability and yield of vertical interconnections for large-surface assemblies need to be verified, considering the demanding operating conditions inside CMS. In addition, in this concept a 1 mm thick interposer covers the entire surface of the module, defining the spacing between the two sensors, providing the top-to-bottom connectivity and carrying power lines and readout signals: the development of a lightweight interposer with the necessary electrical and mechanical properties is a key issue to realize a module with an acceptable material density.

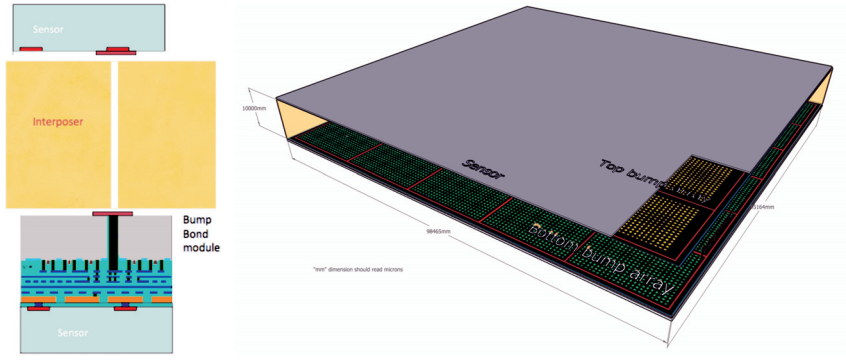

Fig. 5. Sketch of the connectivity for a "VPS module" (left): a 3-d ASIC reads out at the same time the pixellated sensor and, through analogue paths in the interposer, the short-strip sensor on the other side. The interposer defines the spacing between the two sensors, carries at the same time power lines and readout signals. A 3d view of a 10×10 cm size module is shown on the right

5. EVALUATION OF TRACKER OPTIONS AND GEOMETRIES

A dedicated standalone software package ("tkLayout") has been developed to quantitatively evaluate the different options and geometries for the tracker upgrade. The software generates a detector layout starting from a reasonably small set of basic parameters, and also provides simple and flexible implementation of material densities for active and inactive volumes, including the routing of the services. The software calculates, as a function of pseudorapidity, the expected tracking precision and the performance potential for the Level-1 track reconstruction, as well

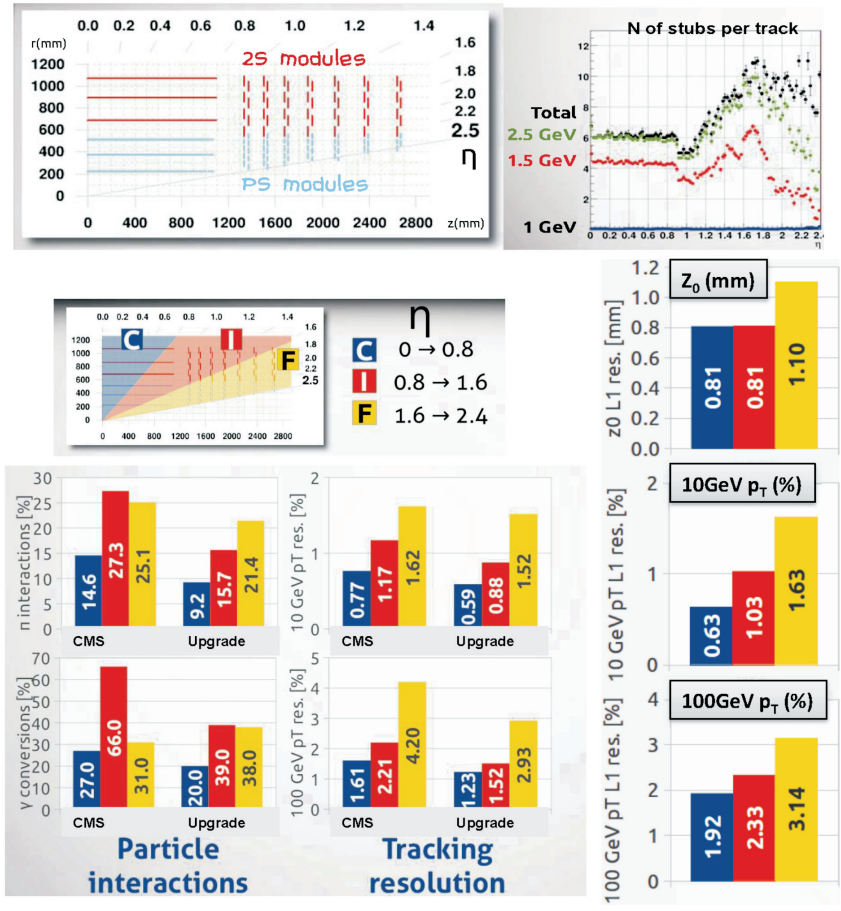

Fig. 6. Example of a detector layout under study, based on a barrel+ endcap geometry. The outer part is populated with 2S modules, the inner part with PS modules providing precise z coordinates. The sensor spacing and acceptance window in the modules is tuned to have high stub finding efficiency for p_T above 2–2.5 GeV, and good rejection for p_T of 1 GeV and below (plot in top-right corner). The performance of this option is compared with the present tracker in terms of fraction of interacting hadrons and photons, and p_T resolution for 10 GeV and 100 GeV particles, in three rapidity regions (histogram on the left side): a significant improvement appears to be achievable in all aspects, despite the implementation of the trigger functionality. The performance potential for the tracking at Level-1 is shown in the three histograms on the right side, in terms of z_0 resolution and p_T resolution for 10 GeV and 100 GeV tracks; this is to be understood as an upper limit of what would be achievable, as it does not account for limitations arising from the available processing time at Level-1

as the fraction of converted photons and interacting pions. In addition, it generates summary statistics such as number of modules, readout channels, power consumption, total weight and many others. For the implementation of the trigger output, a dedicated functionality allows one to optimize the sensor spacing and the width of the acceptance window in the different tracker regions, to maximize the stub finding efficiency above the chosen p_T cut, while maintaining the fake rate at an acceptable level. The package has been validated by modelling the present tracker, demonstrating an excellent agreement between the predicted performance and the one measured from the real detector.

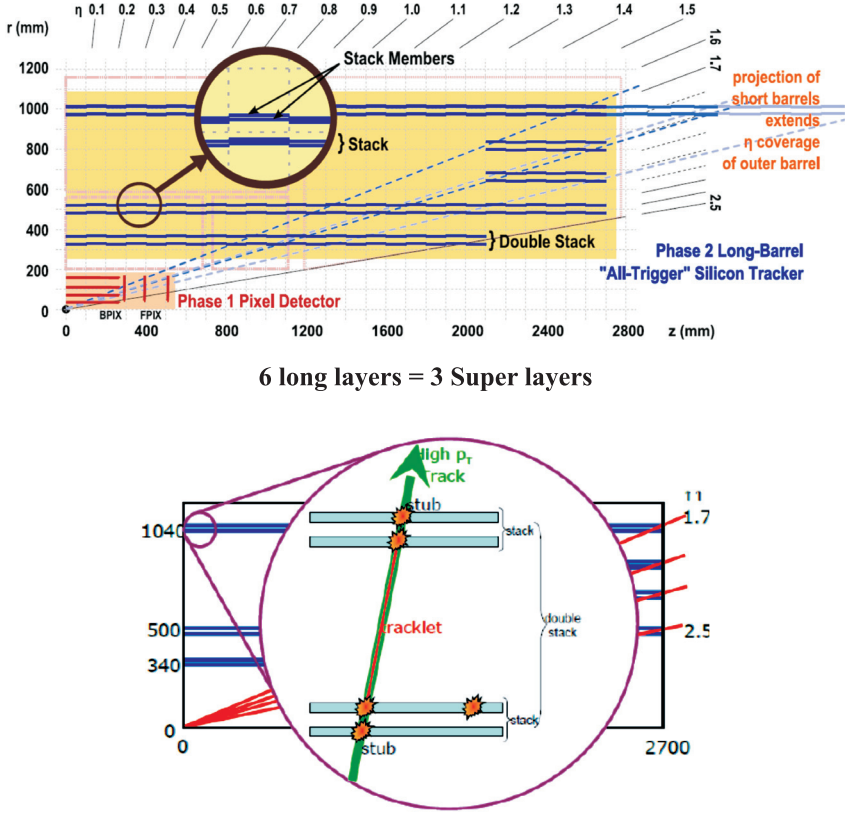

Fig. 7. Tracker layout based on the "double-stack" geometry (top). The geometry is optimized to minimize the combinatorial in the track finding. Within each "super-layer", pairs of stubs are matched to form "tracklets" (bottom). A tracklet has sufficient precision to be extrapolated to the next super-layer, to be associated to other stubs or tracklets

An example of detector geometry under study is shown in Fig. 6, along with some plots showing the main aspects of the expected detector performance (the pixel detector is assumed to be the same as the "phase-1" upgrade).

The analysis of the detector model shows that fully satisfactory tracking performance is achievable, with substantial improvements compared to the present detector. The stub finding efficiency and the stub rates expected from the different regions of the detector have been verified with the full CMSSW simulation, validating the estimates from the standalone modelling. The feasibility of track reconstruction in the Level-1 trigger processors is yet to be proven; a study based on Associative Memories is underway.

A different detector concept is optimized to facilitate track reconstruction at Level-1. The geometry consists only of six barrel layers, arranged in pairs located at a relatively small distance of about 4 cm, forming three "super-layers"; each layer is populated by p_T modules ("double-stack" geometry). The two layers of a super-layer have the same φ-multiplicity, to minimize the amount of connectivity and simplify the processing at the back-end. Stubs are first used as seeds to find matching stubs in the other layer of the same super-layer: two matching stubs in a super-layer form a "tracklet", that has sufficient precision to be extrapolated to the other super-layers and associated to other stubs or tracklets, to eventually form the Level-1 tracks. The detector layout and track finding concept is sketched in Fig. 7.

A detailed description of this track finding concept can be found in [10].

6. OUTLOOK

A coarse schedule for delivering the upgraded Tracker by the Long Shutdown 3 ("LS3", currently planned around 2022) has been developed. The exercise shows that, given the long time needed for the large procurements, the production and quality of control of the part, and the assembly and testing of the detector, substantial prototyping effort should start already in 2013, and the detector concept needs to be defined at latest by the end of 2013. The back-end systems, on the other hand, can be designed in the second half of the decade, to take advantage of the advancements in the relevant technologies.

The phase-2 upgrade of the pixel detector can profit from about 2 years of additional R&D, as the time needed for the detector construction is shorter. The main requirements for the detector are the extreme radiation hardness of the sensor material, a small pixel size and a readout chip able to operate with low threshold, while keeping the power density under control. There is consensus on the choice of 65 nm CMOS as a good target technology for the readout chip.

An important open question concerns the possibility that the phase-2 pixel detector also contributes to the L1 trigger decision. At radii smaller than 20 cm local data reduction is not viable, hence for the pixel detector the only plausible option would be a regional readout based on information provided by the calorimeters and the muon system ("Level-0").

7. CONCLUSIONS

Substantial R&D effort is ongoing, to develop an upgrade for the outer tracker, offering higher granularity, enhanced radiation hardness, reduced material, and capability to contribute to the Level-1 trigger decision. A coarse schedule has been outlined, aiming at delivering such detector by LS3.

Two detector geometries are being studied, corresponding to two different concepts for track finding at Level-1. In parallel with the development of Level-1 track finding, the integration of the tracks in the Level-1 reconstruction can proceed, to assess the benefit of the track trigger option, and establish the possible need of pixel information.

The ultimate upgrade of the pixel detector also starts to receive attention: a development plan for the coming few years is under discussion.

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