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Development of a DC-DC conversion powering scheme for the CMS Phase-1 pixel upgrade

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ABSTRACT: A novel powering scheme based on the DC-DC conversion technique will be exploited to power the CMS Phase-1 pixel detector. DC-DC buck converters for the CMS pixel project have been developed, based on the AMIS5 ASIC designed by CERN. The powering system of the Phase-1 pixel detector is described and the performance of the converter prototypes is detailed, including power efficiency, stability of the output voltage, shielding, and thermal management. Results from a test of the magnetic field tolerance of the DC-DC converters are reported. System tests with pixel modules using many components of the future pixel barrel system are summarized. Finally first impressions from a pre-series of 200 DC-DC converters are presented.

KEYWORDS: Particle tracking detectors; Voltage distributions; Si microstrip and pad detectors

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1 The CMS Phase-1 pixel upgrade

The CMS detector [1], one of the two multi-purpose detectors at the Large Hadron Collider (LHC) at CERN, Geneva, features as its innermost component a silicon pixel detector. This subdetector was developed for an instantaneous luminosity of $1 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and has operated with excellent performance during the first run of the LHC (2010–2012). During the coming years, however, the performance of the LHC will be improved in steps, and it is expected that an instantaneous luminosity of around $2 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ will be reached shortly after the Long Shutdown 2, scheduled for 2018. Depending on the bunch spacing, the number of overlapping interactions per bunch crossing (referred to as pile-up) will increase to 50 (25 ns bunch crossing time) or 100 (50 ns bunch crossing time). This leads to an increase in track density and hit rates, with hit rates of up to $600\,\mathrm{MHz/cm}^2$ in the worst case in the innermost barrel layer of the pixel detector. Under such conditions, the inefficiency in the readout chip would increase dramatically, from its current value of up to 4% to up to 16%, or even 50%, for bunch crossing intervals of 25 and 50 ns, respectively. The CMS pixel detector will therefore need to be exchanged during the technical stop 2016/2017 [2].

The new pixel detector will be improved in many respects, including a new readout chip with much smaller inefficiency, a faster readout, a reduction of the material budget by moving to an evaporative CO_2 cooling system and by relocating electrical boards out of the sensitive tracker volume, and a smaller radius of the innermost barrel layer. To achieve 4-hit coverage over the whole acceptance, and consequently more robust tracking, higher track efficiency and lower fake rates, the number of detection layers will be increased, from the current three layers in the barrel part to four

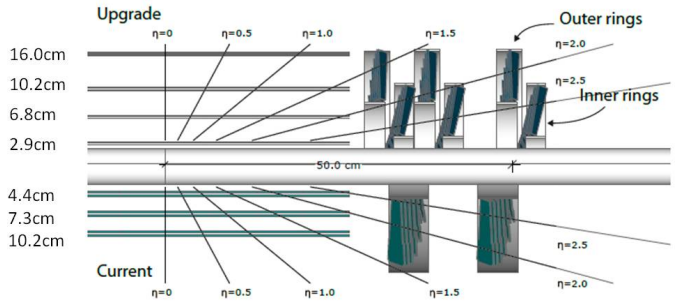

Figure 1. Layout of the present (bottom) and upgraded (top) pixel detector, in $r-z$ view. Here r represents the radial coordinate and z the coordinate along the beam axis. The pseudorapidity η is defined as $\eta = -\ln(\tan(\theta/2))$, with the polar angle θ measured with respect to the beam direction.

layers, and from the current two disks per side to three disks per side (figure 1). This leads to an increase of the channel count by a factor of 1.9 with respect to the present detector. Since front-end power consumption and supply voltages will not change, this translates directly into an increase in the supply current by the same factor. Consequently, power losses ($P_{loss} = R_{cable} \cdot I^2$ with I being the current and R_{cable} the cable resistance) on the 50 m long supply cables that link the detector with the power supplies will increase by a factor of $1.9^2 = 3.6$. The required total power cannot be delivered by the present power supplies, and the heat load on the cables would probably also surpass the tolerable limit. Since a significant addition of more cables is technically excluded and the installation and commissioning of new power supplies is not feasible within a winter technical stop, the pixel detector will feature a DC-DC conversion powering scheme, with step-down converters of the "buck" topology installed on the pixel service structures, approximately 1 m away from the pixel modules and outside the sensitive tracker region.

2 DC-DC buck converters

Step-down DC-DC converters allow the power, $P = V \cdot I$, to be delivered at a higher voltage, V, but with lower current, I: $P = (rV) \cdot (I/r)$. The factor $r = V_{in}/V_{out}$ is called the conversion ratio. Cable losses on the input side of the DC-DC converter are thereby reduced by a factor r^2.

DC-DC converters can be realized in a variety of topologies. For the pixel Phase-1 upgrade, the buck topology has been chosen, as it leads to relatively compact devices, whilst at the same time delivering large currents with high efficiency.

A simplified schematic of a buck converter is shown in figure 2. Two MOSFET transistors, T_1 and T_2, act as switches. During a period, t_{on}, the transistor T_1 is closed and T_2 is open; during period $T - t_{on}$ the transistor T_2 is closed and T_1 is open. The overall period, T, is linked to the switching frequency, f_s, as $T = 1/f_s$. In this way the load is periodically connected to and disconnected from the power supply. An inductor with inductance L acts as energy buffer, allowing a direct current to be supplied to the load. Filter networks at the input and output bypass AC components.

For an ideal, lossless DC-DC converter, the conversion ratio is linked to the duty cycle, $D = t_{on}/T$, as $r = 1/D$.

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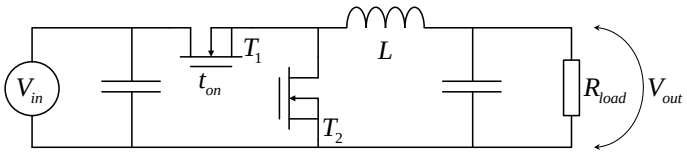

Figure 2. Simplified schematic of a buck converter. The regulation circuit and control logic are not shown.

3 Power system layout and implementation of DC-DC converters

The DC-DC converters in the Phase-1 pixel detector will receive an input voltage of 10 V, and deliver output voltages of either 2.4 V, required for the analog part of the readout chip (ROC), or 3.0 V, for the digital part of the ROC. Losses on supply cables are thus reduced by a factor of about ten. Each pair of DC-DC converters delivers power to between one and four pixel modules, depending on the layer/disk in which the modules are located, as the digital power of the ROC increases with hit rate, and is thus larger at smaller radii. The maximum analog current per converter amounts to 1.7 A, while the maximum digital current per converter is 2.4 A.

The DC-DC converters will be installed on the service structures of the pixel detector, on the supply tube for the barrel part (BPIX) and inside the service cylinder for the forward part (FPIX). For BPIX, the DC-DC converters will be located at the far end of these structures, at a distance of between 1 and 2 m from the pixel modules, as visible on the left of figure 3. This corresponds to a pseudorapidity, η, of about 4, which is outside of the sensitive tracker region. The material budget of the DC-DC converters is therefore not relevant to the tracker performance. Due to the large distance between converters and pixel modules a potential electro-magnetic interference is not a concern.

In BPIX, DC-DC converters are operated on a bus board, a PCB that carries 26 DC-DC converters. One such board will be located in each slot of the supply tube, as visible on the right side of figure 3. DC-DC converters are arranged in two rows, such that the converters within one pair (delivering the analog and digital voltage to the same pixel modules) are sitting side by side. Six or seven pairs of converters are powered by one power supply unit through one cable (through two independent voltage sources and cable conductors), and therefore each bus board is connected to two power cables. Currents of typically 45 A have to be transferred to the detector per slot. The heat load per slot due to the limited efficiency of the DC-DC converters amounts to about 40 W, requiring efficient cooling. The CO_2 pipes that deliver coolant to the pixel detector are used to cool the DC-DC converters and other electronic components.

In FPIX, four pairs of DC-DC converters will be mounted on "mount boards", inside the service cylinder, at a distance of $0.5 - 1.5$ m from the FPIX modules. Each mount board receives power from one power supply unit, and 14 pixel modules are powered from each mount board. Cooling will be provided in a similar way as for BPIX.

In total, 1184 DC-DC converters will be installed, 832 for BPIX and 384 for FPIX.

DC-DC converters for the pixel upgrade have to obey the severe space limitations, in particular in the supply tube slots, and be sufficiently radiation tolerant, with total ionizing doses (TID) of about 120 kGy and 1-MeV equivalent fluences of $2.3 \cdot 10^{14}\,\mathrm{n}_{eq}/\mathrm{cm}^2$ expected over the lifetime of the

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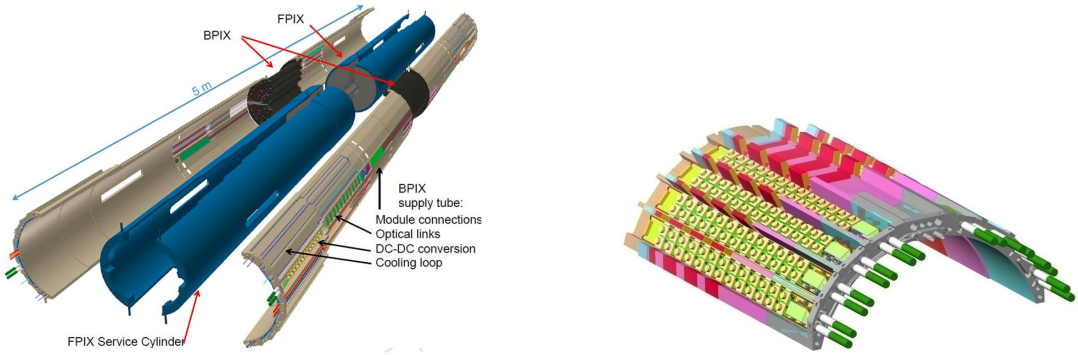

Figure 3. Left: exploded view of the CMS Phase-1 pixel detector. The barrel is drawn in black and is labelled "BPIX", while the forward disks are drawn in dark grey and are labelled "FPIX". The FPIX service cylinders are shown in blue, and the BPIX supply tube is pictured in light grey. For illustration, one slot of the supply tube is populated with electronic components, including the DC-DC converters, labelled "DC-DC conversion". Right: CAD-drawing of the BPIX supply tube end region, fully equipped with bus boards and DC-DC converters.

Phase-1 project (assuming 500 fb^{-1} of integrated luminosity). In addition, the DC-DC converters must work inside the 3.8 T magnetic field provided by the CMS solenoid.

4 DC-DC converter development for the Phase-1 pixel detector

4.1 Buck converter prototypes

DC-DC converters for the pixel project have been under development since 2008 ([3, 4] and references therein). The most recent prototype, named PIX_V10, is shown in figure 4. The PCB consists of two copper layers, and has a footprint of 2.8 x 1.7 cm^2. The boards convert the input voltage (nominally 10 V) to 2.4 or 3.0 V, as mentioned above. The switching frequency is 1.5 MHz. The inductor is realized as a toroid with a plastic core, providing an inductance of about 450 nH. Noise filters consisting of two capacitors (typically 20 μF each) and one inductor (12 nH) in pi-configuration are mounted at the input and output, respectively. The measurements shown in the following have been obtained with PIX_V9, which is identical to V10 aside from a subtle difference in the noise filter and the thermal contact of the shield, which was improved for V10.

The power transistors are located inside an ASIC, together with drivers, regulators, a band gap reference, a regulation circuit based on Pulse Width Modulation, logic blocks, and protection features handled by a state machine. The ASIC is developed by CERN PH-ESE [5]. The newest version, FEAST1, is presently under study by the designers. In the PIX_V9 and PIX_V10 converters described in this paper, the most recent accessible version, AMIS5, has been used. The chips are fabricated in a radiation tolerant 0.35 μm CMOS process. The AMIS5 ASIC is specified for currents of up to 4 A and input voltages between 5 V and 10 V. Output voltages between 1.2 V and 4.0 V and switching frequencies between 1.0 MHz and 3.5 MHz can be configured through external resistors. The chip outputs a status signal and can be switched on and off remotely.

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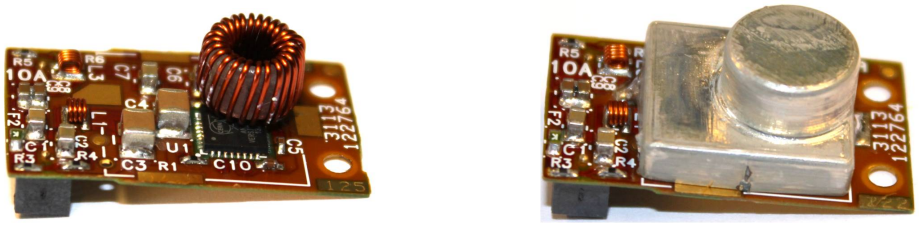

Figure 4. Photographs of a PIX_V10 DC-DC converter, without (left) and with (right) the shield attached.

Part of the converter, including the chip and the coil, is covered by an electro-magnetic shield. The shield is made of a 300 μm plastic core, galvanically coated with a 30 μm thick layer of copper. A 1 μm thick tin layer, deposited by electroless plating, improves solderability. The shield serves three purposes: it shields the environment from electro-magnetic emissions by the coil, it reduces the coupling of noise from (mainly) the coil into the pi-filters, and it serves as a cooling contact for the coil. The weight of the board, including the shield filled with heat conductive paste, is approximately 3 g.

4.2 Efficiency

The efficiency is one of the most important properties of a DC-DC converter. Unavoidable inefficiencies arise mainly from Ohmic losses in the coil, the power transistors and the passives, switching losses, and driving losses. The mean efficiency from five PIX_V9 converters with an output voltage of 2.5 V, fabricated in-house, is shown in figure 5, left. With efficiencies of 78-80% for the relevant input voltage of 10 V and output currents of 1-3 A, the efficiency is adequate. Due to the lower conversion ratio, the efficiency of 3.0 V converters is slightly higher, 80-82% in the same phase space. The right plot in figure 5 shows the standard deviation of the efficiency in per cent. The efficiency is uniform, with a typical spread of only 0.3%.

For the measurements leading to the above numbers the converters were screwed to a cooling block, which was kept at +20°C. The efficiency increases for lower temperature, mainly due to the temperature dependence of the resistance of the inductor. A linear dependency with a slope of -0.046%/K has been measured. In the experiment, where the cooling blocks will be kept at -20°C, the efficiency will thus be 2% higher.

4.3 Stability of the output voltage

It is crucial that the voltage delivered to the pixel modules stays within the allowed range, as too high voltages pose a risk to the ROCs, while for too low voltages the ROCs do not work properly. Since the DC-DC converters do not feature remote sensing, considerable voltage drops (depending on the load) arise between the DC-DC converters and the pixel modules, as large currents have to be transferred over a distance of up to 2 m. These drops have been calculated and have already partly been verified on prototype bus boards and other prototypes of the powering chain. The remaining tolerable voltage variation for the DC-DC converters amounts to about 280 mV.

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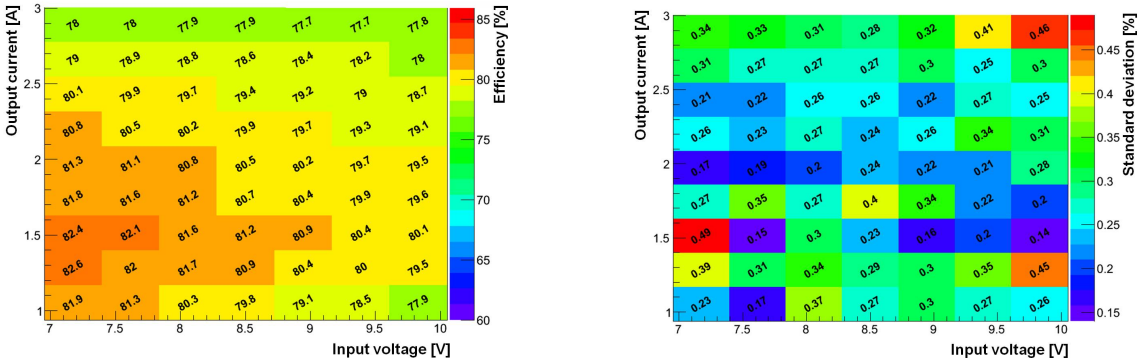

Figure 5. Mean efficiency (left) and standard deviation of the efficiency (right), measured on five PIX_V9 DC-DC converters with 2.5 V output voltage.

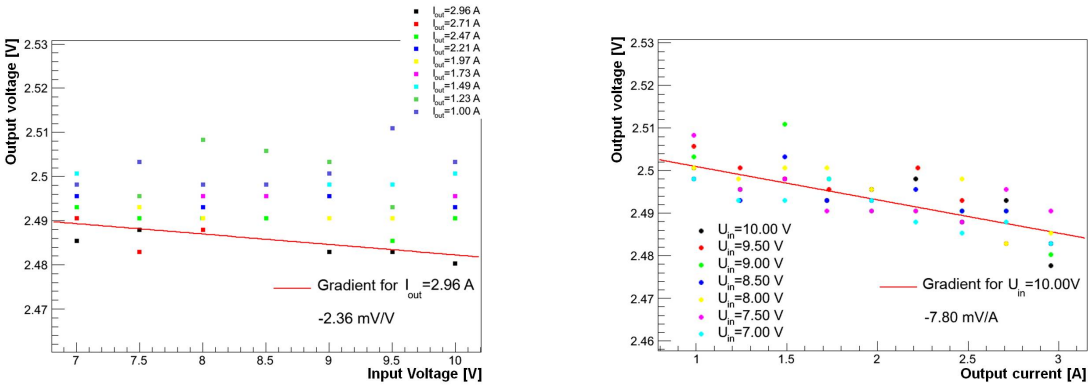

Figure 6. Line regulation (left) and load regulation (right) of a PIX_V9 DC-DC converter with 2.5 V output voltage. The red lines represent linear fits.

The standard deviation of the output voltage, measured on a limited sample of five PIX_V9 converters, amounts to about 10 mV. Allowing for three standard deviations, a spread of 30 mV can be expected. In addition, the output voltage deviated on average by 33 mV from the nominal.

The line regulation, the dependence of the output voltage on the input voltage, is shown for one converter in figure 6, left. The line regulation is very good and for an output current of 3 A the linear fit results in a mean slope (using five converters) of −2.46 mV/V. Assuming that input voltages between 7 and 10 V will be used (a very conservative assumption), a variation of below 8 mV will arise due to imperfect line regulation.

Figure 6, right, shows the load regulation, the dependence of the output voltage on the output current, for one DC-DC converter. The mean slope (using five converters) from a linear fit to the data with an input voltage of 10 V amounts to −8.9 mV/A. For a change of the current between 0 and 3 A, the variation is therefore 27 mV.

Since the output voltage is regulated through comparison with a bandgap reference, which is not perfectly stable with temperature, the output voltage depends also on the temperature of the converter. This has been measured for one converter and a slope of 0.69 mV/K was observed. For

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a temperature variation of 40 K between the final operating temperature and room temperature a variation of 28 mV is expected due to this effect.

A change in the output voltage of about 60 mV due to irradiation effects on the bandgap reference must also be expected, based on studies by the chip designers.

Adding up all effects linearly, which is very conservative as some of the effects will cancel another out, results in a variation of 185 mV and 230 mV for 2.5 V and 3.0 V converters, respectively, well within the allowed budget. The difference is mainly due to the temperature dependence, which is larger in 3.0 V converters, as a voltage divider with one on-chip resistor and one external resistor is used to set the output voltage. This will be changed in future versions.

4.4 Effectiveness of the shield

The main purpose of the shield is to reduce electro-magnetic emissions from the inductor, so that the performance of nearby electronic components (e.g. opto-hybrids) is not compromised. Measurements with a pick-up coil placed at a defined distance above the inductor or shield showed that the maximum emission (measured as a voltage) is reduced to about 5%, while the mean emission in a region of 4 cm x 4 cm around the inductor is reduced to 13%. The remaining emissions are considered negligible.

The shield also reduces coupling of electro-magnetic emissions from the coil (and possibly other components) into the parts of the pi-filters that are outside the shield: the inductor and the capacitors on the connector-side of the filters. Measurements of the conducted noise, propagating through the cables, have been performed on the input and output in Differential and Common Mode, using pick-up coils clamped around the cables. While the Differential Mode noise is not reduced significantly, the Common Mode noise at the converter's output is reduced from 6.9 μA to 1.9 μA, where the current is the quadratic sum of all noise peaks up to 30 MHz.

Finally, the shield is used as a cooling contact for the inductor, which is otherwise cooled only through its leads. The shield is soldered to the PCB at two locations, and heat is transferred through vias to the backside of the PCB, which features a large ground plane. For an output current of 3 A, the temperature of the coil, measured with a temperature sensor placed inside the coil, is reduced by about 15 K. Heat conductive paste (KP98 Keratherm) must be applied inside the shield. The thermal performance is considered adequate, with the inductor and chip package at temperatures of about 50 °C for thermal stabilization at room temperature. The over-temperature protection in future chip versions will set in at 120 °C. Nevertheless, more and larger solder pads, with more vias, have been implemented in the PIX_V10 PCB, to improve further the thermal management.

4.5 Magnetic field tolerance

The DC-DC converters have to work with high efficiency inside the 3.8 T magnetic field of CMS. Ferrite inductors would saturate, resulting in reduced efficiency or even complete failure. Due to the usage of an air-core inductor, no problems are expected. Nevertheless, several PIX_V9 DC-DC converters were operated in a 4 T NMR magnet at Forschungszentrum Jülich. The efficiency was measured and compared to laboratory measurements of the same converters, using exactly the same set-up. Since the measuring equipment had to stay outside the shielded magnet room, cables of 10 m length had to be used. It was verified that this did not introduce deviations with

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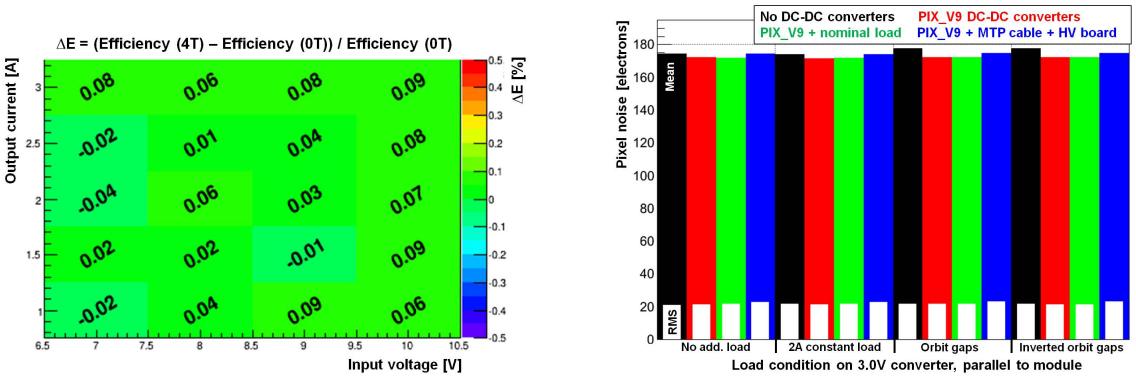

Figure 7. Left: Relative difference in efficiency inside and outside a 4 T magnetic field, for a PIX_V9 DC-DC converter. Right: Pixel noise measured in system tests. Black: without DC-DC converters; red: with PIX_V9 DC-DC converters; green: applying maximum load on the power supply and DC-DC converters not connected to the pixel module; blue: using the micro twisted-pair module cable (MTP cable) and high voltage (HV) board. Load conditions are explained in the text.

respect to standard measurement conditions. The converters could be operated in three orientations with respect to the field lines: field lines parallel to the long side ("horizontal", comparable to the situation inside CMS) or short side of the PCB plane, and field lines orthogonal to the PCB plane ("transverse"). The relative efficiency difference, ΔE, in horizontal orientation, defined as ΔE = (Efficiency (4 T)-Efficiency (0 T)) / Efficiency (0 T), is shown in figure 7. Differences are below 0.1%. In transverse orientation larger deviations, of up to 0.5%, have been observed. This difference between orientations was reproduced in the laboratory (without magnetic field) and is therefore, although not yet fully understood, considered unrelated to the magnetic field.

As a cross-check it has been verified that the usage of a ferrite-core inductor leads to a significant reduction of the efficiency.

The converter's noise emissions remained unchanged, and the behaviour during switch on/off was monitored on an oscilloscope and found to be identical to measurements without magnetic field.

4.6 System tests with pixel modules

System tests have been performed to rule out any degradation of the performance of the pixel modules due to the usage of DC-DC converters. For example, remaining noise emissions from the converters could increase the noise of the pixel modules. Large, fast load changes are another source of concern. These arise from the orbit gaps (3 μs every 89 μs) in the LHC beam structure, during which the digital current consumption drops, as no hits are registered. System tests have been performed with present pixel modules, as modules with the new ROC are not yet available. The powering chain consisted of the pixel power supply, modified to be compatible with DC-DC converters (exactly as planned for the final system), a pixel multi-service cable of original length, eight PIX_V9 DC-DC converters on a prototype bus board (of which one pair is used to power the pixel module), a prototype of the future pixel module cable (with micro twisted-pair conductors), and a prototype of a flex board that will be used in the final system to deliver the bias voltage to the modules. The noise of the pixel modules has been extracted as the width of the

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s-curve, a standard method. Figure 7, right, shows the mean noise of all pixels as colored bars, and the standard deviation as white bars. Measurements without converters (black) are compared to different configurations: using PIX_V9 converters (red), applying in addition realistic loads to the power supply and the converters that are not powering the tested pixel module (green), and using the micro twisted-pair cable and high voltage board (blue) - this last configuration is the most realistic test performed so far. The converter supplying the digital voltage to the pixel module has, in addition, been stressed with a constant load of 2 A (resembling a situation with several modules connected to one converter), a changing load as expected from the orbit gaps, and a changing load with inverted time structure (as expected for a pilot beam with only a few bunches filled). Under all tested conditions, the noise of the pixel modules was not increased significantly with respect to measurements without DC-DC converters.

4.7 DC-DC converter pre-series

A pre-series of 200 PIX_V10 DC-DC converters was produced, with the aim of qualifying the production companies. The inductors and shields were produced in industry. The component placement was also done by industry, including soldering of the non-SMD components (the inductor and the shield). The heat conductive paste was also applied at the company. All devices were subjected to an acceptance test. The yield was 99%, with one chip not functioning and one inductor not soldered correctly. A fraction of the devices were actively thermo-cycled between $-20°$C and $+20°$C, and some even between $-30°$C and $+50°$C, and no breakdowns were observed. More work is needed to fully exploit this large sample of converters and to assess its quality and uniformity.

5 Summary and outlook

The CMS collaboration has chosen a DC-DC conversion powering scheme for its Phase-1 pixel upgrade. DC-DC converter prototypes based on the AMIS5 ASIC designed by CERN have been developed and extensively studied. The electrical and thermal performance was found to be adequate. Boards with the next version of the chip, FEAST1, are under development. Mass production of 1800 DC-DC converters is planned for the second half of 2014.

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