The Read-Out Driver (ROD) card for the ATLAS experiment: commissioning for the IBL detector and upgrade studies for the Pixel Layers 1 and 2

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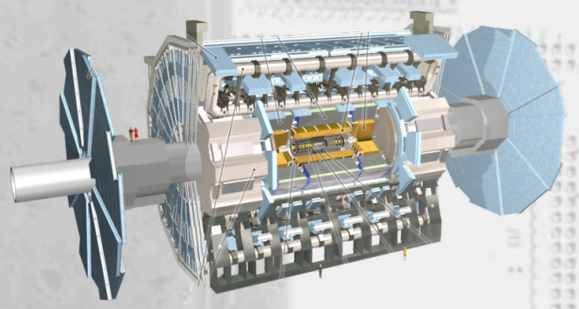
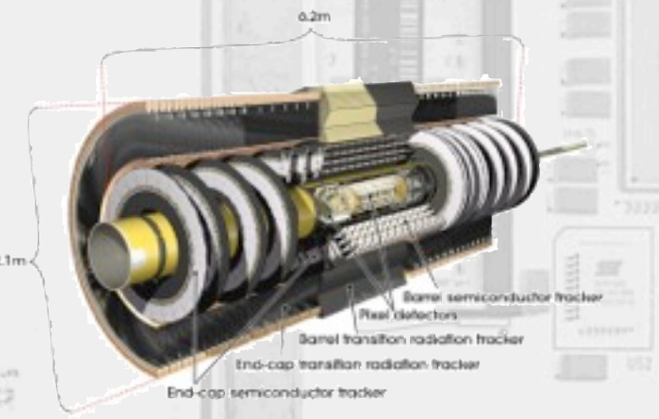
Session B2 : Systems, Planning, installation, commissioning and running experience

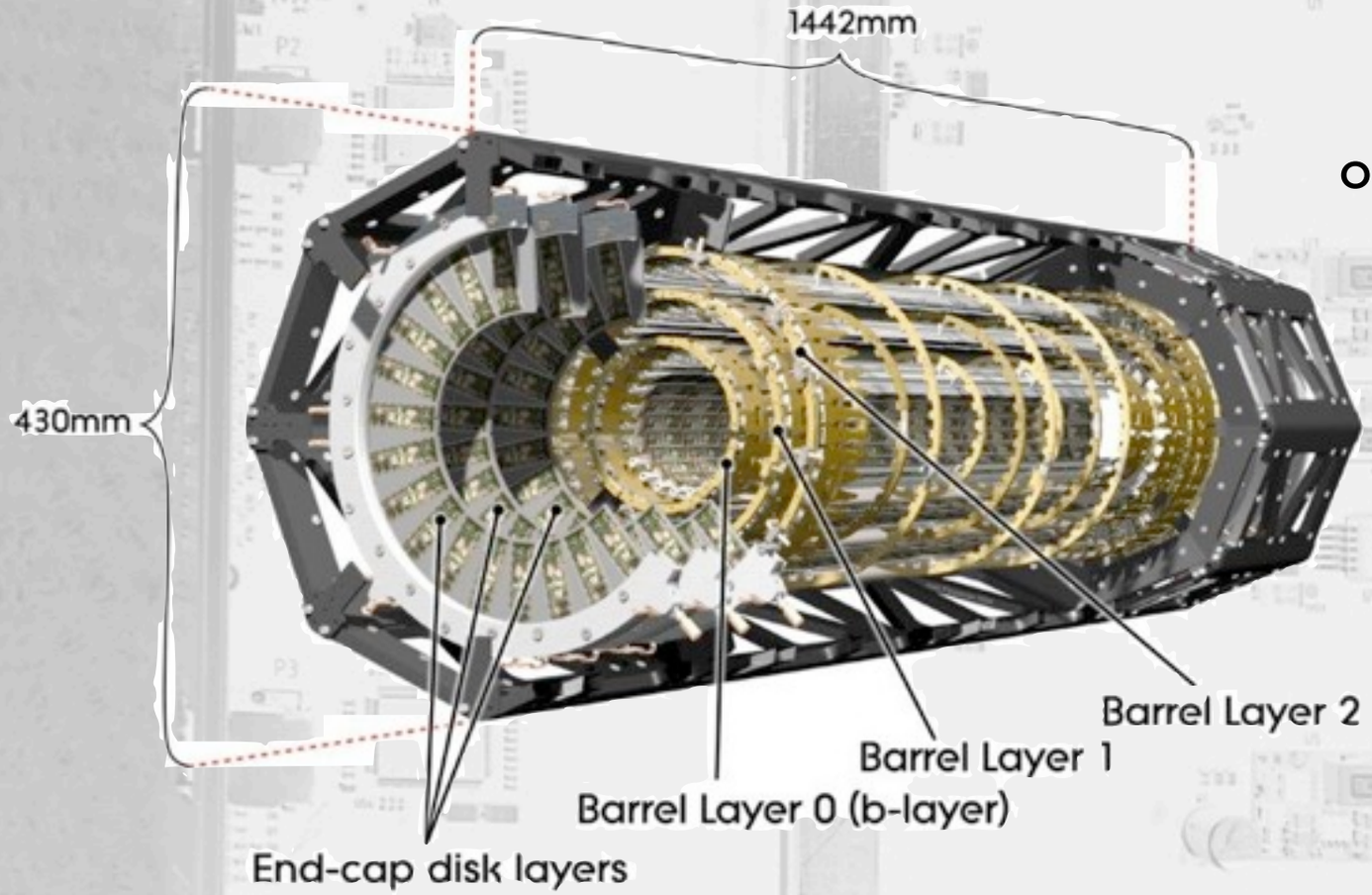
Atlas Pixel Detector Overview





innermost detector: tracking and vertexing
3 barrel layers - b-layer closer the beam pipe
(<r>=5cm)
8 10^7 pixel in total (50 um x 400 um)

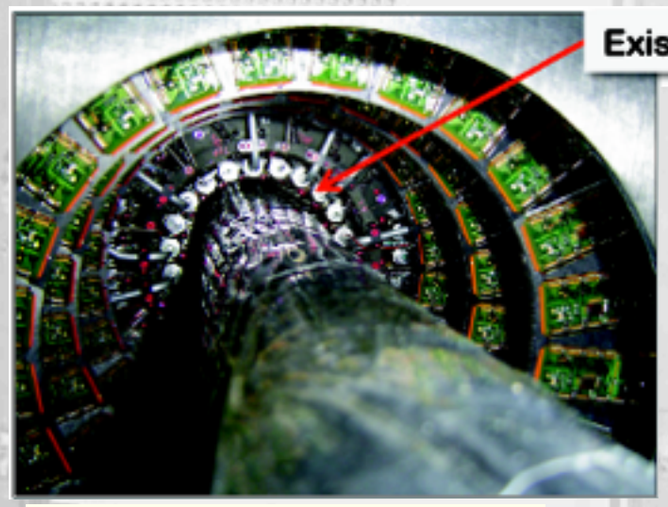
front-end chip : FE-I3 (2880 channels x chip)
basic unit: module (sensitive region coupled with 16 FE-I3)
1774 modules in total

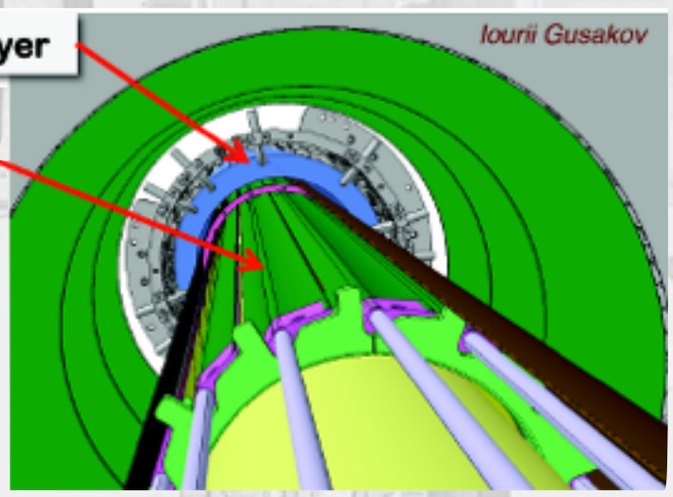


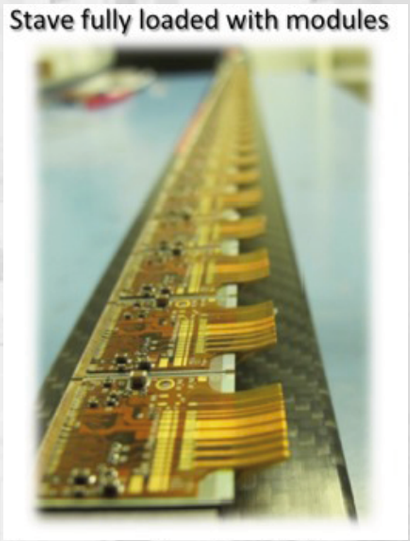
one Module Control Chip (MCC) x module
different readout schemes:
b-layer: 2 link @ 80 MB/s (160 Mb/s)
layer 1: 1 link @ 80 Mb/s
layer 2: 1 link @ 40 Mb/s

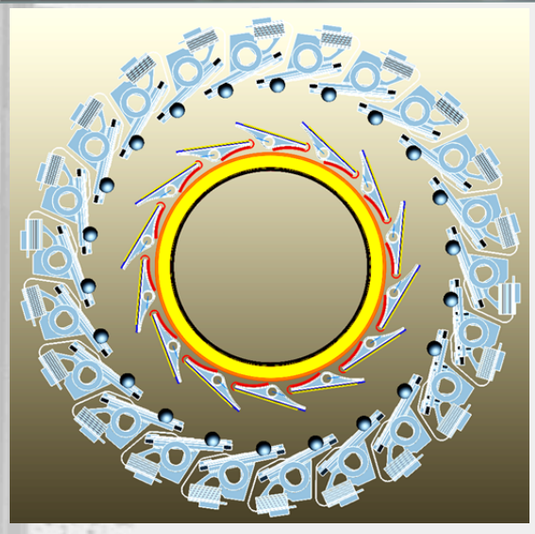
Each off-detector readout unit
handles up to 160 MB/s
(2 link @ full speed)
(1 S-Link)

Pixel Detector Upgrade: Inner Barrel Layer (IBL)

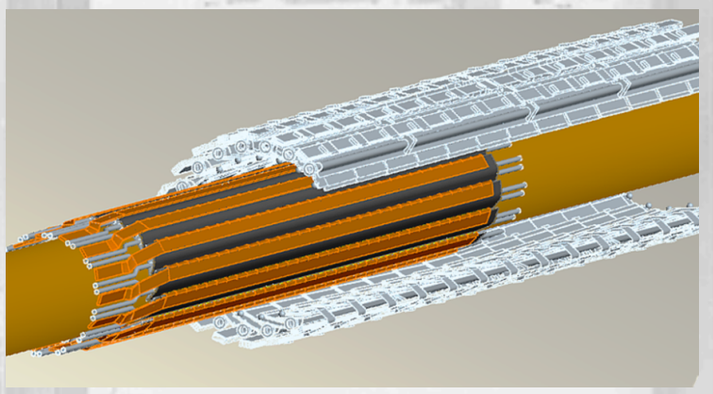








Number of pixels 6.02×10^6
Pixel size : 50 x 250 um
<R> = 33 mm
|Z| < 33.2 cm
14 Staves
224 Modules



Major Goals:

- strengthen the tracking capability by increasing both redundancy and precision;
- preserve the performances of the Pixel Detector for effects due to the increased luminosity expected after LHC upgrades (greater pile-up and radiation doses).

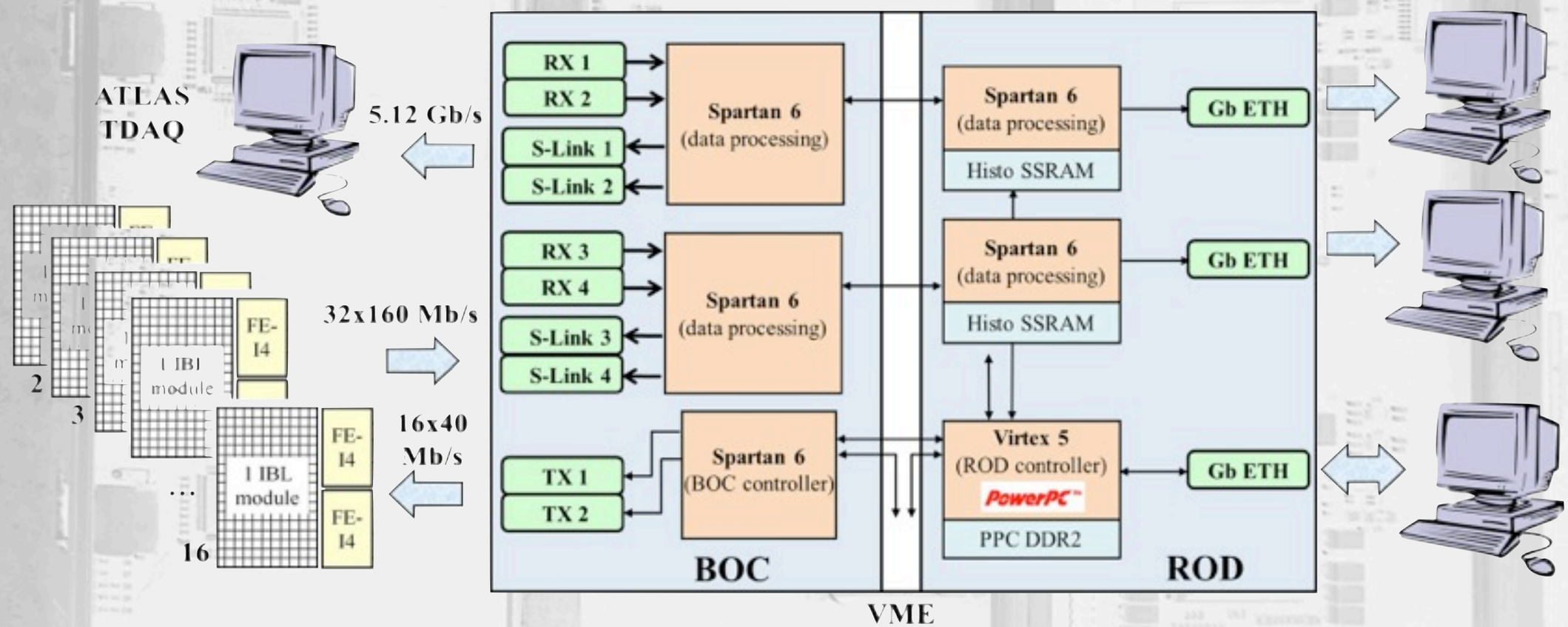
Installation during LHC long shutdown 1
(ends in June 2014)

New Read-Out electronics for IBL

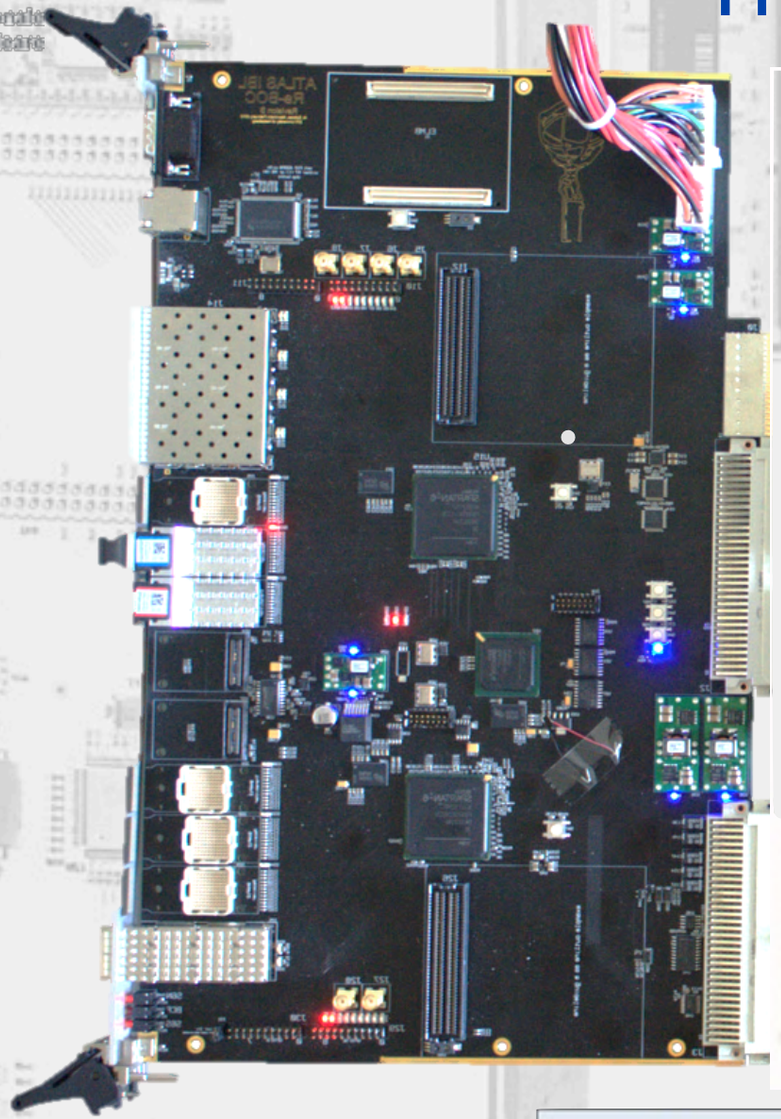
A new front-end ASIC, called FE-I4 has been designed to face the larger occupancy as well as to manage the increased bandwidth expected for IBL.

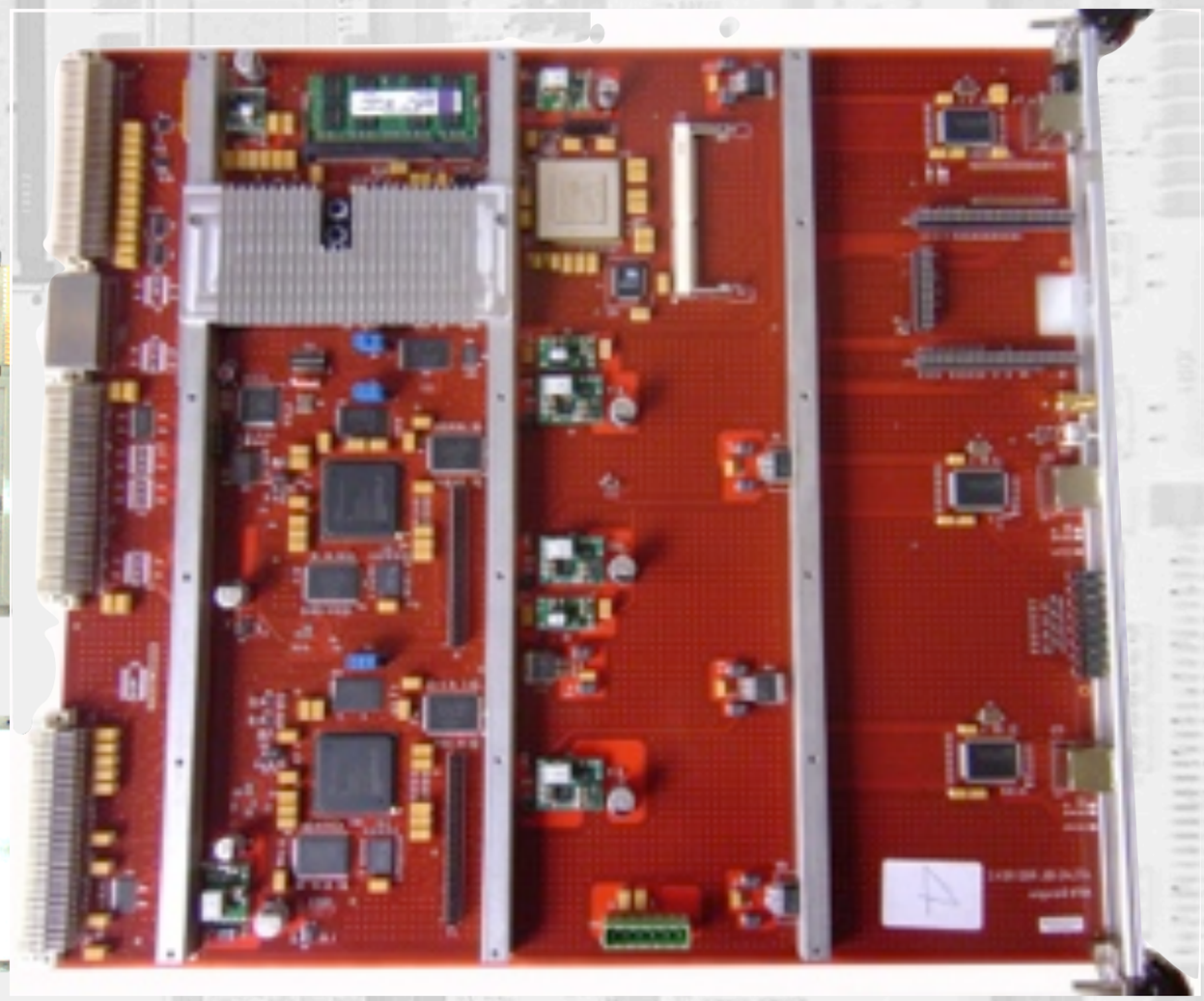
New off-detector electronics have been foreseen as well, in order to overcome limitations in the current system; it consists of two 9U-VME cards: Back-of-Crate (BOC) and Read-Out Driver (ROD) respectively implementing optical I/O interface and data processing. Each card pair processes data received from 32 FE-I4 data links for a total I/O bandwidth of 5.12 Gb/s.

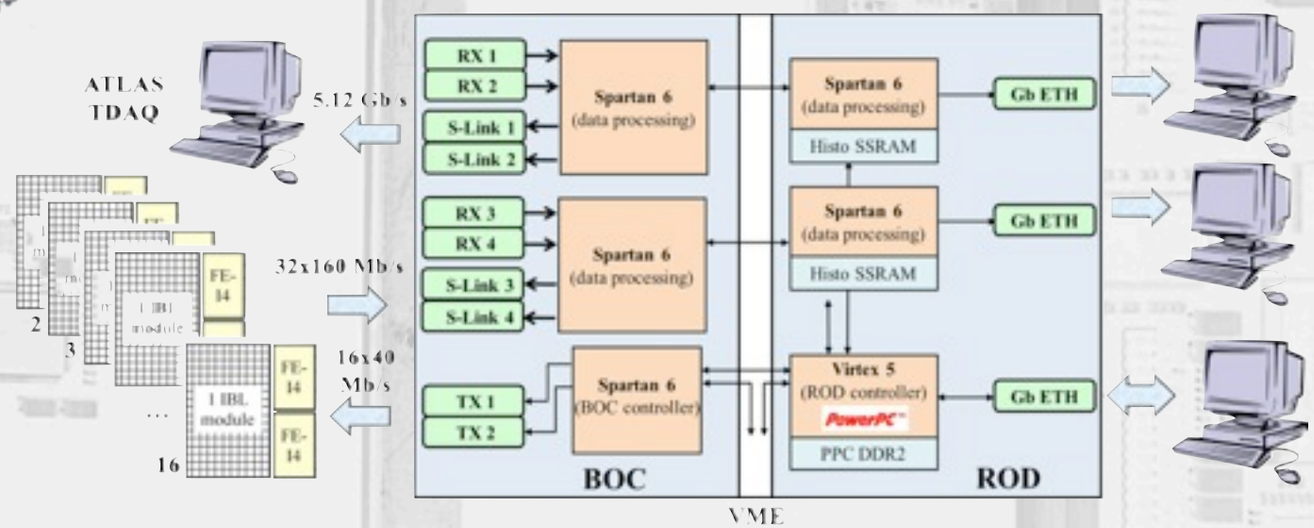
BOC-ROD Output through 4 S-Links per pair to drive the data out. Faster calibration link by using Gb Ethernet instead of the VME bus for data transfer.



The ROD-BOC

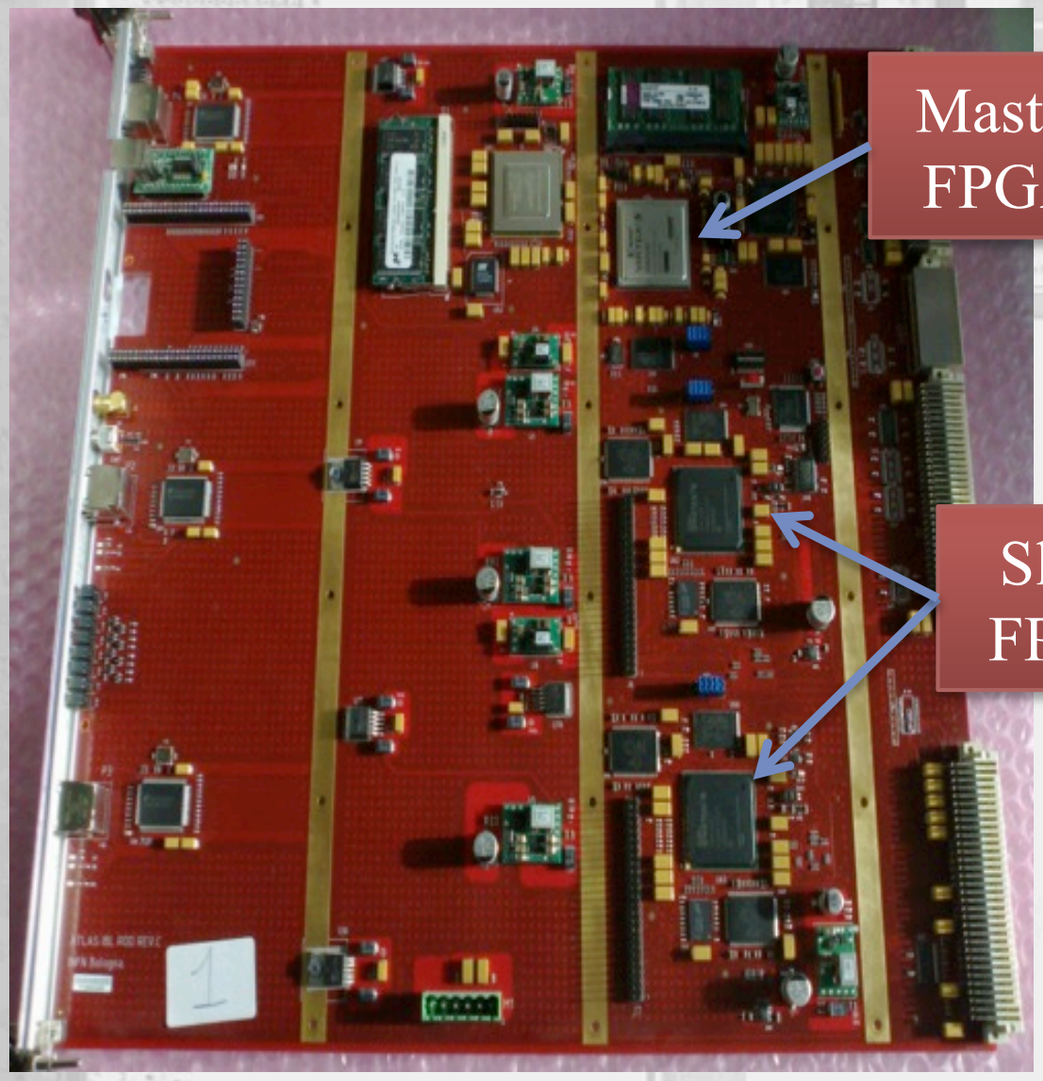






16 pair to be installed in total

the ReadOut Driver (ROD) card



rev C - february ’13 - 5 card - pre-production

Control:
commands to FE-I4 (configuration, triggers)
configure BOC

Data taking:
gathering of front-end output
event building

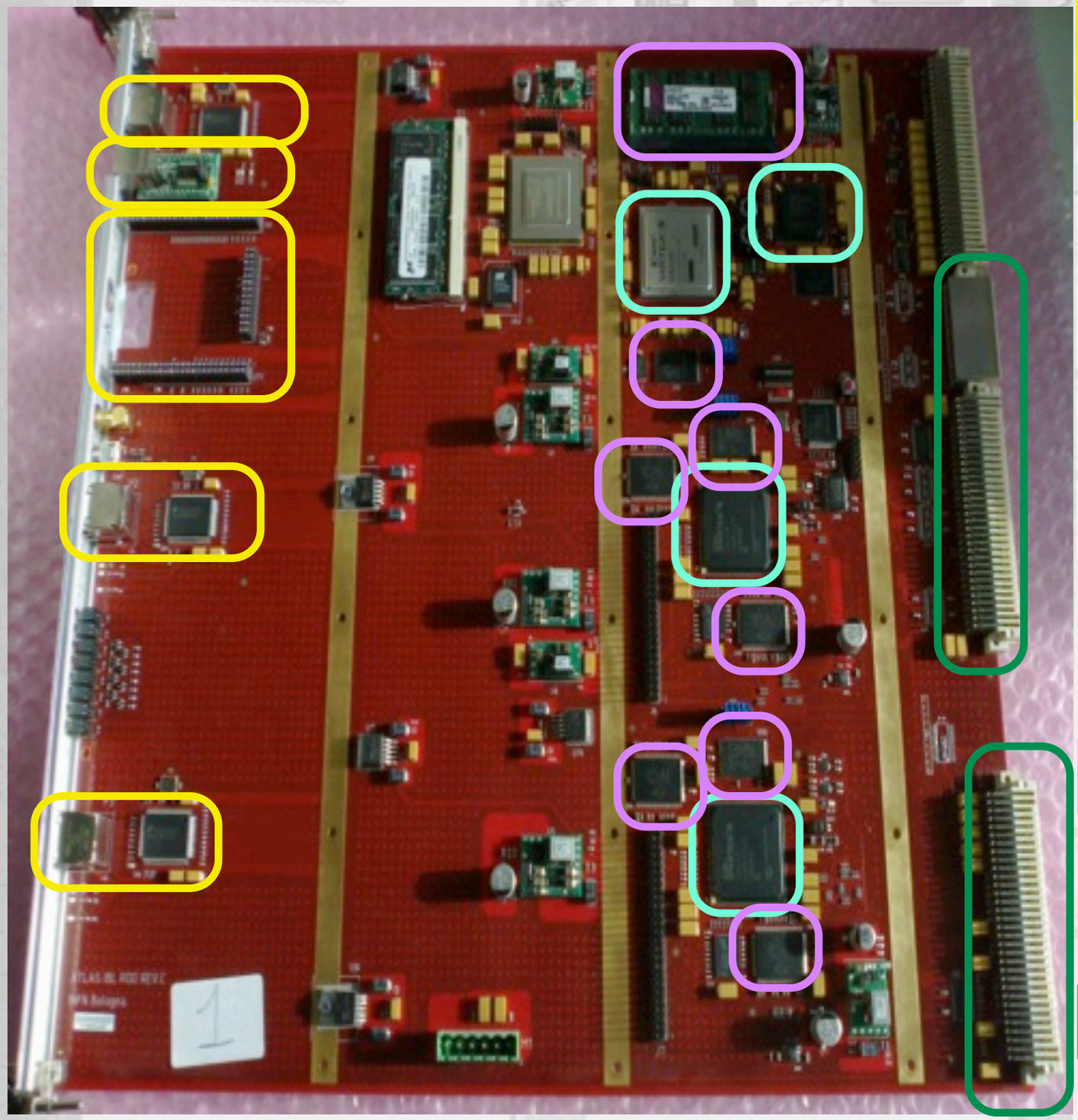
Detector calibration and monitoring:
Scan performing
histogramming

rev A - sept. ’11
3 cards
1st proto

rev B - february ’12
5 cards
distributed at labs

ROD - Hardware

14 layers PCB - 9U VME



Control, debug and interface with Calibration Farm/PC:

- 3 Gbit Ethernet Connectors:
  - 1 receiving config. from PC
  - 2 sending histos to PC farm
- 1 USB mezzanine
- 1 TTCrq mezzanine

Main Firmware components:

- 1 Spartan6 (Xil.) Prog. Res. Man.
- 1 Virtex5 (Xil.) Master: operation control (PowerPC)
- 2 Spartan6 (Xil.) Slaves: data processing (MicroBlaze)

Other components:

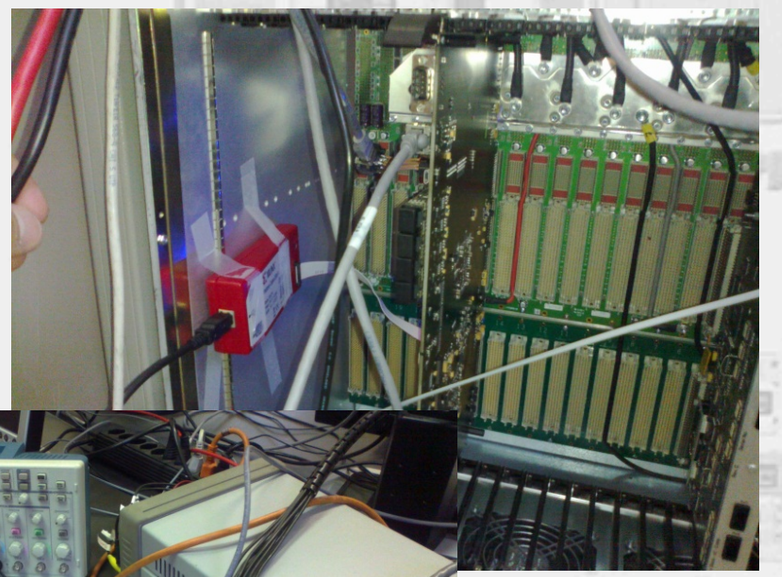
- 4 SSRAM (2 per Sp6)
- 1 Flash (Atmel) for the Vtx5
- 3 DDR2 (1 per each Sp6 + 1 Vtx5)

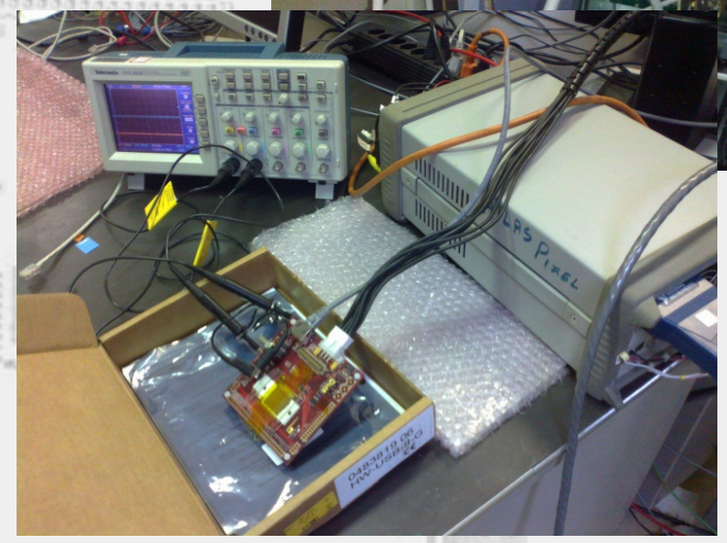
Interface with BOC (FE-I4&ROS):

- P0/P2/P3 connectors 40-80Mhz

ROD commissioning strategy

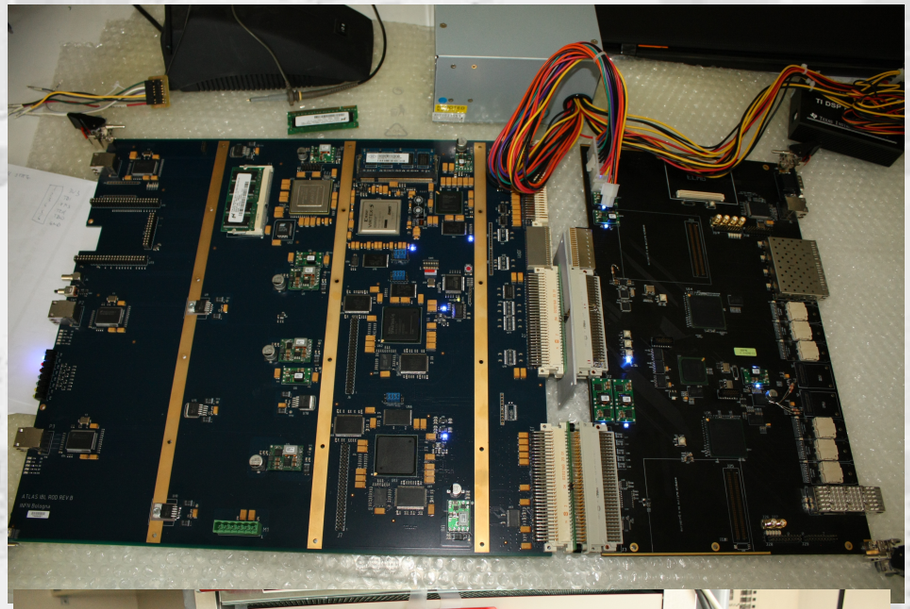
integration tests with FE-I4 at the Pixel lab (CERN)

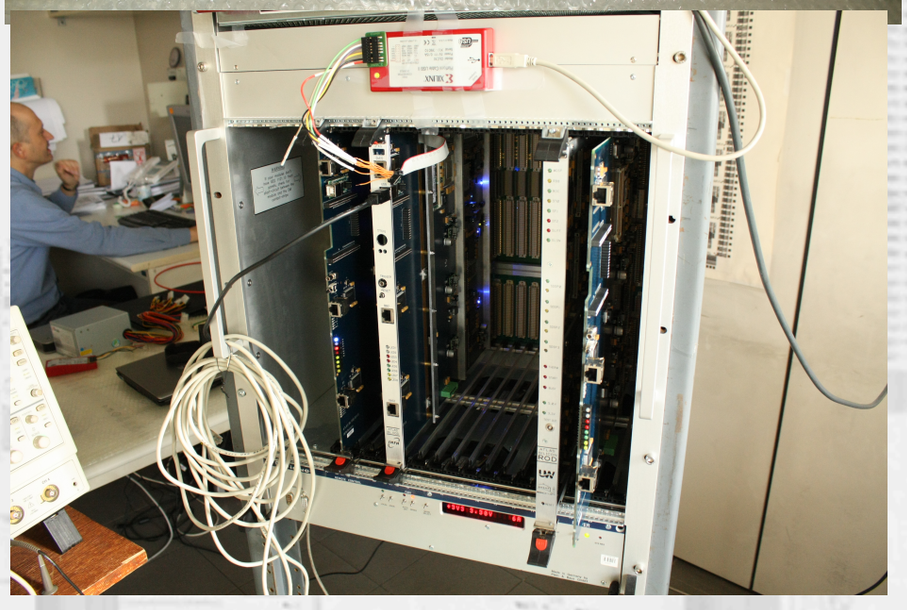




Many test stands have been assembled; different functionalities have been verified as well as distinctparts of firwares are developed based on local setups

BOC-ROD off-crate test





BOC-ROD on-crate test

6 labs with different setups:
CERN, Bologna, Wuppertal, Mannheim, Genova, Gottingen

ROD commissioning

test	status	comments
power supply	DONE	25.7 W with current fw
temperature	DONE	V5 < 42 C ; SP6 < 50 C
clock distribution	DONE	
interface with TIM	almost done	electrical test w. chipscope
interface with DDR2 and FLASH mem	DONE	
VME	DONE	
On-board and to BOC slow control Bus	DONE	
BOC -> ROD	DONE	96 lines (SSTL3 @ 80 MHz)
ROD -> BOC	ongoing	tested with full speed but not with S-Link protocol
interface with SRAM	almost done	stand alone @ 200 MHz (36 bit) full fw @ 140 MHz (32 bit)
Ethernet	DONE	3 gigabit links
V5 fw and sw upload from VME	DONE	
SP6 fw upload from VME	DONE	
SP6 sw upload from ETH	DONE	
Integration with FE-I4	well advanced	see next slides

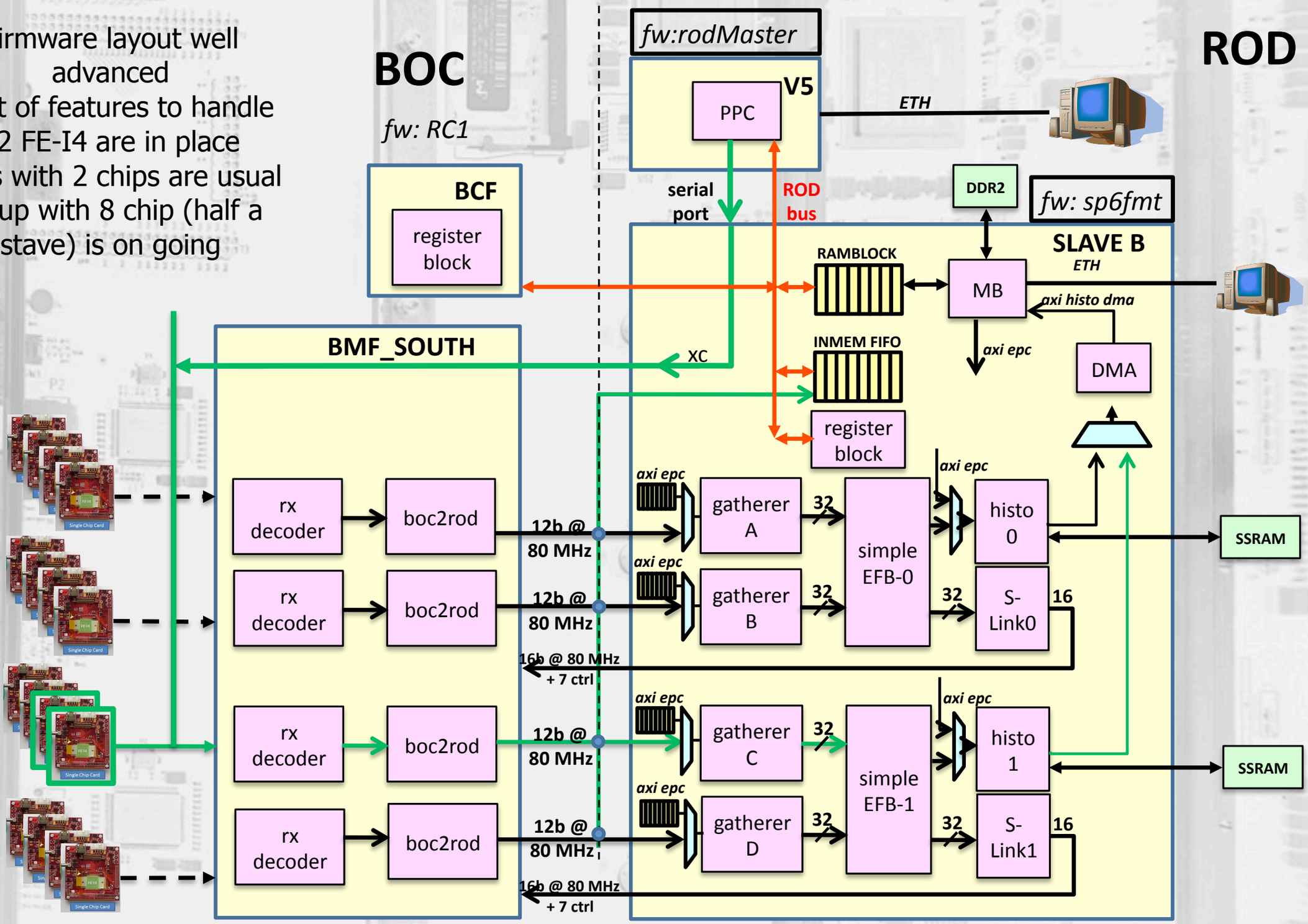
Example test #1 :BOC-ROD trasmission

Data are sent @ 80 Mb/s on the 96 bit-wide bus (SSTL3 logic)
Different phases of the sampling clocks
2 hour running per phase
good uniformity: same sampling windows for all 5 rev C cards

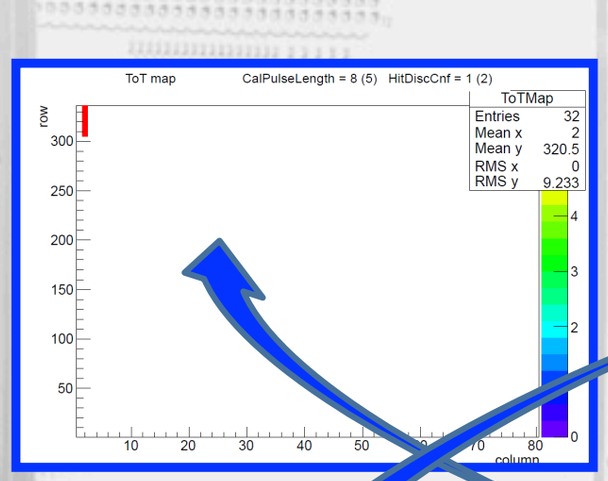
Phase (degrees)	Device	Status	Problems
0	SP6A	FAIL	Multiple errors on every bus
	SP6B	FAIL	Multiple errors on every bus
90	SP6A	FAIL	One error in 2 hours of test
	SP6B	OK	
180	SP6A	OK	
	SP6B	OK	
270	SP6A	OK	
	SP6B	OK	

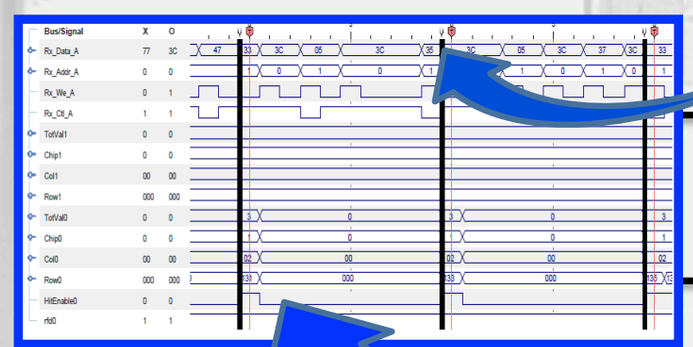
Example tests #2: Integration with FE-I4 (1)

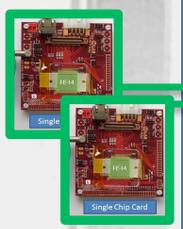
Firmware layout well advanced
Most of features to handle 32 FE-I4 are in place
Tests with 2 chips are usual
Setup with 8 chip (half a stave) is on going

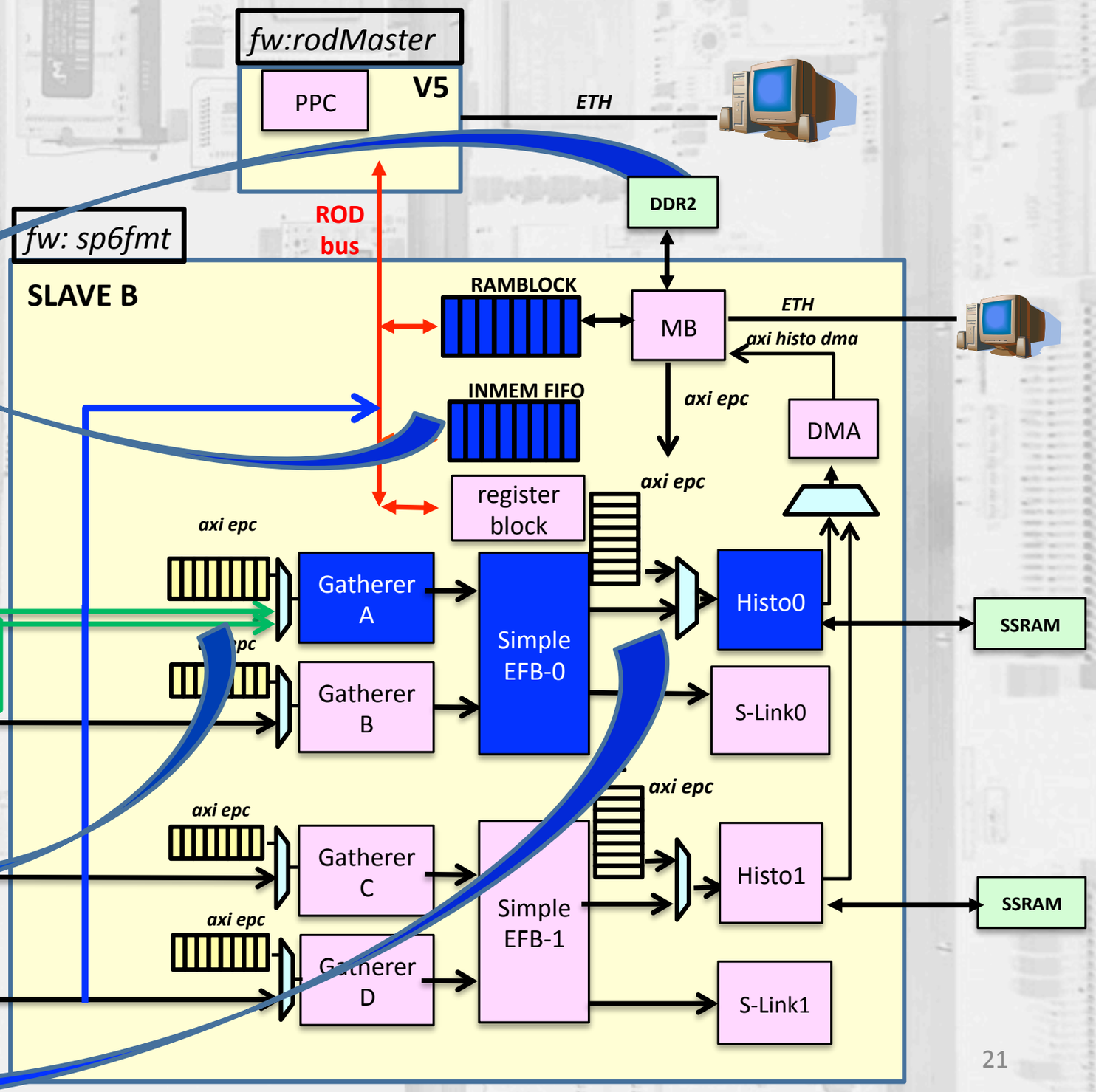


Example tests #2: Integration with FE-I4 (2)

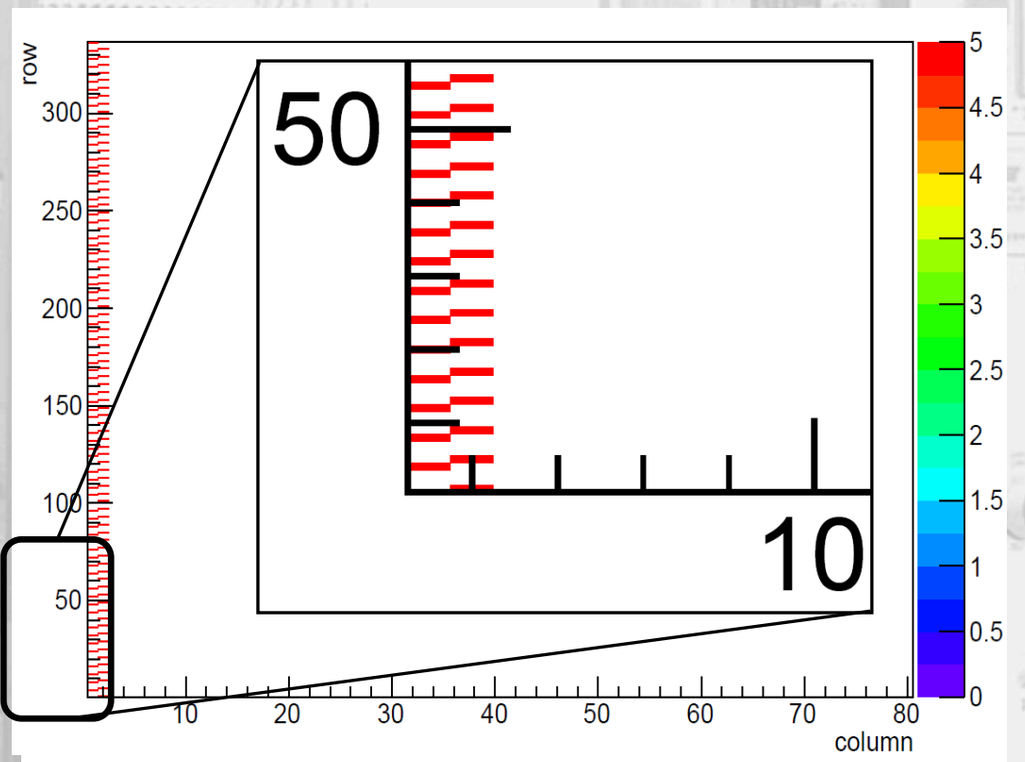


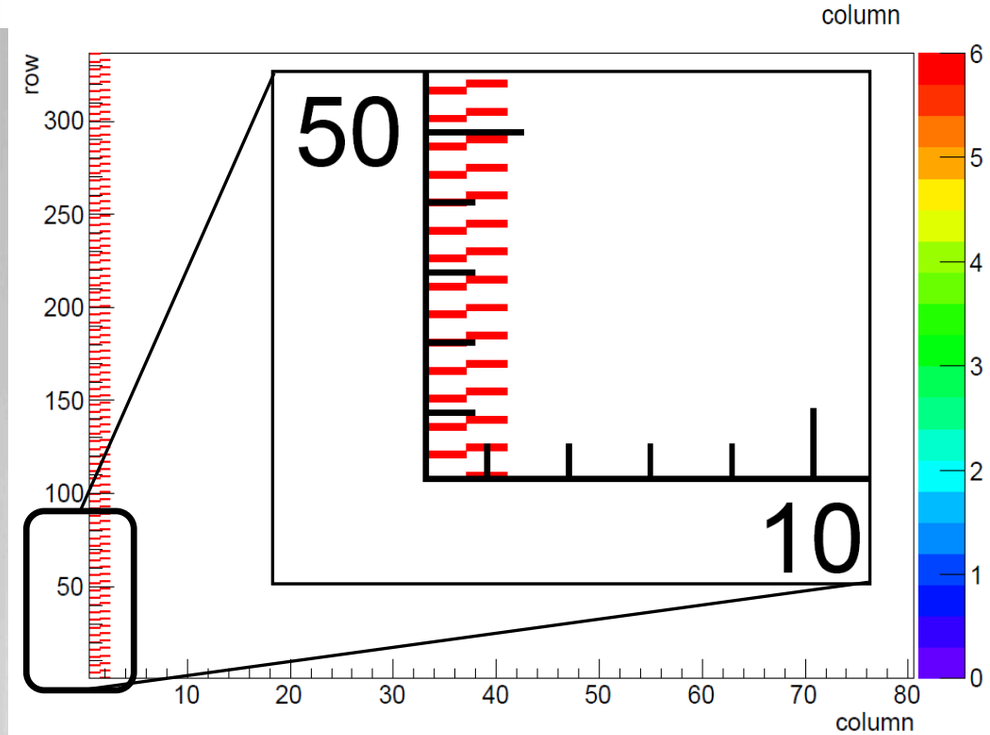






Example tests #2: Integration with FE-I4 (3)





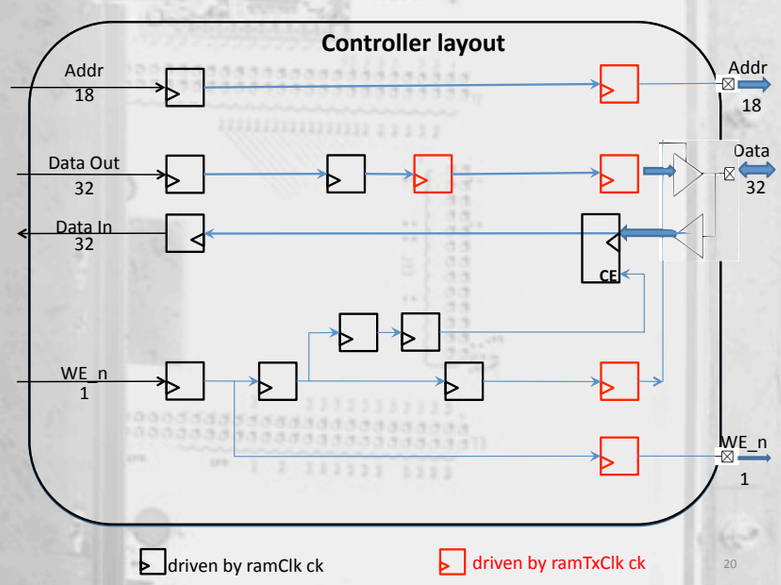
CHIP #0
¼ PixelMask
Cal Pulse Length = 5 BC
First Mask Stage

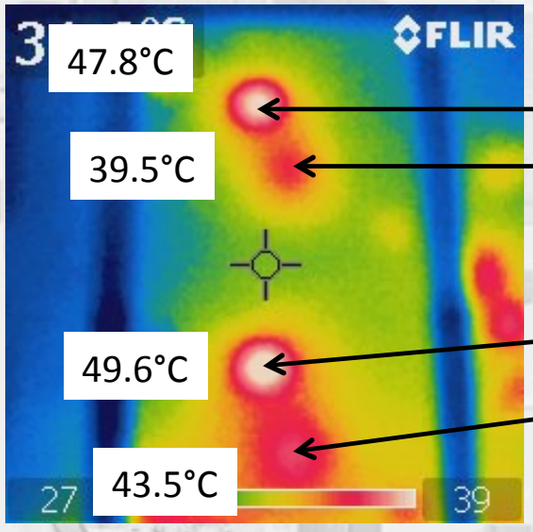
```
MPixNum 0 Hist 0,Chip 0, Odd_Col 1, Row 4, Result 0x100281: occ 1, tot 2, tot² 4
MPixNum 80 Hist 0,Chip 0, Odd_Col 1, Row 8, Result 0x100281: occ 1, tot 2, tot² 4
MPixNum 160 Hist 0,Chip 0, Odd_Col 1, Row 12, Result 0x100281: occ 1, tot 2, tot² 4
MPixNum 240 Hist 0,Chip 0, Odd_Col 1, Row 16, Result 0x100281: occ 1, tot 2, tot² 4
MPixNum 320 Hist 0,Chip 0, Odd_Col 1, Row 20, Result 0x100281: occ 1, tot 2, tot² 4
MPixNum 400 Hist 0,Chip 0, Odd_Col 1, Row 24, Result 0x100281: occ 1, tot 2, tot² 4
MPixNum 480 Hist 0,Chip 0, Odd_Col 1, Row 28, Result 0x100281: occ 1, tot 2, tot² 4
MPixNum 560 Hist 0,Chip 0, Odd_Col 1, Row 32, Result 0x100281: occ 1, tot 2, tot² 4
MPixNum 640 Hist 0,Chip 0, Odd_Col 1, Row 36, Result 0x100281: occ 1, tot 2, tot² 4
MPixNum 720 Hist 0,Chip 0, Odd_Col 1, Row 40, Result 0x100281: occ 1, tot 2, tot² 4
MPixNum 800 Hist 0,Chip 0, Odd_Col 1, Row 44, Result 0x100281: occ 1, tot 2, tot² 4
MPixNum 880 Hist 0,Chip 0, Odd_Col 1, Row 48, Result 0x100281: occ 1, tot 2, tot² 4
MPixNum 960 Hist 0,Chip 0, Odd_Col 1, Row 52, Result 0x100281: occ 1, tot 2, tot² 4
```

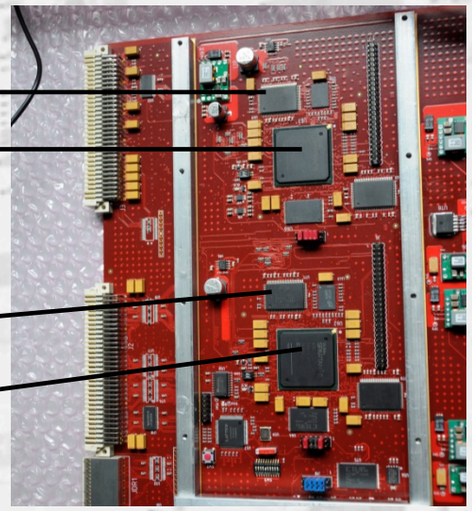
CHIP #1
¼ PixelMask
Cal Pulse Length = 6 BC
First Mask Stage

```
MPixNum 6720 Hist 0,Chip 1, Odd_Col 1, Row 4, Result 0x240381: occ 1, tot 3, tot² 9
MPixNum 6800 Hist 0,Chip 1, Odd_Col 1, Row 8, Result 0x240381: occ 1, tot 3, tot² 9
MPixNum 6880 Hist 0,Chip 1, Odd_Col 1, Row 12, Result 0x240381: occ 1, tot 3, tot² 9
MPixNum 6960 Hist 0,Chip 1, Odd_Col 1, Row 16, Result 0x240381: occ 1, tot 3, tot² 9
MPixNum 7040 Hist 0,Chip 1, Odd_Col 1, Row 20, Result 0x240381: occ 1, tot 3, tot² 9
MPixNum 7120 Hist 0,Chip 1, Odd_Col 1, Row 24, Result 0x240381: occ 1, tot 3, tot² 9
MPixNum 7200 Hist 0,Chip 1, Odd_Col 1, Row 28, Result 0x240381: occ 1, tot 3, tot² 9
MPixNum 7280 Hist 0,Chip 1, Odd_Col 1, Row 32, Result 0x240381: occ 1, tot 3, tot² 9
MPixNum 7360 Hist 0,Chip 1, Odd_Col 1, Row 36, Result 0x240381: occ 1, tot 3, tot² 9
MPixNum 7440 Hist 0,Chip 1, Odd_Col 1, Row 40, Result 0x240381: occ 1, tot 3, tot² 9
MPixNum 7520 Hist 0,Chip 1, Odd_Col 1, Row 44, Result 0x240381: occ 1, tot 3, tot² 9
MPixNum 7600 Hist 0,Chip 1, Odd_Col 1, Row 48, Result 0x240381: occ 1, tot 3, tot² 9
MPixNum 7680 Hist 0,Chip 1, Odd_Col 1, Row 52, Result 0x240381: occ 1, tot 3, tot² 9
```

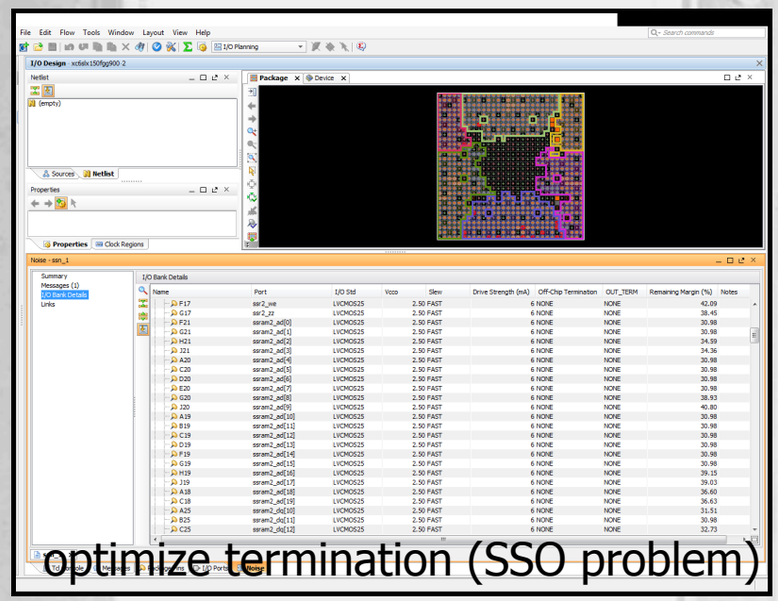
Example #3: Interface with SRAM for Histogramming





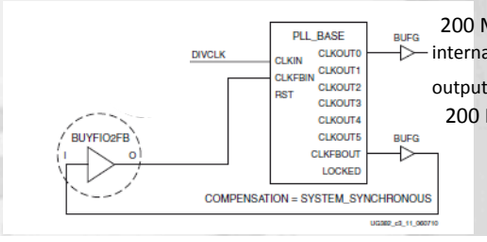


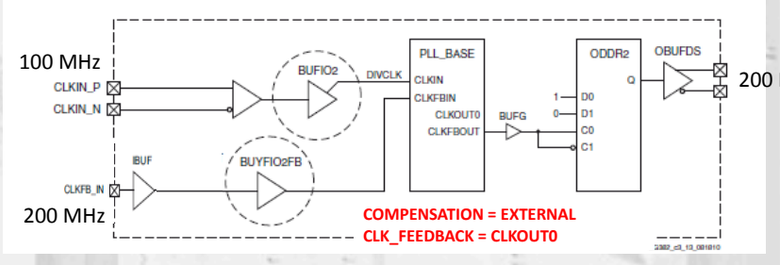
Custom fw solutions are developed in order to enhance the calibration scan
a high frequency interface with SRAMs is on study
a 140 MHz clock interface has been successfully integrated in the "official" fw
a 200 MHz clock interface has been successfully tested stand-alone



optimize termination (SSO problem)

Clock distribution





ROD production plan and testing procedures

ROD ready for production for IBL

We defined a list of minimal procedures to validate the ROD cards after production

- ✦Firmware-software upload from VME, JTAG and Gb/s-Ethernet ports
- ✦ROD-2-BOC dataflow over all I/O lines
- ✦R/W tests for Virtex5 and Spartan6 external memory modules
- ✦Dataflow tests on the 3 Gb/s ports
- ✦TIM card connectivity test

Test committed-delegated to the ROD manufacturer company

- **This is the same we asked for ROD ver B and C cards**
- Electrical test after component supply
- RX test for large BGA-packaged components

15 RevC IBL ROD board production started on August 26th 2013
Boards are expected on the first week of October
Distribution to CERN might start at the end of October

Pixel Layer 1 and 2 future limitations

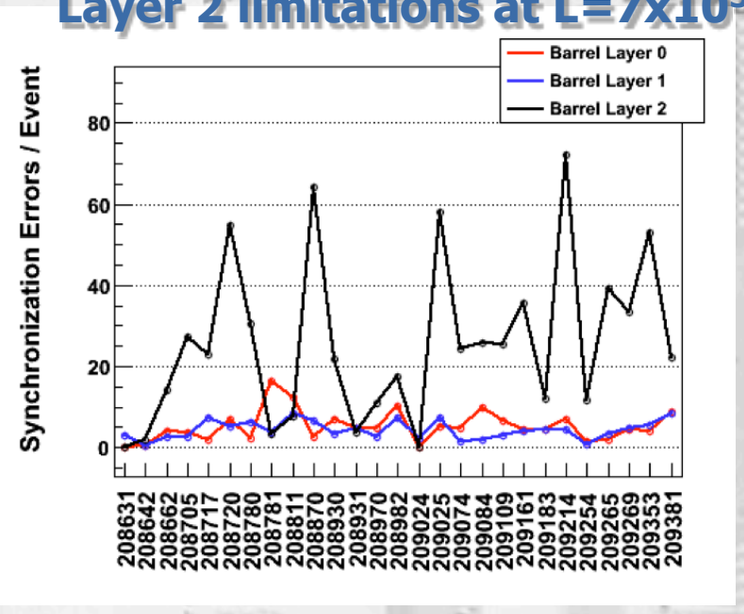
With the restart of LHC we expect a higher luminosity, which will increase even more in the next years.

The link occupancy for the Pixel readout link will suffer from bandwidth limitations.
(reminder: link bandwidth is a function of both occupancy and trigger rate)
Module and link occupancy have been extrapolated using the experience gained from the last year(s).

Suffering for Layer2 could be observed already in the last run period.
Possible Action: Increase link bandwidth to 80 Mb/s

Layer 1 will experience at ~ $2x10^{34}$ luminosity
Layer 1 is already read out at 80 Mb/s
Possible Action: Double the links per module and upgrade the bandwidth to 2x 80 Mb/s,
(requires installing additional fibres now)

Layer 2 limitations at $L=7x10^{33}$



Adopting ROD for layer 1 and 2

Therefore, using the presented IBL ROD and BOC cards is a viable solution also for the Pixel upgrade to overcome the bandwidth limitations.

Firmware of the ROD need modification to handle the Pixel module data.

No Atlas official plan at the time being but discussion well advanced.

We can propose to repeat the same roadmap for Layer2
(caveat:
new boards production should start soon; to be installed mid next year)

Whatever needed for Layer 1 will be probably postponed after IBL and Layer 2 commissioning; only components might be bought earlier

further benefits:

No major further development is needed as the ROD and BOC are there for the IBL anyhow

Firmware adaptation to Pixel needs

This will uniform our readout system:

Common spares for the 4-Layers Pixel

Summary and conclusions

- The ROD card for the readout of the Atlas IBL pixel has been presented
- Tests on the pre-production batch have been discussed and selected results shown
- The final production has been launched (15 cards)
- Bandwidth limitation of existing Pixel layers 1 and 2 have been analyse
- The benefits of adoption of the IBL ROD even for layer 1 and 2 have been pointed out

Additional Material

IBL ReadOut system summary

Number of IBL Staves /ROD-BOC pair	14
# DAQ Modules per ROD-BOC pair	16
# FE-I4s chip per ROD-BOC pair	32
Total # of FE-I4s in IBL	448 (32*14)
Number of Pixels per FE-I4	26880
Total # of read-out channels	~12 M