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P. Aspell, M. De Gaspari, H. França, E. García García, L. Musa

April 12, 2013

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## I. Introduction

THE Super-Altro 16 channel Demonstrator (S-Altro) is a front-end ASIC designed for the readout of gaseous detectors such as Multi-Wire Proportional Chambers (MWPC), Gas Electron Multipliers (GEM) and Micro-MEsh GAseous Structures (Micromegas). The main applications for the chip are the readout of a Time Projection Chamber (TPC) prototype for the future Linear Collider [1] and for GEM and Micromegas test benches.

The baseline is the ALTRO chipset [2], which was developed for the TPC of the ALICE experiment at CERN [3]. In that application, the readout is based on MWPC, the pad size is approximately 30 mm$^2$ and the front-end electronics is mounted on boards perpendicular to the TPC endplate. This allows readout based on a preamplifier/shaper and a separate ALTRO chip. In the TPC for the Linear Collider (LCTPC), the minimum pad size is as small as 1x4 mm$^2$ and the readout electronics has to be mounted parallel to the endplate. The essence of S-Altro is its innovative compact design, where preamplifiers/shapers are integrated together with ADCs and DSP in the same silicon chip. The chip also offers the capability of handling both signal polarities to be useable with different types of detector.

S-Altro is designed in a 130 nm CMOS technology and measures 5.75 mm by 8.56 mm. Its main function is to amplify charge pulses coming from gaseous detectors, digitize them, process them digitally in order to correct imperfections and enable the readout of zero suppressed data.

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## II. General architecture

The Linear Collider TPC requires front-end electronics capable of efficient zero suppression, to reduce the amount of data that has to be transmitted.

In order to apply efficient zero suppression, any imperfections of the signal or of the baseline need to be corrected. Typical distortions of the signal shape may arise from the presence of ions in a TPC, whilst baseline systematic jumps or patterns have been problematic for previous large scale gaseous detectors systems.

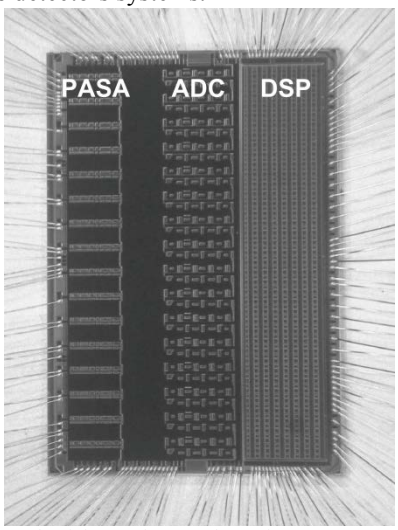


Fig. 1. A photograph of the S-Altro 16 channel Demonstrator.

Fig. 2 shows the block diagram of the S-Altro signal path. Each of the 16 channels is composed of a programmable Pre-Amplifier Shaping Amplifier (PASA), a pipelined

Analog-to-Digital Converter (ADC), and a Digital Signal Processor (DSP).

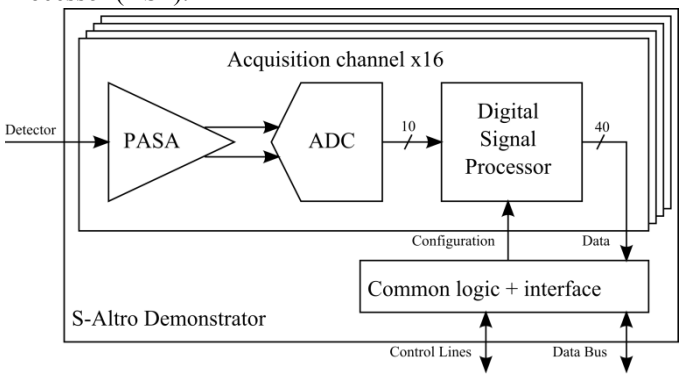


Fig. 2. Block diagram of the S-Altro 16 channel Demonstrator.

The zero-suppressed output of the full chain is saved in internal memories (Multi-Event Buffer) for eventual read out.

The main design specifications for the S-Altro are outlined in Table I.

TABLE I
S-ALTRO SYSTEM SPECIFICATIONS

| | |
|---|---|
| Supply voltage | 1.5 V core, 2.5 V pads |
| Programmable gain | 12, 15, 19 or 27 mV/fC |
| Programmable peaking time | 30, 60, 90 or 120 ns |
| Shaper type | CR-$(RC)^4$ |
| Programmable signal polarity | Positive or negative |
| Linearity | ±5% up to 150 fC |
| Detector capacitance | 4-20 pF |
| ENC | <1000 $e^-$ @ 12 pF |
| Cross-talk | <1% |
| Number of bits | 10 |
| Sampling frequency | 10-40 MHz |
| Readout frequency | max 80 MHz |
| Power consumption | <50 mW/channel |
| Area | <4 $mm^2$/channel |

One important specification was that the S-Altro should be compatible with the existing readout infrastructure used for the ALTRO chip in the ALICE experiment. In particular the interface protocol is unchanged from the ALTRO development.

As well as applying DSP functions to an incoming signal, it was also a requirement that these functions could be disabled to allow the readout of the raw digitized signal unprocessed. This is particularly useful when using the chip with new uncharacterized detectors. The S-Altro hence has an operational mode in which the DSP is disabled and the outputs of a selectable subset of the 16 ADCs are buffered continuously into the communication bus.

## III. ANALOG FRONT-END

### A. Preamplifier and Shaper

The charge pulses produced by the detector are amplified and shaped by the PASA, shown schematically in Fig. 3. A pre-amplifier integrates the charge onto a feedback capacitor $C_f$, which is continuously discharged by a feedback resistor $R_f$ (implemented as a transistor operating in linear region). The total input capacitance is approximately 3 pF, optimized for detector capacitances of approximately 10 pF.

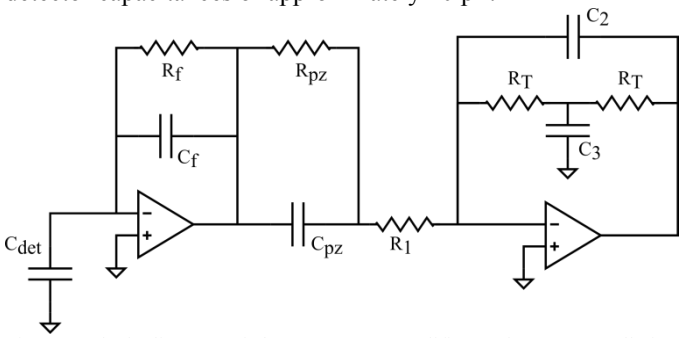


Fig. 3. Block diagram of the PASA. Preamplifier, pole-zero cancellation network and first T-bridge amplifier are shown; $C_{det}$ represents the detector capacitance.

After a pole-zero cancellation network ($R_{pz}$ and $C_{pz}$), two amplifiers, in T-bridge configuration [4], filter the signal and provide a differential voltage output. The nominal single-ended output range is 250 mV to 1.25 V, giving a peak-to-peak output differential voltage of 2 V.

The resulting transfer function of the system is a CR-$RC^4$ filter where a current pulse at the input is converted into a semi-gaussian differential pulse at the output. As in the ALICE TPC, the $4^{th}$ order shaping is chosen because it offers a faster return to baseline as compared to lower-order filters. This helps preventing pile-up when two or more pulses come closely spaced in time.

Some parameters of the PASA can be set externally, using static control inputs. These include:

--Shaping time (3 bits): the time-to-peak of the output pulse can be selected from 30-60-90-120 ns.

--Gain (2 bits): the voltage/charge gain can be set to 12-15-19-27 mV/fC.

--Polarity: Positive or negative input charge.

--*BiasDecay*: an external voltage controls the resistance of the feedback transistor, shown as $R_f$ in Fig. 3, in the range 300 kΩ - 2.3 MΩ.

--Shut down mode: the PASA can be shut down for power saving when not in operation.

There is also a choice of ESD input protection. Two structures were implemented using two input pads per channel. One structure is a simple double diode and the second more robust structure contains a current-limiting resistor in series with the input and an additional pair of diodes. The choice of which structure to use is done at the bonding stage.

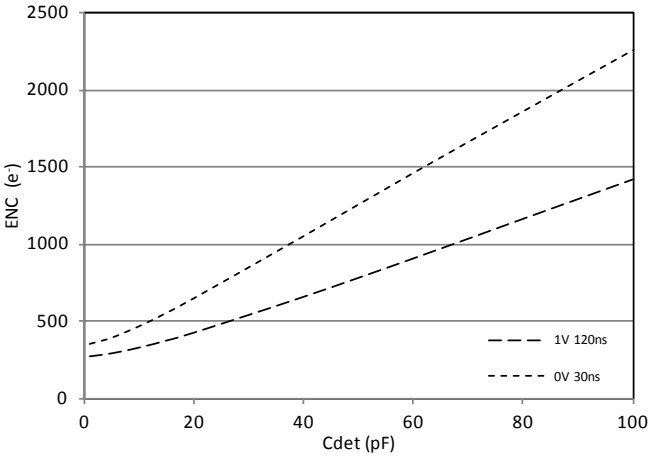


Fig. 4. Simulated ENC of the PASA, as a function of the detector capacitance. The upper line corresponds to a configuration with BiasDecay 0 V and shaping time 30 ns, while the lower line corresponds to 1 V and 120 ns.

Fig. 4 shows the simulated Equivalent Noise Charge (ENC) of the PASA in two different configurations of shaping time and *BiasDecay* voltage. The minimum noise, for small detector capacitances, is approximately 300 electrons. The dominant noise sources are the series noise of the input transistor and the parallel noise of the feedback transistor which implements $R_f$. For high values of the *BiasDecay* voltage (high $R_f$), the input transistor is the biggest noise source, while for low $R_f$ the white noise of the feedback transistor dominates.

### B. Analog-to-Digital Converter

The PASA output is digitized by a 10-bit pipelined ADC, which was independently prototyped [5]. The maximum ADC sampling frequency is 40 MHz.

The pipeline architecture is implemented with switched capacitors and consists of eight 1.5-bit stages followed by one 2-bit stage, as shown in Fig. 5.

The main amplifier of each 1.5-bit pipeline stage is fully differential. The sampling capacitor structure of every stage is duplicated allowing double sampling, i.e., while one structure is sampling, the other one is amplifying. This allows two clock periods for each amplifier to settle before the next sample is taken. The 9$^{th}$ pipeline stage is a 2-bit flash made up of three comparators.

Externally applied reference voltages (250 mV and 1.25 V) are used to match the ADC input range to the PASA output range. The transfer function of 1.5-bit pipeline stages shows that the degradation of linearity caused by capacitor mismatch and finite operational amplifier gain increases linearly as the input voltage is either increased from $-V_{ref}$ to the lower threshold ($-V_{ref}/4$) or is decreased from $+V_{ref}$ to the higher threshold ($+V_{ref}/4$). If the two thresholds are further spaced out, the degradation of linearity is interrupted earlier in the voltage scale, resulting in better INL. In this design, dynamic comparators set thresholds of $\pm 3/8V_{ref}$; this improves the INL, as compared to the conventional $\pm 1/4V_{ref}$ thresholds [5].

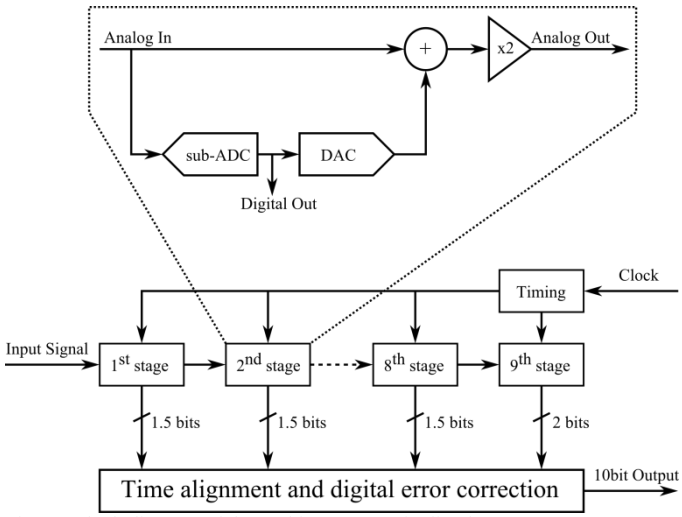


Fig. 5. Block diagram of the 10-bit 40 MHz pipelined ADC.

The sampling clock is delivered to the chip externally. Internally, the phase of sampling clock edges is carefully controlled and delivered to each channel via a balanced clock tree.

At the tail end of the ADC a digital error correction block removes redundancies from the 18 bits generated by the pipeline stages, and provides a clean 10-bit output free of comparator errors. The total latency of the ADC is 10 clock cycles.

The ADC prototype was tested at room temperature and at the nominal conversion frequency of 40MHz. The measured integral and differential non-linearities are INL=0.71 and DNL=0.58 (LSB). Dynamic tests were run injecting sinusoidal test signals with frequencies from 1MHz to 20MHz. At low frequencies, the effective number of bits is ENOB=9.07. When close to the Nyquist frequency the ENOB=8.63 and the figure of merit is 1.54 pJ per conversion step.

Biasing of all 16 ADCs in the S-Altro is provided by one beta-multiplier circuit [6]. The beta-multiplier circuit (Fig. 6) has its current-setting resistor split into two parts such that an on-chip resistor (ensuring stability of the circuit) is complemented by an off-chip resistor. This allows users to set the power consumption externally, depending on the required sampling frequency, or to open the bias network, turning off the ADCs. The nominal value of the external resistor is 3 kΩ, providing the appropriate current for a sampling frequency of 40 MHz.

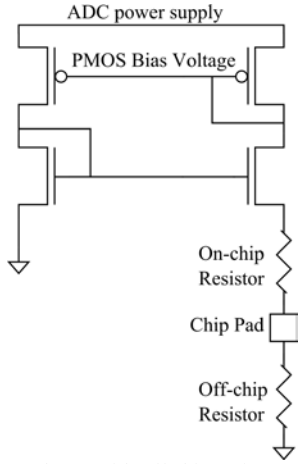


Fig. 6. Beta multiplier scheme with off-chip resistor, used to bias the ADCs [6].

## IV. Digital Section

### A. Timing and Triggering

Two trigger levels define the data acquisition structure of S-Altro. The first level trigger (L1) starts the data acquisition and by doing so determines the start of the acquisition window, while the second level trigger (L2) validates the data from the previous L1. When a L2 trigger is received, data corresponding to the last acquisition are stored within the chip's internal memory called the Multi-Event Buffer (MEB). In case that a L1 trigger is followed by another L1, without an L2 validation, a new acquisition is started and the data from the first acquisition are lost.

The MEB can store up to 1000 samples per channel and per acquisition. The maximum time duration of an acquisition is 100 μsec for a 10 MHz sampling rate, or 25 μsec for 40 MHz.

After one or more L2 triggers, a readout command can be issued, and the contents of the MEBs are transferred off-chip.

### B. Digital Signal Processing

Digital Signal Processing (DSP) is performed by the blocks shown in Fig. 7 in a pipeline fashion.

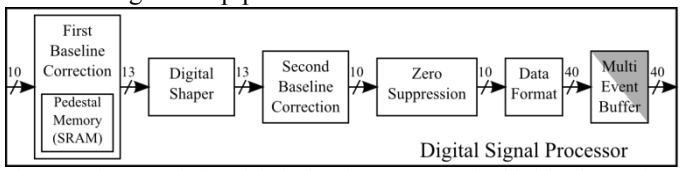


Fig. 7. Diagram of the Digital Signal Processor embedded in the S-Altro. Most blocks operate at the sampling clock frequency, while the Multi Event Buffer, partially shaded in grey, works with the readout clock, as well.

The first block performs the first level of Baseline Correction (BC1), which can remove a baseline by subtracting a pedestal value. The pedestal value can be either fixed (for systematic offsets) or variable (in the case of low frequency baseline drifts). If the fixed baseline subtraction is chosen then the baseline is determined by the user and saved in a register during a calibration phase. For the "variable" case, the variable value is calculated by the BC1 using an Infinite Impulse Response (IIR) filter, whose time response can be adjusted by setting a dedicated register. The IIR filter is only active outside the acquisition window (before L1 trigger) and when there is no pulse. Programmable thresholds define which samples are to be considered baseline, so that the signal does not disturb the baseline calculation.

This feature of the BC1 is useful for the correction of slow variations of the baseline due, e.g., to a temperature drift.

Another functionality is to remove systematic patterns that can be introduced, for example, by the switching of the gating grid of a TPC with MWPC readout. In order to do this, a Pedestal Memory (PMEM) is used to store baseline samples during a calibration phase which are subtracted from the data stream during data taking. The size of one PMEM is 1.25 Kbyte (1000 samples of 10 bits each).

The second block is the Digital Shaper (DS). Its task is to compensate the distortion of the signal shape due, for example, to long ion tails in the detector. The DS is an IIR filter with eight programmable filter coefficients that determine the positions of up to four poles and four zeros in its transfer function. The filter is implemented as a cascade of four first-order IIR transposed filters [7]. With appropriate values of the filter coefficients, it is possible to remove either a tail, or an undershoot from the incoming pulses.

The Second Baseline Correction block (BC2) reduces non-systematic baseline movements via a Moving Average Filter (MAF). The MAF is a Finite Impulse Response (FIR) filter that computes the average of the last two, four or eight samples (decided through a programmable register). The user can set parameters which define a higher and a lower threshold, that the MAF uses to exclude signal samples from the calculation of the baseline. The function of the BC2 is to correct variations of the baseline occurring within the time frame of the acquisition window. This could help correct for instabilities in the power supply.

The main purpose of the previous blocks has been to remove imperfections from the baseline and signal such that clean discrimination of the signal can be applied to remove all data void of a signal. The last DSP block is the Zero Suppression (ZS). This block removes the baseline samples below a programmable threshold. Included is a glitch filter, which removes pulses shorter than a programmable minimum number of samples. Samples directly before and after a pulse may also be kept and stored; the exact number is programmable.

The Data Formatting (DF) unit converts the 10-bit data flow in a 40-bit data format which includes a header and a trailer, time stamp, configuration information and error flags. The data are saved in this format in the Multi-Event Buffer.

The size of the MEBs is 40 Kbit (5 Kbyte); this allows saving four 1000-sample acquisitions or eight 500-sample acquisitions. At the receipt of a L2 trigger, a write pointer in the memories is pushed forward, and the already acquired data are protected from being overwritten.

The MEB hence stores all L2 zero suppressed data during the acquisition window. Readout of the MEB is only performed outside of the acquisition window.

### C. *Interface*

The common logic and interface block of Fig. 2 implements the communication between S-Altro and the outside world. This communication is based on 40 data/address lines and 12 control lines. The interface allows configuration of the chip as well as data readout of the MEB. The configuration of the many programmable S-Altro features is done by reading and writing 9 global registers and 13 channel registers, and issuing 7 commands.

The total memory of the MEBs is 80 Kbyte. The maximum frequency of the readout clock is 80 MHz, which means that the maximum readout time (and hence dead time) is 0.2 ms.

## V. ISOLATION TECHNIQUES

The S-Altro is a complex mixed-signal chip, which integrates low-noise analog structures together with potentially noisy digital circuitry. Minimizing noise coupling from the digital part to the analog part has been a critical part of the design.

The most sensitive analog node is the input of the PASA, where a voltage step of 20 μV on a 5 pF capacitance corresponds to a charge of 0.1 fC, comparable with the intrinsic noise introduced by PASA and ADC. On-chip digital signals have a voltage swing of 1.5 V requiring attenuation of the coupling greater than 90-100 dB. In order to achieve such a level of isolation, several techniques have been used.

The shaper and the ADC are designed to be fully differential in order to reduce their sensitivity to common-mode noise.

Logic switching activities are kept to a minimum and concentrated in non-critical time intervals. An internal clock tree provides clocks to the ADCs and DSP block. The DSP clock is delayed by 600 ps with respect to the ADC clock to ensure that the ADC sampling is done during a quiet period before the toggling of the DSP logic starts. The readout of the memories is done outside of the data acquisition window.

Careful floor-planning and layout also aim at minimizing noise coupling. The PASAs, ADCs and DSP form blocks which are completely isolated from one another. Each has its own independent power supply. There are in total five power domains: PASA, ADC analog, ADC digital, DSP, and digital pads. All signal lines belonging to a given domain are geometrically confined inside that domain and do not cross signals of other domains. The power supply paths on-chip are designed as wide as possible. The analog power of the ADC is the most critical, because of the large current needed. Its supply path is 770μm wide in order to avoid voltage supply drops in excess of 10mV. The chip makes extensive use of on-chip decoupling capacitors. The space available underneath the supply lines is used to implement decoupling capacitors. These amount to 600pF per channel for the PASA supply lines, 600pF/channel for the ADC analog, 80pF/channel for the ADC digital and 40pF/channel for the ADC reference voltages. The digital pads with a high toggle rate have been placed far from the ADC and PASA domains, while static digital pads are closer.

The 130 nm CMOS technology offers a lightly doped high-resistivity substrate implant. This is employed extensively around every power domain in order to increase the substrate resistance between adjacent domains. For the smallest digital islands in the ADC, the resistance between different substrate partitions reaches 700Ω. The implant is complemented on both sides by N-wells, to collect electrons, and $p^+$ guard rings, to provide clean bias to the inner substrate region.

## VI. TEST RESULTS

Functional tests prove that the chip is fully operational. The processing chain works smoothly and the chip communicates correctly with the external world.

Fig. 8 illustrates the functionality of the chip. Voltage steps are applied to a PASA input and the resulting signals are filtered and processed by the full PASA+ADC+DSP chain. The figure shows three pulses, two acquired with the same settings of gain but different shaping times and one pulse acquired with a different gain.

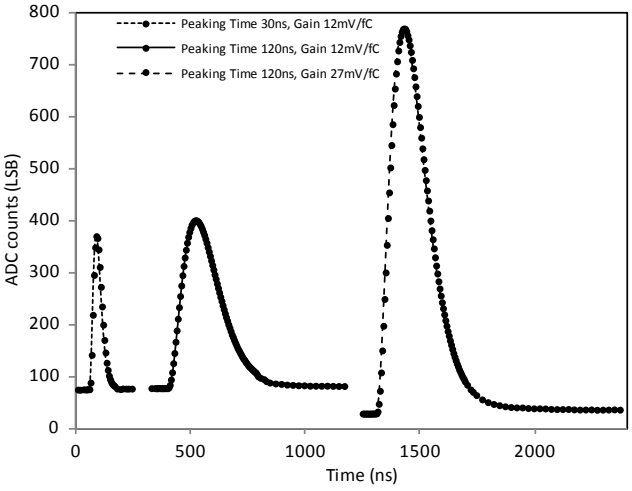


Fig. 8. The pulse shape, plotted with different PASA gains and shaping times. Acquisitions at 40 MHz sampling frequency (25 ns period) are repeated in 5 sets using the same channel. In each set of acquisitions, the delay between the L1 trigger and the input pulse is increased by 5ns. This produces a scan of the pulse shape with a granularity of 5 ns.

Fig. 9 plots the gain of one PASA channel, as a function of the charge injected at the input. The vertical error bars include random noise of the acquisitions (20 acquisitions per point) and the random uncertainty on the injected charge. The gain uncertainty on this type of measurement is dominated by the tolerance of the on-board capacitors used to inject charge to the PASA input.

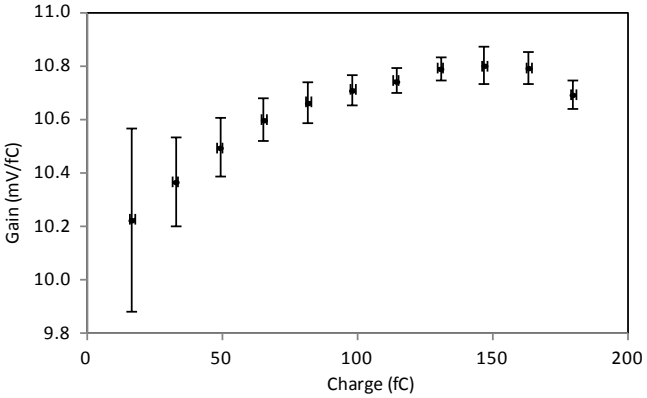


Fig. 9. Typical gain of one channel, for different values of input charge.

The baseline noise is measured during the acquisition window when no input stimulus is provided and calculated as the standard deviation of many samples of the baseline.

The noise was measured under two different packaging conditions. The first ignored the additional capacitive loading on the inputs by severing the input bonds, measuring the baseline noise in mV and dividing the noise (in mV) by the gain. These results are shown in Table II with different settings for peaking time and gain. The results are averaged over the 16 channels, and expressed in ADC Least Significant Bits (LSB), equivalent input charge in fC, and number of electrons.

TABLE II
S-ALTRO DEMONSTRATOR NOISE IN DIFFERENT PASA CONFIGURATIONS

| Shaping time | 120 ns | 120 ns | 30 ns | 30 ns |
|---|---|---|---|---|
| Gain | 12 mV/fC | 27 mV/fC | 12 mV/fC | 27 mV/fC |
| Noise (LSB) | 0.480 | 0.655 | 0.526 | 0.683 |
| Noise (fC) | 0.088 | 0.051 | 0.103 | 0.059 |
| Noise ($e^-$) | 547 | 316 | 641 | 370 |

The noise results of Table II include all ASIC noise sources such as random noise of the PASA and ADC, quantization noise of the ADC, and noise pickup from the DSP. These results hence give the lower limit on the noise performance achievable on a board with very clean ground planes and low additional input capacitance. The best noise measurement, taken as a reference, is 316$e^-$, very close to the simulated PASA noise of 320$e^-$. This demonstrates that the logic switching activity in ADCs and DSP does not deteriorate the PASA noise performance.

The second set of measurements is made with a fully bonded chip. Measurements were taken with varying values of additional external capacitance added to the input. The shaping time and gain settings were fixed to 120 ns and 12 mV/fC respectively. The results are plotted in Fig. 10.

The typical minimum ionizing particle charge deposition in the ALICE TPC is 4.8 fC resulting in a signal to noise ratio of 54. The maximum input charge is 150 fC and the dynamic range is 64.6 dB.

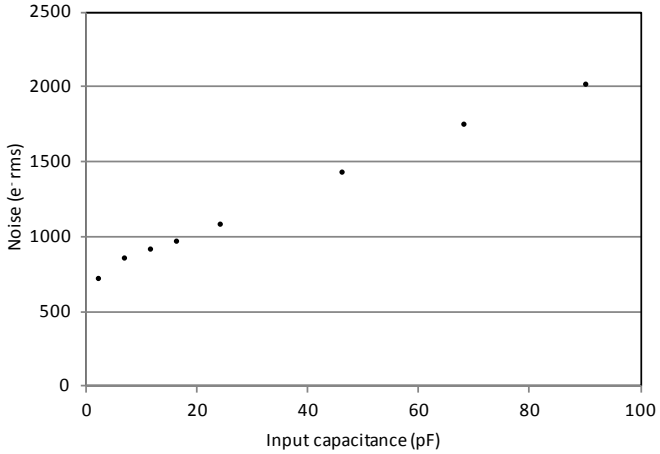


Fig. 10. Noise of one channel, for different values of input capacitance.

Crosstalk was evaluated by the injection of a full-scale signal into one channel (the aggressor), whilst, at the same time, measurements were taken in the neighboring channels (the victims). The results showed crosstalk, from aggressor to victim, to be smaller than 0.7% between adjacent channels.

The digital part of the S-Altro was also tested independently using the Pedestal Memory. Patterns were loaded in the PMEM and played through the DSP. In this way, tests could be performed with the stimulus files used for simulation during the design.

Fig. 11 illustrates the action of the Digital Shaper on some input pulses with undershoot.

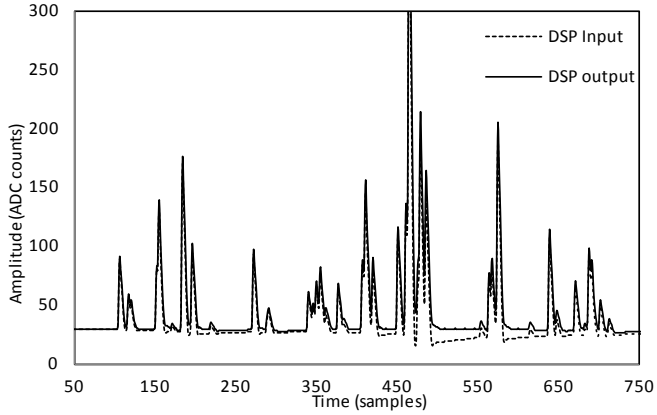


Fig. 11. Example of functionality of the Digital Shaper: undershoots in the input data stream are corrected at the output.

Similarly, Fig. 12 shows how Baseline Correction 2 can remove a drift of the baseline.

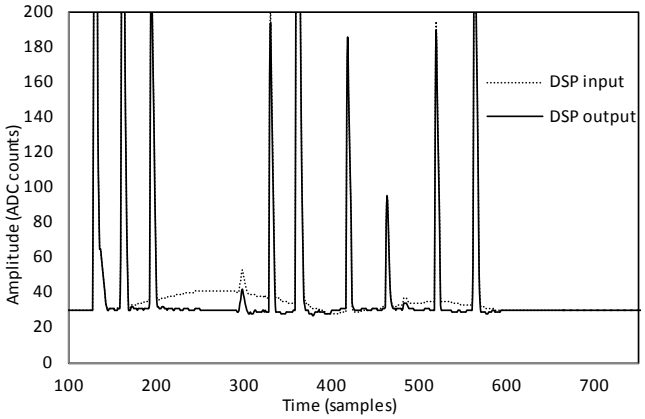


Fig. 12. In this example, the Baseline Correction 2 removes the baseline drift from an input pattern.

The power consumptions of PASA, ADC, and DSP are reported in Table III. Power consumption measurements were made in "shut down mode" (PASA and ADC are shutdown, the DSP is not clocked) and under normal running conditions.

TABLE III
S-ALTRO DEMONSTRATOR POWER CONSUMPTION

| Power Domain | Shut down mode | Normal mode | Power/channel |
|---|---|---|---|
| PASA | 2.12 mW | 164 mW | 10.26 mW |
| ADC Analog | 6.88 mW | 500 mW | 31.28 mW |
| ADC Digital | | 27 mW | 1.71 mW |
| DSP | 0.16 mW | 65 mW | 4.04 mW |
| S-Altro Total | 9.2 mW | 757 mW | 47.3 mW |

The dynamic shutdown capabilities of the S-Altro and its test board allow implementation of power pulsing cycles, particularly useful in the LCTPC application.

The wake-up time has been measured. The system was powered up after a shutdown period and then a L1 trigger and a test pulse were sent at a given delay after power up. Fig. 13 plots the amplitude of the acquired pulse as a function of this delay.

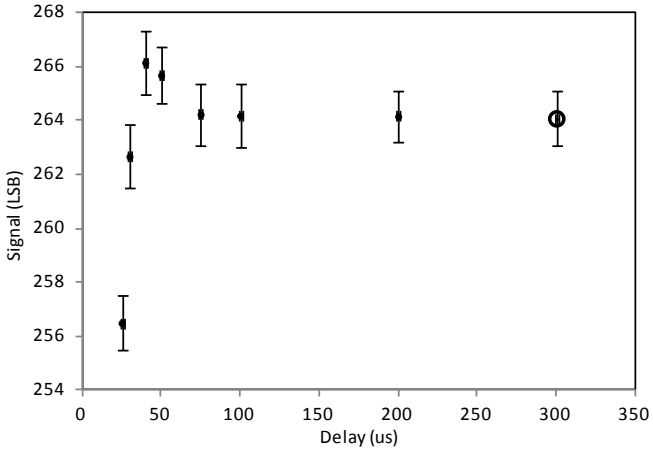


Fig. 13. Amplitude of a test pulse acquired after a shutdown period, as a function of the delay between power up and L1 trigger. The last data point (circled) is measured in continuous mode.

Measurements at 200, 100 and 75 µs do not differ from acquisitions taken in continuous mode. This test shows that, after a wake-up time of 75 µs, the system is ready to acquire data.

## VII. SUMMARY

The S-Altro Demonstrator has been designed, prototyped and tested successfully. It is a 16-channel front-end chip designed for the readout of gaseous detectors, based on ADCs and DSP capabilities. The architecture is based on a charge amplifier/shaper, ADC and DSP per channel. The technique of digital filtering is capable of removing imperfections of the signal shape and variations of the baseline, which allows efficient zero suppression. Two external triggers are used to start and then validate an acquisition. On-chip memories store up to four acquisitions of up to 1000 samples (25 µs at 40 MHz sampling) from 16 channels. Data packets including time stamps are created and transmitted to the outside world via a 40-bit parallel bus.

Test results show full functionality of the chip. The S-Altro chip effectively demonstrates that using careful design techniques, the integration of low-noise analog components and complex digital functions on the same silicon die is possible with little effect on noise performance.

The chip provides an effective stepping stone on the path to the Linear Collider (LC) TPC and is immediately useable in LCTPC prototypes. The area is 3.07 $mm^2$/channel. Power pulsing features are also included.

Moreover, the S-Altro system also provides a useful tool for studying the electrical behaviour of new micro pattern gaseous detectors.

A possible evolution of the project, currently under investigation, is optimization for lower power consumption.

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