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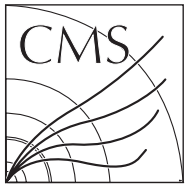

**The Compact Muon Solenoid Experiment**

**Conference Report**

Mailing address: CMS CERN, CH-1211 GENEVA 23, Switzerland

**18 March 2013 (v2, 23 March 2013)**

# DC-DC Powering for the CMS Pixel Upgrade

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The CMS experiment plans to replace its silicon pixel detector with a new one with improved rate capability and an additional detection layer at the end of 2016. In order to cope with the increased number of detector modules the new pixel detector will be powered via DC-DC converters close to the sensitive detector volume. This paper reviews the DC-DC powering scheme and reports on the ongoing R and D program to develop converters for the pixel upgrade. Design choices are discussed and results from the electrical and thermal characterisation of converter prototypes are shown. An emphasis is put on system tests with up to24 converters. The performance of pixel modules powered by DC-DC converters is compared to conventional powering. The integration of the DC-DC powering scheme into the pixel detector is described and system design issues are reviewed.

Presented at *VCI 2013 13th Vienna Conference On Instrumentation*

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*Keywords:* CMS, LHC Upgrades, Tracking Systems, Pixel Detector, Power Distribution, DC-DC Conversion

## 1. Introduction

DC-DC conversion inside the detector volume as a means to reduce power transmission losses and to limit conductor cross sections is a novel approach in high energy physics which is currently under consideration in several experiments. In this paper the application of such a powering scheme in the planned upgrade of the CMS pixel detector will be described. While the challenges will be discussed in this concrete application the results should be applicable to other systems as well.

## 2. CMS Pixel Upgrade

The current CMS pixel detector has been specified for the LHC design luminosity of $1 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$. However, according to the current planning, the instantaneous luminosity will reach twice this value already sometime between 2015 and 2018. Since this higher luminosity would cause severe dead time, CMS plans to exchange the pixel detector in the shutdown 2016/17. Besides the implementation of a new read-out ASIC the new pixel detector will feature an additional detection layer (4 instead of 3 in the barrel, 3 instead of 2 in each endcap) and a factor of 1.9 more channels. Since the existing cable plant must be re-used the approximate doubling of the supply current would lead to an excessive increase of the cable losses by a factor 4. A new powering scheme is needed to reduce these losses.

## 3. Powering Options

Two quite distinct schemes could be envisaged to provide the increased power required by the upgraded detector [1]. Both supply power to the detector at an increased voltage and therefore reduced current. In the DC-DC conversion scheme DC-DC converters are introduced close to the detector modules to perform this voltage conversion. This maintains the modularity of the power supply system, the grounding scheme, and other system level aspects close to the current well established systems. Only one new component needs to be introduced. The second scheme connects many detector modules in series to the power supply (serial powering). Since each module then has a different ground potential and the maximum current needed by any given module has to be routed through the full chain, several modifications of the system design are necessary including AC coupled communications and bypass circuits. Further aspects to consider when choosing between these schemes are the switching noise of the DC-DC converters which must be tolerated by the detector system and differences in the distribution of the material budget which have to be evaluated for the application under consideration.

CMS has chosen the DC-DC scheme for the pixel upgrade in order to keep the changes to the system design minimal and local [2]. The switching noise and the material of the converters are less of a concern in this application since they will be placed about 2 m away from the detector modules, outside the tracker acceptance. This decision was based on the well advanced R&D on this scheme both in CMS [3, 4] and at CERN [5]. Since there is no experience with such a powering scheme in any HEP experiment, careful design and comprehensive tests are mandatory.

## 4. DC-DC Buck Converter

Converters of the 'buck' type will be employed (Fig. 1). The main components are an ASIC which contains two large transistors and control logic, an inductor as energy buffer, and filter

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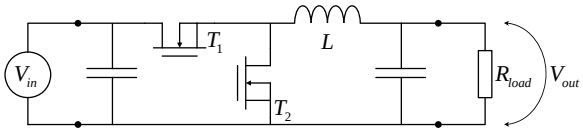


Figure 1: Simplified schematics of a DC-DC buck converter. Transistors $T_1$ and $T_2$ are operated by a pulse width modulation logic which is not shown.

networks. The load is connected in series with the inductor to the power supply via one of the transistors ($T_1$). This transistor is closed only for part of the time (duty cycle $D$) while for the rest of the time the inductor keeps the current to the load flowing via the second transistor ($T_2$). Since the average current drawn from the power supply is reduced by the factor $D$, energy conservation requires that the input voltage to the converter has to be higher by the inverse factor, assuming a lossless converter: $V_{in} = V_{out}/D$. Typical conversion ratios are in the range 2 to 10. Pulse width modulation logic is used to regulate the output voltage. Since the current ripple at the inductor decreases with switching frequency, high frequency operation seems advisable to minimize this ripple and the corresponding resistive losses in the inductor and the transistors. However, switching and driving losses of the transistors increase with frequency and a switching frequency in the range of 1 MHz turns out to be optimal for our application. Efficiencies, defined as the ratio of the power provided by the converter to its input power, are in the range 60 to 90 %. For the CMS pixel system the input voltage to the converter will be 10 V while the output voltages, defined by the analogue and digital voltages needed by the module electronics and voltage losses between the converters and the modules will be 2.4 V and 3.0 V, respectively. The conversion ratio is therefore 3-4 and the cable losses are reduced by the square of this ratio, i.e. an order of magnitude.

## 5. Implementation into the CMS Pixel System

For the full CMS pixel system 1184 converters will be needed. They will be mounted about 2 m away from the pixel modules on the carbon fibre cylinders used to guide all the pixel system services. For the barrel layers of the pixel system the services are organized in channels. Each of them contains 13 DC-DC converter pairs (analogue and digital voltage) which are plugged into a bus board. Six or seven pairs of converters are powered from one external power supply which is located outside the CMS detector and connected via about 50 m long cables. Each converter pair serves one to four pixel modules, depending on their current consumption, which is higher for modules closer to the interaction point because of the higher hit rate. The output current of the DC-DC converters is always below 3 A. Fig. 2 shows a mock-up of such a channel. The converters are cooled via aluminium cooling bridges to which they are screwed and which, in turn, are clamped around $CO_2$ cooling pipes which run along each channel.

There are a number of system integration issues which need to be dealt with. Since DC-DC converters are a novel component inside a high energy physics detector there is no working experience and it is unclear which control and protection features are essential. The approach chosen for the CMS pixel system is as follows. The control logic in the converter ASIC includes protection against over-temperature and under-voltage and limits the converter output current. A solid state fuse will disable converters with excessive current permanently such that the other converters (and modules) supplied by the same external power supply can still be operated. Individual converter pairs can be enabled or disabled and their status read back via slow control communications. In order to promote system stability both the external power supplies and the converters regulate the voltage locally at their output (no remote sensing). Voltage drops therefore need careful attention.

Possible electromagnetic interference between the switching converters and the detector modules or other parts of the experiment is one of the prime concerns one might have with the DC-DC powering scheme. Due to the relatively large distance to the pixel modules and the solid shielding of the converters in their channels this is, however, less of a concern in this application. Extensive tests have, nevertheless, been performed and results are reported below.

The space available for the converters is tight and they have to be shaped accordingly. The envelope for a converter is $30 \times 20 \times 14$ mm$^3$. The bus board, which has to distribute large currents (about 40 A) and provide the required connectivity, is also highly constrained. Still the converters should be easily accessible and replaceable.

The last system integration issue which we would like to point out is the cooling which is needed for safe operation of the converters. Due to its inefficiency each converter dissipates about $1-2$ W of power which will be removed via $CO_2$ cooling pipes.

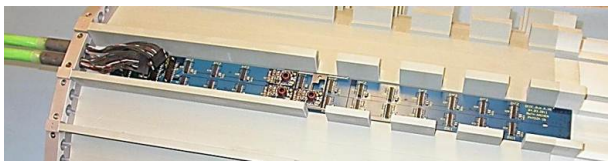

Figure 2: Prototype of a DC-DC bus board in a channel of a supply tube mock-up. The board is equipped with three converters. The converter in the centre is mounted on an aluminium cooling bridge which is clamped onto pieces of cooling pipe. In the final system all converters are mounted in this way.

## 6. DC-DC Converter Development

The application described above defines the requirements that must be met by the DC-DC converters. Beyond what has already been mentioned, the converters have to operate in a harsh radiation environment. A fluence of $2 \times 10^{14}$ n$_{eq}$/cm$^2$ and an ionizing dose of 100 kGy are expected at the location of the converters for an integrated luminosity of 500 fb$^{-1}$. Furthermore, the converters have to operate in the 3.8 T magnetic field of CMS. These two requirements are very different from the environment for which commercial converters are designed. The high magnetic field saturates all ferrite materials and enforces the use of an air core inductor. The required radiation hardness

has motivated the development of a radiation tolerant ASIC at CERN [5]. Prototypes of this ASIC (called 'AMIS4') which is fabricated in the AMIS I3T80 0.35 $\mu$m CMOS process of *ON Semiconductor* are available and have been shown to reach the required radiation tolerance in terms of fluence and ionising dose. Tests for single event effects are ongoing. With respect to the board layout, recommendations by the developers of these ASICs have been used to develop DC-DC converters tailored to the needs of the CMS pixel system. Figure 3 (left) shows a photograph of a prototype of such a converter. The two layer PCB has a size of $28 \times 16$ mm$^2$. It is equipped with $\pi$ filters at the input and output. The biggest component is the plastic core toroidal inductor which has an inductance of 450 nH and a resistance of about 40 m$\Omega$. Underneath this inductor sits the AMIS4 ASIC in a QFN32 package. This prototype converts an input voltage of 10 V to the required output voltages of 2.4 V or 3.0 V at a switching frequency of 1.5 MHz.

Figure 3 (right) shows a cover on the converter which serves three purposes. It shields the magnetic emissions (mainly from the inductor), it acts as a cooling contact for the inductor and it segregates the noisy parts of the converter from the output filters. The shape of this shield is driven by the space constraints in the pixel system. In order to minimize the material budget this shield is made from a plastic core with 0.3 mm wall thickness, plated with 30 $\mu$m of copper and 1 $\mu$m of tin on both sides. A large number of covers have been successfully produced by rapid prototyping. It remains to be decided whether this technique or injection moulding will be used for the series production. The total weight of one converter is about 2.9 g. About 60 DC-DC converters have been built so far.

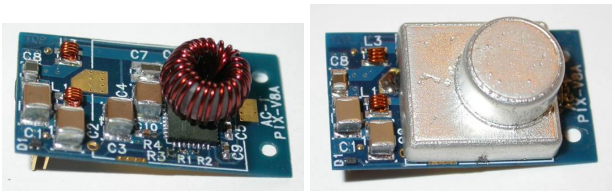

Figure 3: Prototype DC-DC converter without (left) and with (right) shield. The size of the PCB is 2.8 cm times 1.6 cm.

The effectiveness of the cover has been demonstrated in several measurements. The magnetic field emitted by the inductor has been mapped with a scanning pick-up probe and shown to be strongly suppressed by the cover. The noise on the output lines of the converter has been measured with a spectrum analyser. With the cover in place the noise spectra, in particular the common mode noise, are much cleaner, which is attributed to the shielding of emissions into the output filters of the converter as well as the output lines. Thermal measurements have demonstrated that the shield lowers the temperature of the inductor by about 20° C under typical operating conditions.

A very important parameter is the power conversion efficiency of the converters. Figure 4 shows the mean efficiency measured on 12 converter prototypes with 2.5 V output voltage. In the relevant region of 10 V input voltage and $2-3$ A output current we find a very good efficiency of around 80 % which is also very uniform among the different converters. Further measurements have confirmed that the maximum efficiency is reached for the chosen switching frequency of 1.5 MHz and that there is a very mild temperature dependence of about 1 % efficiency increase per 20° C temperature decrease.

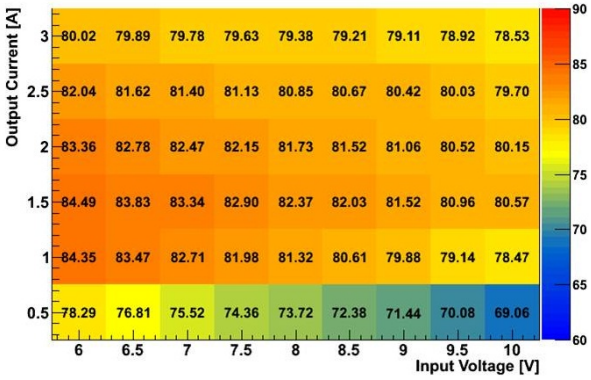


Figure 4: Mean efficiency measured on 12 converter prototypes with 2.5 V output voltage in percent as a function of input voltage and output current. The cooling block temperature was set to +20°C.

Figure 5 shows the temperatures measured on the ASIC and the inductor as a function of the converter's output current for three different temperatures of the cooling block onto which the converter is mounted. It can be seen that the required operation at up to around 3 A of output current is very safe. Given a proper cooling system, the converters could actually provide significantly more current.

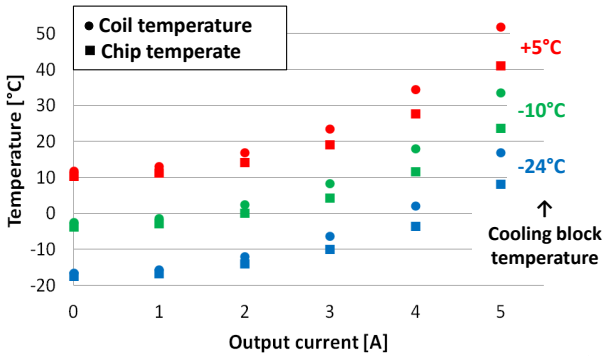


Figure 5: Temperatures measured on the coil (circles) and on the chip (squares) as a function of output current and for different cooling block temperatures of −24°C (blue), −10°C (green), and +5°C (red).

## 7. System test results

After it had been verified that individual converters provide the required performance various system level tests had to be performed.

In the first set of tests, a prototype of the bus board was equipped with 24 dummy converter circuits (since at the time of these measurements a sufficient number of converters was not yet available). The voltage drops on the bus board have been measured and compared to the calculated drops. Good agreement has been found which proves that these voltage drops are

well understood. The bus board was then subjected to 120 thermal cycles between −10°C and +40°C under load. The voltage drops measured after the cycling did not show any degradation of the bus board or its connections.

Once a sufficient number of converters was available a system test was set up which was intended to resemble, as far as possible, the final system in the experiment. The bus board was equipped with 24 DC-DC converters. These were screwed onto aluminium cooling bridges which were attached to $CO_2$ cooling pipes. The system was powered by a prototype pixel power supply via 50 m long cables as will be the case in the experiment. Two barrel pixel modules (of the current type since the new ones are not yet available) were powered by the DC-DC converters, via 2 m of low mass cables. An additional electronic load has been used to fully load the system. In the first step the thermal performance was tested. The two phase $CO_2$ system was operated at −20°C with all converters running under full load. The temperatures measured on the ASICs and the inductors were just below +20°C at 3 A output current per converter, demonstrating the proper thermal functionality of the full system.

Then data was taken with the two pixel modules in order to measure the noise distribution of all pixels on these modules. Three scenarios have been compared. In the first one, power was provided directly by the external power supply as in the current pixel system. In the second case the two modules were powered via DC-DC converters with all 24 converters running in parallel. Finally a test was performed to determine if the fast load variations expected due to the LHC beam structure (3 $\mu$s abort gap every 89 $\mu$s during which the digital activity and therefore the corresponding current of the modules drops to zero) has an impact on the stability of the system. As can be seen from Fig. 6 the noise distributions measured in these cases are practically identical. Both tested modules show the same result. These measurements demonstrate that in as close an approximation to the final system as can be operated at the current point in time the DC-DC converters do not have any adverse effect on the noise of the pixel modules.

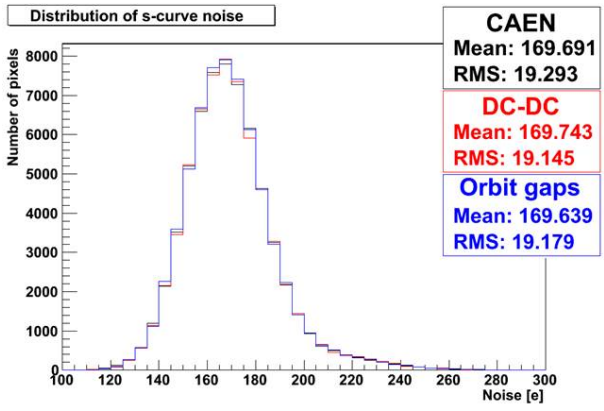


Figure 6: Noise distribution (in electrons) of all pixels on a current CMS pixel module when operated with CAEN power supplies as in the experiment today (black), by a pair of DC-DC converters with 24 converters operating in parallel (red), and when fast load changes as expected from the LHC orbit gap are simulated (blue).

One concern when operating many DC-DC converters in parallel could be that these oscillators may synchronize to each other and then cause large transients in the system. Simulations show that even a synchronization of all converters fed by the same power supply would be tolerable due to sufficient filtering [6]. Nevertheless, we have performed tests to see if synchronization actually occurs when many converters are operated in parallel. Each converter has a slightly different frequency. Synchronization would result in an alignment of frequency and phase between converters. The frequencies of 8 converters running in close proximity have been measured versus time and found to be stable. One converter has been modified such that its frequency could be varied. The frequency of a nearby operated converter was not affected when the frequency of the first one crossed the frequency of the second. Further tests were made in which a close-by frequency was imposed onto the input lines of the converter or radiated onto the converter by an external coil. In summary we were unable to observe synchronization under any realistic conditions.

## 8. Summary and Outlook

The new CMS pixel detector will be powered via on-detector DC-DC converters. This powering scheme allows the provision of twice the power of the current pixel system through the same cable plant, at reduced cable losses. The development of the converters is close to completion. Valuable support has been given by the CERN electronics group through the development of the radiation tolerant converter ASIC. The integration of the DC-DC powering scheme into the CMS pixel system has been designed. Electrical and thermal tests of individual converters and of many converters at the system level show good performance. The project is therefore now moving into the production phase. Investigations of DC-DC powering for the full CMS tracker upgrade are on-going and applications in other areas of CMS and other HEP experiments are under consideration.

## 9. Acknowledgements

We would like to thank the German Federal Ministry of Education and Research (BMBF) and the Helmholtz Alliance 'Physics at the Terascale' for their financial support. We would like to thank the CERN/PH/ESE Group for providing prototype ASICs to us.

## References

[1] M. Weber, 'Power distribution for SLHC trackers: Challenges and solutions', NIM A592 (2008) 44–55, and references therein.
[2] CMS Collaboration, 'CMS Technical Design Report for the Pixel Detector Upgrade', CERN-LHCC-2012-016, CMS-TDR-11.
[3] L. Feld et al., 'DC-DC conversion powering for the CMS tracker at SLHC', NIM A628 (2011) 453-456.
[4] K. Klein et al., 'A DC-DC conversion powering scheme for the CMS pixel detector upgrade', contribution to TWEPP-12, 2013 JINST 8 C02024.
[5] F. Faccio, S. Michelis et al., 'A complete DCDC converter ASIC for LHC upgrades', contribution to TWEPP-12, to be published in JINST.
[6] F. Faccio, contribution to ACES11, http://indico.cern.ch/conferenceDisplay.py?confId=127662.