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The ALPHA – detector: Module Production and Assembly

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ABSTRACT: ALPHA is one of the experiments situated at CERN's Antiproton Decelerator (AD). A Silicon Vertex Detector (SVD) is placed to surround the ALPHA atom trap. The main purpose of the SVD is to detect and locate antiproton annihilation events by means of the emitted charged pions. The SVD system is presented with special focus given to the design, fabrication and performance of the modules.

KEYWORDS: Particle tracking detectors; Large detector systems for particle and astroparticle physics; Particle tracking detectors (Solid-state detectors)

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1 Introduction

ALPHA is a low energy antiproton experiment located at the CERN's AD. ALPHA routinely produces cold antihydrogen in presence of a neutral atom trap [1], and recently also demonstrated its ability to trap some of the antiatoms and keep them confined over a long period of time [2, 3]. The long term goal of the ALPHA experiment is to perform high precision antihydrogen laser spectroscopy. The SVD surrounds ALPHA's atom trap and it is placed outside the antiproton beam pipe. During an antiproton annihilation, several charged pions are emitted. The pions penetrate the SVD, where upon the readout electronics records the interactions in the SVD, and the data are then used to reconstruct the antiproton annihilation vertex. The SVD consists of 60 modules (hybrids), each having two silicon sensors in them together with four charge sensitive preamplifiers. This paper gives the details of the module production and performance.

2 Detector mechanical mount

The SVD consists of 60 hybrids, set symmetrically in three layers in two opposite halves, see figure 1 and 2. The detector is placed between the beam pipe and the solenoidal magnet inner bore with physical dimensions of 140 and 260 mm in diameter, respectively, and it operates in dry air atmospheric pressure. The main emphasis in the design was to make the support structure as lightweight as possible by using aluminium alloy to avoid unnecessary scattering material along the particle trajectories. The inner aluminium drum of the detector support structure onto which the hybrid supporting structures are mounted was processed down to 400 μm thickness. None of the aluminium components were stress relief annealed. This treatment softens the material and reduces its tensile strength. To overcome the inherent residual stress of the supplied materials, rough machining of the parts was initially carried out; these parts were then left to settle naturally and unclamped before final machining. This allowed the accuracy to be maintained without risk of "movement" of the material due to the final machining process. The only additional material between the adjacent silicon layers are the 1600 μm thick Printed Circuit Board (PCB) frames onto which the silicon sensors are mounted.

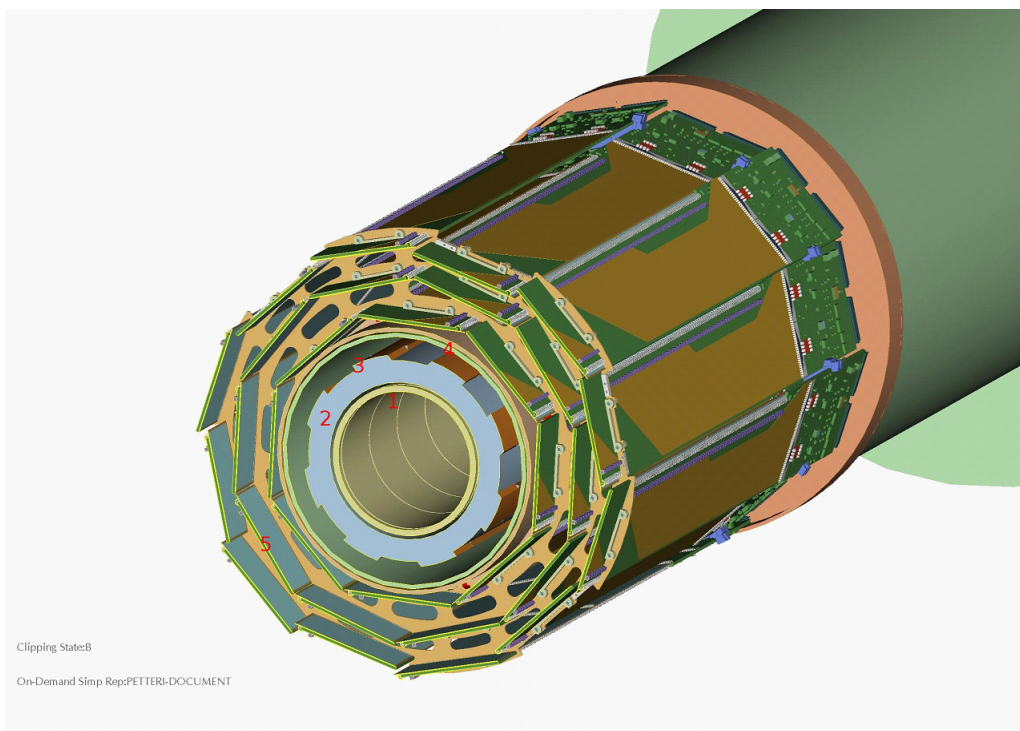


Figure 1. Cross sectional view of the ALPHA -detector hybrid arrangement. From center: 1) Trap electrodes. 2) Supporting structures. 3) Octupole winding. 4) Beam pipe. 5) Hybrids.



Figure 2. Detector in its mount frame before sealing the outer covers.

The outer shield of the detector support structure also carries ducts for air cooling. The cooling is mainly guided to the heat generating electronics. The cool, dried and filtered air is provided by two vortex tubes, removing the excess power of about 50W to atmosphere and maintaining the detector operational temperature at $23 \pm 2^\circ\text{C}$.

Table 1. Summary of the sensor parameters and the typical measured values.

Physical size	61 x 115 mm
Active area	58.1 x 112.0 mm
Typical bias resistor value	7–15 M Ω
Depletion voltage	40–50 V

	p-side	n-side
Strip length	112 mm	58 mm
Strip pitch	227 μm	875 μm
Interstrip spacing	50 μm	10 μm
Typical strip leakage current	6 nA	12 nA
Number of strips	256	128

3 Si sensors, ASICs and the PCB mount

The silicon sensors were produced by Micron Semiconductor Ltd. in the U.K. [4]. The sensors are double sided strip detectors, built in 300 μm 6 inch wafers as a standard p on n -technology. The strip pitches were chosen with the aid of Monte Carlo simulations; the large amount of scattering material between the trap walls and the detector undermines the achievable imaging resolution, so the simulations were used to avoid over- or under-specification of the strip pitches. A summary of the sensor parameters is presented in table 1. The strip active sizes are for the p-side 229 μm \times 112 mm and for the n-side 890 μm \times 58 mm. The p-side strips (ϕ -direction) are DC -coupled to the charge amplifier inputs in the Application Specific Interated Circuit's (ASIC), whereas the n-side (z-direction) strips are AC coupled using external 1 nF capacitors. Because of the DC coupling on the p-side, the sensors were carefully tested before accepting them for production as the strip leakage current flows directly into the ASIC's preamplifiers. Each ASIC handles 128 strips. Polysilicon strip bias resistors are integrated within the silicon. Resistor voltage drop and strip current were measured and tests also included IV- and CV-characteristics and a 72 h stability test. The overall acceptance criteria was less than 1% substandard strips per sensor.

Silicon sensors were mounted on the PCBs by using custom made vacuum jigs, as seen in figure 3. The PCB was positioned on the jig by using its central mount point and support bracket holes. The silicon sensors were positioned on the vacuum jigs using the sensor and jig alignment marks. An array of Araldite 2011 droplets (chosen for its low sodium content and long curing time) were silk screen printed in a defined pattern on the PCB surface. The sensors were then placed at 100 μm vertical distance from the PCB surface and left for the glue to cure. The achieved mounting accuracy was better than 50 μm , confirmed by Coordinate Measuring Machine (CMM) measurements.

The PCB itself is manufactured by Express Circuits in the UK from Nelco 4000 material which has a coefficient of expansion closer to that for silicon than standard FR4. It has 8 layers with blind vias on both faces and a gold over nickel finish, suitable for wire bonding. The signals from the silicon p-side pass the shortest distance possible to the charge amplifiers which is reflected

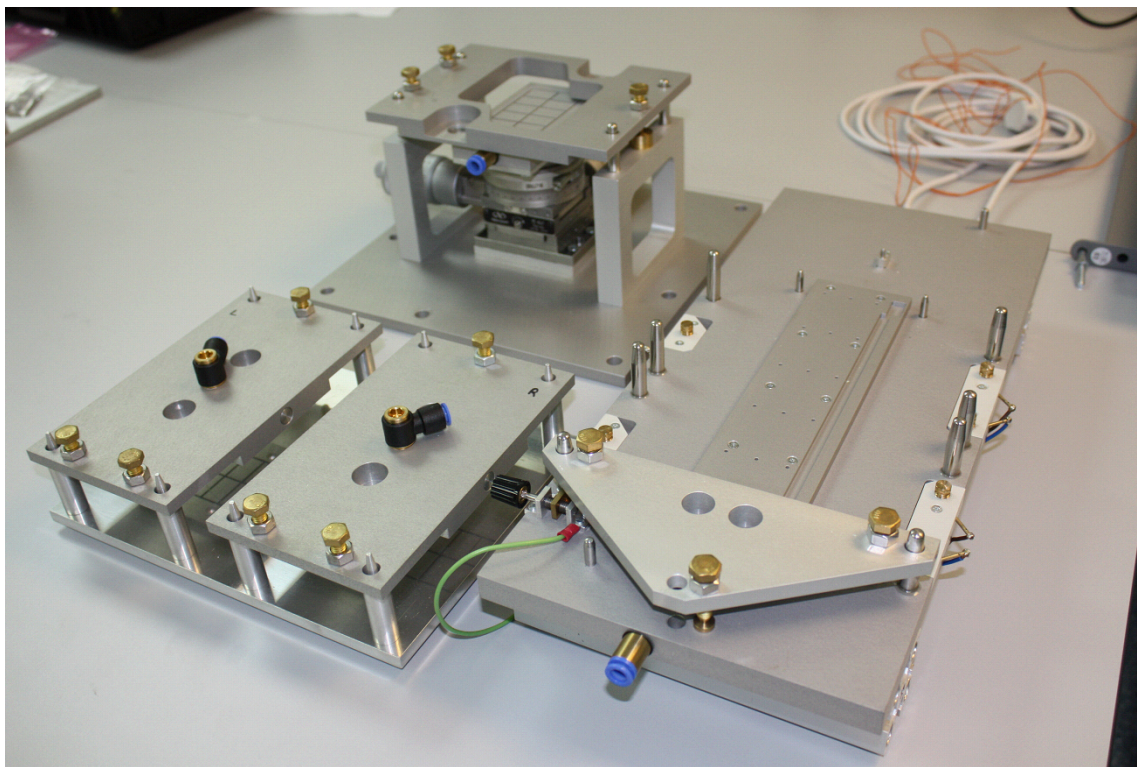


Figure 3. Silicon mounting jigs. The PCB is placed on the jig right. The rear left jig with xy -table is used to position the silicon. The two jigs at the front lift the silicon from the xy -jig on to the PCB jig.

in the noise performance of this side. The n-side signals are routed through thin copper tracks and microvias to the ASIC inputs. The ASIC signals to and from the PCB are passed through commercial CMOS buffers to isolate and protect the ASIC from noise and external charge damage. Components on the boards were hand soldered to avoid heat distortion from reflow. The overall board size is 344 mm x 61 mm. During assembly and testing the PCB is held in a machined aluminium handling frame. Plastic covers protect the units when in transit or storage. The frames and assembly jigs are anodised to prevent contamination.

A pion generated in the antiproton annihilation corresponds to one minimum ionizing particle (MIP), and generates roughly 24000 electron hole pairs in 300 μm thick silicon. The ASICs chosen were ValTa chips produced by Ideas/Gammamedica, Norway [5]. The linear input range of the ASICs is about ± 10 MIPs, with the + and - corresponding to p- and n-side readouts, respectively. The ASICs have 128 input channels and they produce a fast 75 ns trigger pulse and slow analogue signal, typically with 1 μs shaping time. All chip parameters are programmable. The chip also contains a single event upset recovery circuit. The ASIC schematics are shown in figure 4.

The detector assembly consists of the following steps and quality control measures:

1. PCB cleaning and PCB and silicon visual inspection;
2. Silicon electrical tests;
3. ASIC and pitch adaptor glueing on populated PCBs, ASIC back -end wire bonding to the PCB; ASIC functionality test;

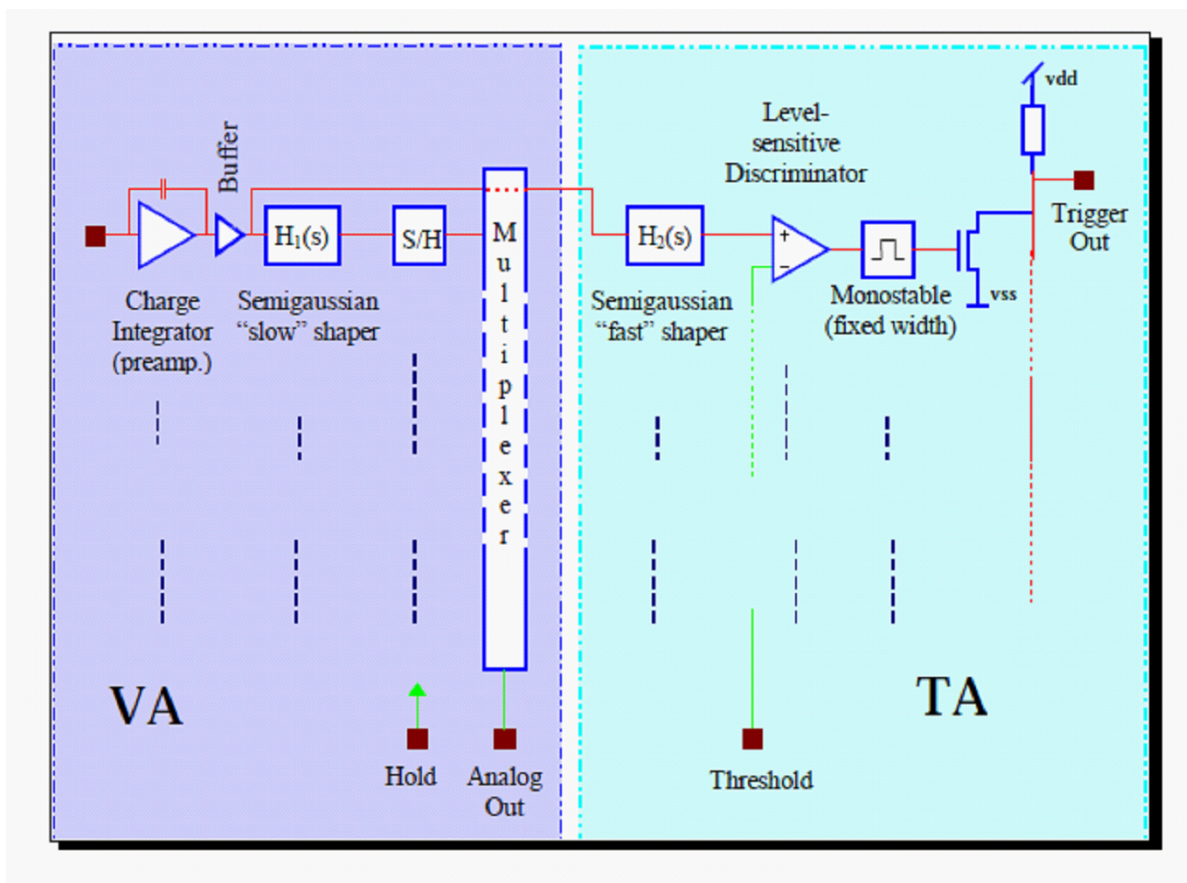


Figure 4. Schematics of the Va1Ta chip.

4. ASIC front-end wire bonding to pitch adaptors; retest.
5. PCB to pitch adaptor bonding;
6. Pre-silicon functionality test;
7. Silicon assembly on the PCB. CMM measurement of the silicon locations;
8. PCB – silicon strip wire bonding; Post silicon test;
9. Module mounting in the detector support frame; Functionality test.
10. Final tests for the completed detector.

During these steps there are three visual inspections, one metrological measurement and nine electrical tests for each module. There are all together 1144 ultrasonically bonded wires in each module, bonded with the Kulicke & Soffa 8090 bonding machine. The bonds were carefully tested and had high quality as indicated in figure 5. During the final test no unexpected behaviour was observed. Shorted or high current strips (denoted as “substandard” above) were bonded together and guided to a single channel or the bonds disconnected, as appropriate. Such cases including noisy channels in the ASICs, amounted 10 out of the total 30720 readout channels. A completed module is shown in figure 6.

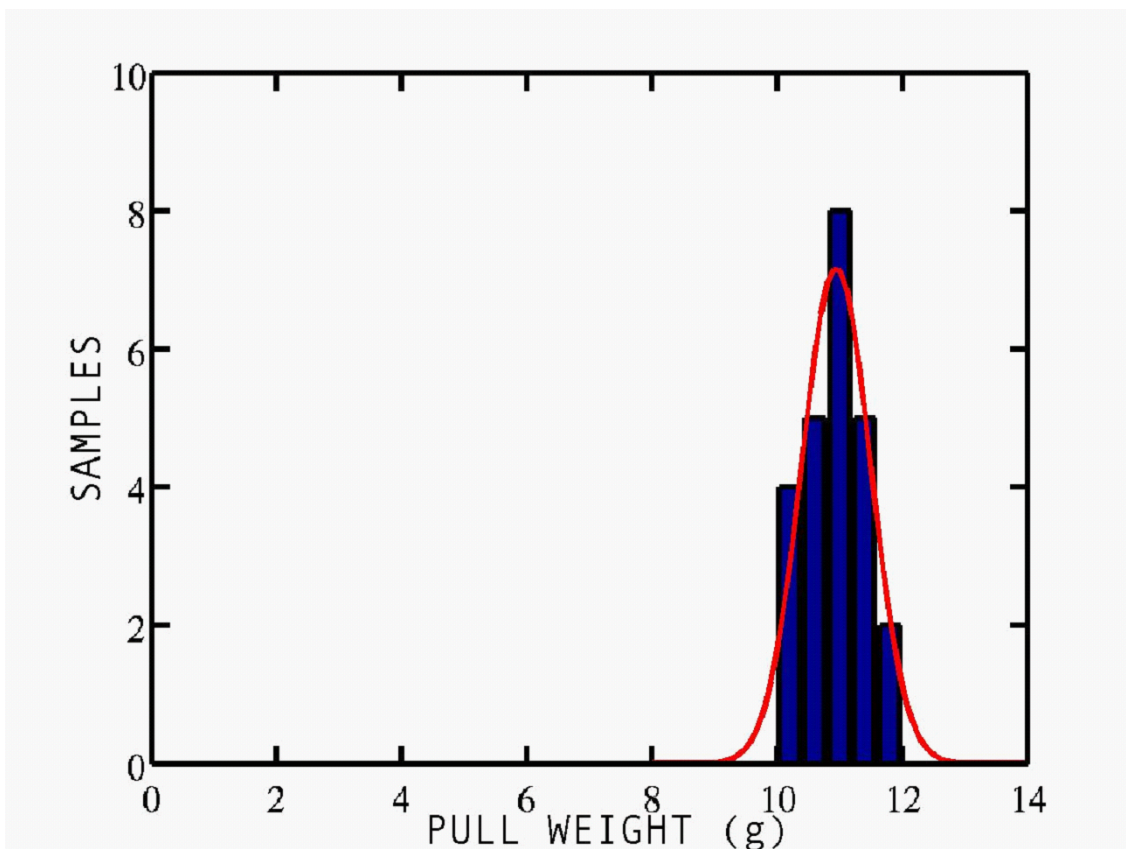


Figure 5. Sample of 25 wire bonds pulled off between pitch adaptor and the silicon bonding pad. The histogrammed quantity is the critical force (expressed in grams) to break the bond wire. These figures were determined from modules which required reworking during manufacture.

4 Module performance

The modules were carefully monitored throughout the assembly by measuring the pedestal noise, test pulse response, trigger threshold levels and the cosmic muon spectra. Typically the RMS noise level is around 11 and 7 mV in n- and p-sides, respectively. The ASIC has a 1V dynamic output range. The test pulse response typically is 42 and 55 mV/fC in the n- and p-sides, respectively. The linearity of the response to the injected charge was also monitored. The MIP signal to noise ratio, defined as the median of the cosmic background Landau distribution versus the RMS noise, has typical values of 15 and 33 in the n- and p-sides, respectively. The more modest S/N ratio on the n-side is due to the long copper wires carrying the signal from the strips through the PCB to the ASICs. The extra capacitance introduced by these wires both increases the noise as well as lowers the gain. The overall detector performance is equivalent to that reported with similar module setups, e.g., in [6]. The S/N ratios when while recording the actual annihilations, e.g., in [2, 3], are very similar to the figures mentioned above but will be discussed in detail in a forthcoming article. The vertex reconstruction is described in [7].

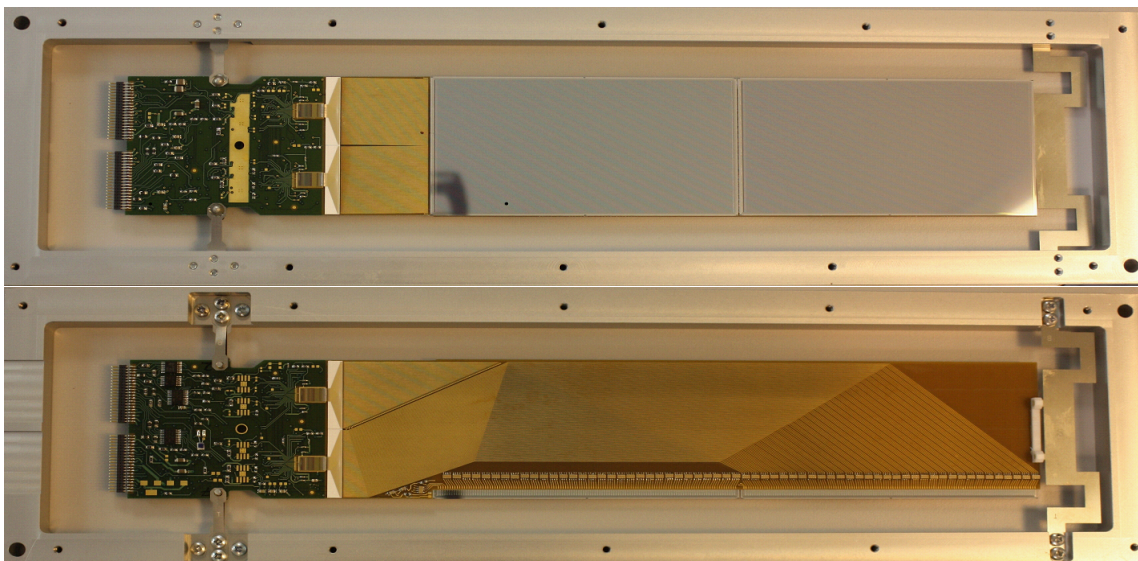


Figure 6. Upper: hybrid p-side up. The horizontal strips are wire bonded together between the adjacent silicon sensors forming effectively a 230 mm long strip. Lower: The vertical n-side strips are bonded to the backside of the hybrid, connected to the external coupling capacitors and further wired through the PCB to the ASICs. The hybrids are positioned using three mount points; the center mount point symmetrically left between the ASICs and the plastic pin locator (shown on the n-side picture rightmost) which attaches to two pins on the central mounting disc in the final device.

5 Conclusions

The first version of the ALPHA SVD has now had more than two years of stable operation installed inside the ALPHA apparatus. All the module characteristics have remained intact over this period of time. Currently new module production as well as mechanical design has restarted in the Liverpool Semiconductor Detector Centre for the second stage of ALPHA. The new design is similar to the existing one but it will be mounted on larger radii. The expected radiation load of the SVD in the new ALPHA -apparatus is 10^9 (200 MeV pions)/cm²/yr indicating that the silicon sensor performance will not deteriorate over the lifetime of the detector by radiation induced damage.

Acknowledgments

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