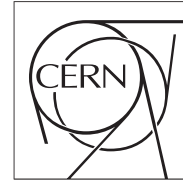


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A DC-DC Conversion Powering Scheme for the CMS Phase-1 Pixel Upgrade

Lutz Feld, Martin Fleck, Marcel Friedrichs, Richard Hensch, Wacław Karpinski, Katja Klein, Jan Sammet and Michael Wlochal for the CMS Collaboration

Abstract

The CMS pixel detector was designed for a nominal instantaneous LHC luminosity of $1 \cdot 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. During Phase-1 of the LHC upgrade, the instantaneous luminosity will be increased to about twice this value. To preserve the excellent performance of the pixel detector despite the increase in particle rates and track densities, the CMS Collaboration foresees the exchange of its pixel detector in the shutdown 2016/2017. The new pixel detector will be improved in many respects, and will comprise twice the number of readout channels. A powering scheme based on DC-DC conversion will be adopted, which will enable the provision of the required power with the present cable plant.

The powering scheme of the CMS pixel detector will be described, and the performance of prototype DC-DC buck converters will be presented, including power efficiency, system tests with DC-DC converters and pixel modules, thermal management, reliability at low temperature, and studies of potential frequency locking between DC-DC converters.

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KEYWORDS: Voltage distributions; Particle tracking detectors; Si microstrip and pad detectors.

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1. The CMS Phase-1 Pixel Upgrade

The instantaneous luminosity of the LHC will increase during Phase-1 of the LHC upgrade from its design value of $1 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ to a value of about $2 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. While the CMS pixel detector works very well at the present luminosity, and will continue to work well up to the LHC design luminosity, unacceptably large inefficiencies are predicted for the expected hit rates at Phase-1 luminosities. The present pixel detector will therefore be replaced with an improved device, to be installed in the extended shutdown 2016/2017 [1].

The new pixel detector will be improved in many respects. In particular, a new readout chip with increased buffer sizes and the transition to digital readout will decrease inefficiencies. The material budget will be reduced by the deployment of an ultra-light mechanical support structure and the change to an evaporative CO₂ cooling system, as well as through the relocation of electronic boards. The layout of the detector will also be changed: while the present CMS pixel detector consists of three barrel layers (BPIX) and two disks per side (FPIX), the new detector will comprise four barrel layers and three disks per side. While this will lead to more robust tracking and improved track resolutions, it also leads to a factor of 1.9 more readout channels, and consequently a factor of 1.9 higher front-end power consumption. This power must be provided through the already installed cable plant, as access to services is very limited, and since cable channels are full already, excluding the installation of a significant number of additional cables. Doubling the front-end power consumption leads to an increase of resistive losses on the long (50 m) supply cables by a factor of four, which implies an unacceptable head load in the cable channels. A novel powering scheme based on the DC-DC conversion technique will therefore be required to power the Phase-1 CMS pixel detector.

2. A DC-DC Conversion Powering Scheme for the CMS Phase-1 Pixel Detector

Custom DC-DC buck converters, described in detail in the next section, will convert the input voltage of about 10 V to output voltages of 2.4 V and 3.0 V, which are the voltages required by the analogue part of the readout chip and the digital module electronics, respectively, including the voltage drops on the supply tube. Consequently two types of DC-DC converters are used, in the following referred to as “analogue DC-DC converters” and “digital DC-DC converters”. The conversion ratio of 3-4 leads to a reduction of resistive losses on supply cables by a factor of about ten.

The DC-DC converters will be installed at the far end of the mechanical support structures of the pixel detector: on the supply tube for BPIX and on the service cylinder for FPIX (Fig. 1 (left)). With a distance of about 2.2 metres to the interaction point, the DC-DC converters are located outside of the tracking region. The material budget of these devices is therefore not as critical as in applications where the DC-DC converters would be installed close to the detector modules. In addition, the large distance to the pixel modules reduces the risk of electro-magnetic interference. In the case of BPIX, the DC-DC converters will be installed in “slots” on the supply tube, as shown in Fig. 1 (left). The cooling pipes of the evaporative CO₂ cooling system pass through these slots and are used to remove the heat, caused by unavoidable inefficiencies, from the DC-DC converters. The DC-DC converters are plugged into Printed Circuit Boards named “bus boards” (Fig. 1 (right)). Up to thirteen pairs of DC-DC converters, where one pair consists of an analogue and a digital DC-DC converter, are connected to one bus board. Six or seven pairs of DC-DC converters are powered through one cable from one power supply. The number of pixel modules that are supplied from one pair of DC-DC converters varies between one for the innermost layer and four for the outermost layer of modules, due to the dependence of the digital current on hit rate and thus layer radius. The

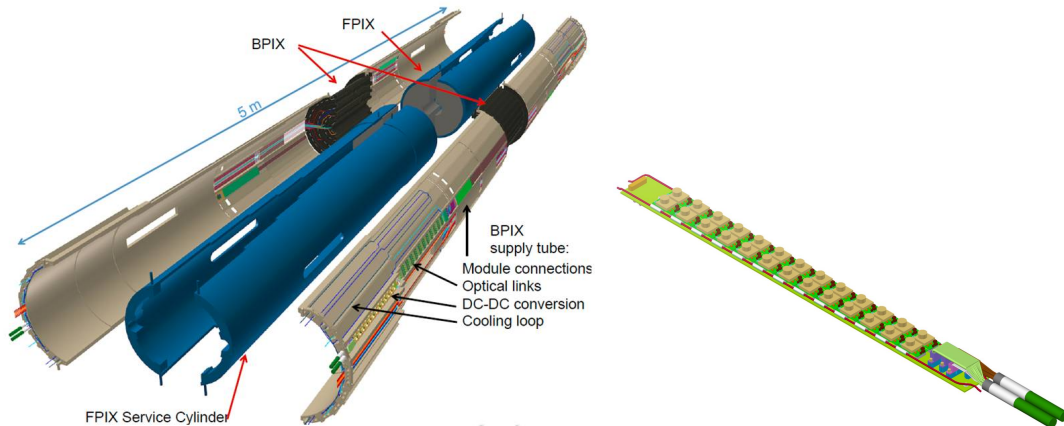


Figure 1. Left: exploded view of the CMS Phase-1 pixel detector. The barrel is drawn in black and is labelled “BPIX”, while the forward disks are drawn in dark gray and are labelled “FPIX”. The FPIX service cylinders are shown in blue, and the BPIX supply tube is pictured in light grey. One slot of the supply tube is populated with electronic components, including the DC-DC converters, labelled “DC-DC conversion”. Right: CAD-drawing of the BPIX bus board with thirteen pairs of DC-DC converters.

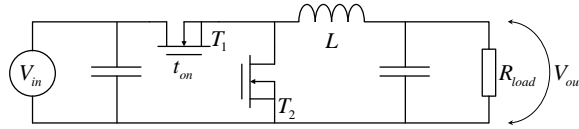


Figure 2. Simplified schematic of a buck converter.

required output current of a single DC-DC converter is always below 3 A. The integration of DC-DC converters into FPIX is conceptually very similar. In total, 1184 DC-DC converters will be installed in the Phase-1 pixel detector.

3. DC-DC Converter Development and Performance

The DC-DC step-down converters foreseen for the pixel detector are of the “buck” type. The basic schematic is shown in Fig. 2. Two power transistors, T_1 and T_2 , act as switches. They are periodically switched on and off with a switching frequency f_s , such that during a time t_{on} transistor T_1 is conducting and T_2 is open, while during time $T - t_{on}$, where $T = 1/f_s$, T_2 is conducting and T_1 is open. In this way the load is periodically connected to and disconnected from the power supply. The ratio t_{on}/T is the duty cycle, D , of the converter. An inductor stores energy up to the time t_{on} and releases it during the time $T - t_{on}$. The core of the inductor has to be made of non-magnetic material, since all ferrites would saturate in the 3.8 T magnetic field present in the CMS tracking volume. Capacitors at the in- and output of the converter bypass AC components. A feedback loop based on the Pulse Width Modulation technique (not shown in the figure) stabilizes the output voltage at a hardware-programmable value.

Radiation-tolerant buck converter ASICs are under development in the PH-ESE group of CERN, using a 0.35 μm CMOS process. The chip includes the power transistors and the drivers to operate them, as well as the control circuitry, whereas the inductor and the filter networks are external.

Current CMS buck converter prototypes, named AC_PIX_V8, are based on the most recent ASIC prototype, AMIS4 [2]. The two-layer PCB has an area of 2.8 x 1.6 cm^2 (Fig. 3 (left)). A toroidal plastic-core inductor with an inductance of 450 nH is used, and the switching frequency is configured to 1.5 MHz. Pi-type filters are installed both at the input and the output. The fully populated converter boards have a weight of about 2 g. The DC-DC converters are equipped with a shield, as shown in Fig. 3 (right).

About 60 AC_PIX_V8 DC-DC buck converters were produced. In the remainder of this note, their performance will be discussed.

3.1 Power Efficiency

The power efficiency, defined as the output power divided by the input power, is one of the most important properties of a DC-DC converter. The efficiency has been measured as a function of both input voltage and output current. Figure 4 (left) shows the mean efficiency from twelve AC_PIX_V8 converters with an output voltage of 2.5 V. Except for very low output currents, the efficiency is close to or even above 80 %. For an output voltage of 3.0 V, the efficiencies are typically 2 % (absolute) higher. The efficiency is also very uniform - the standard deviations, calculated for each

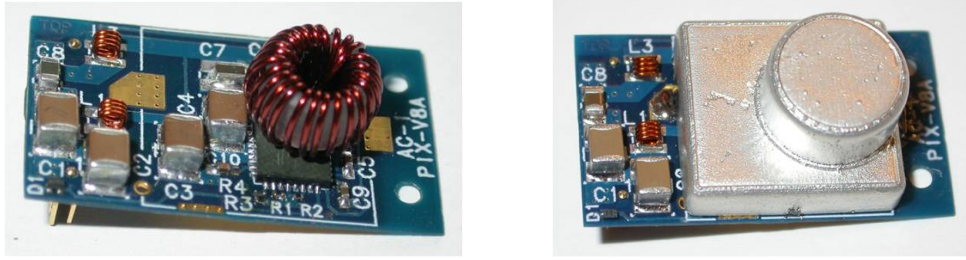


Figure 3. AC_PIX_V8 DC-DC buck converter prototype without (left) and with (right) shield.

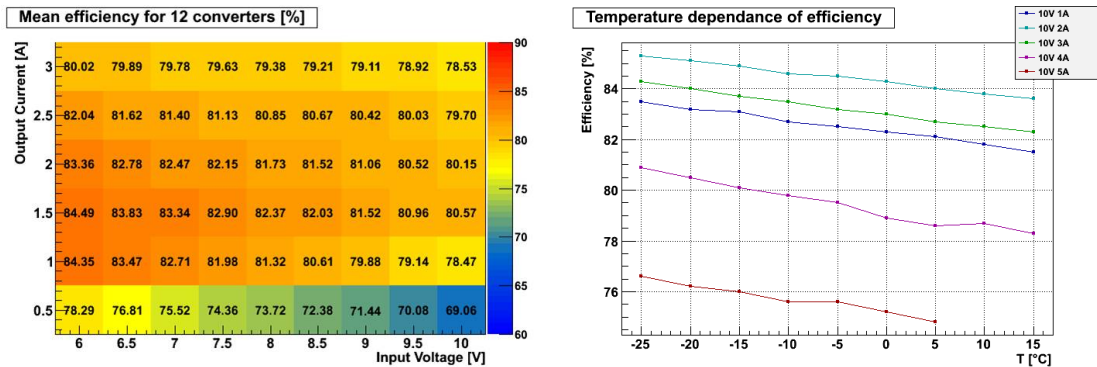


Figure 4. Left: mean power efficiency, calculated from twelve AC_PIX_V8 DC-DC converters with an output voltage of 2.5 V. Right: dependence of the efficiency on the cooling block temperature, for an AC_PIX_V8 converter with 3.3 V output voltage, an input voltage of 10 V and different output currents (dark blue: 1 A; light blue: 2 A; green: 3 A; violet: 4 A; red: 5 A).

output current and input voltage from the same twelve DC-DC converters, amount to 0.5 % or below (except for very small currents).

The efficiency has also been studied as a function of the switching frequency, which can be adjusted via a resistor on the PCB. The efficiency is maximal for the default switching frequency of 1.5 MHz. The efficiency decreases both for lower and higher frequencies, in the first case due to higher conduction losses, in the latter case due to larger switching and driving losses.

The efficiencies quoted above have been obtained in a set-up where the DC-DC converter is attached to a copper cooling block, which is kept at +20 °C. In the pixel detector, the converters will be cooled to lower temperatures. Lower operating temperatures lead to a reduction of Ohmic losses and thus to a higher efficiency. Figure 4 (right) shows the measurement of the efficiency versus cooling block temperature, for various output currents. The efficiency increases typically by an absolute 0.05 % per degree C reduction. The increase in efficiency, when moving from room temperature to a coolant temperature of below -20 °C, will therefore roughly amount to 2 % (absolute).

3.2 Shielding

The DC-DC converters are equipped with a shield. This shield serves three purposes: it reduces

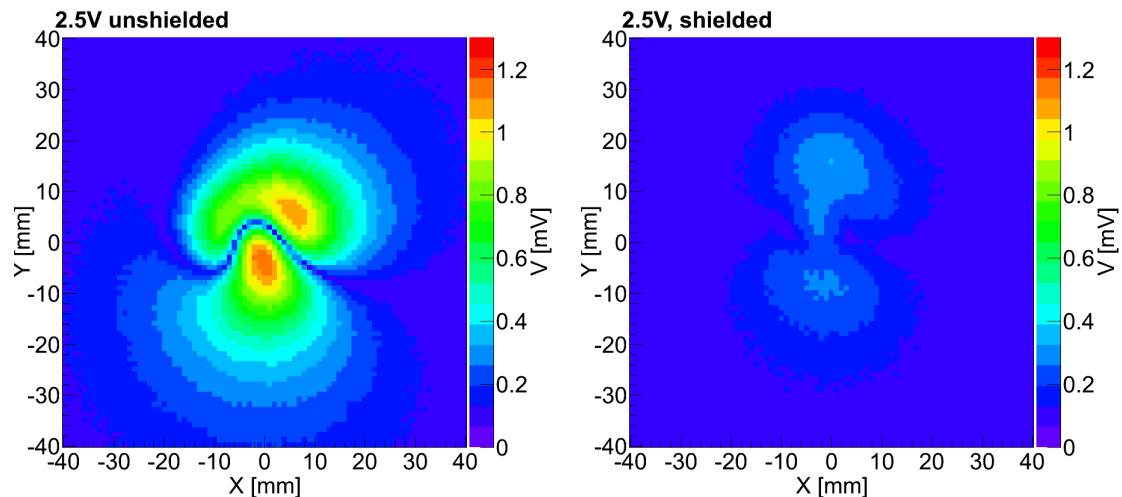


Figure 5. Magnetic emissions of an AC_PIX_V8 DC-DC converter, at a distance corresponding to a height of 1.5 mm above the shield. The field component perpendicular to the PCB plane is presented. The colour-coding shows the voltage induced in a magnetic near field probe. Left: without shield, right: with shield.

electro-magnetic radiation from the coil, it segregates noisy parts of the PCB from quiet parts, thus preventing the coupling of noise from one part of the buck converter to another, and it acts as cooling contact for the coil.

Due to space constraints in the BPIX supply tube slots, the shield is of complex shape. Various shielding technologies have been studied. The currently favoured option consists of a plastic body of 0.3 mm thickness, galvanically coated with a 30 μm thick layer of copper, plus a 1 μm thick tin layer, deposited by electroless plating, to improve solderability. For the body, both rapid prototyping and injection molding are under consideration for the upcoming mass production.

Figure 5 shows a measurement of the inductor's magnetic field, measured with a near field probe both with and without shielding. The measurement was performed with the latest prototype shield, shown in Fig. 3 (right), whose body was produced with rapid prototyping. The magnetic field is strongly reduced, down to a level that is acceptable. Further measurements showed that the shield also significantly reduces high-frequency components in the Common Mode output noise spectrum [1].

3.3 Thermal Studies with Single DC-DC Converters

The DC-DC converters need to be cooled, to remove the heat caused by their inefficiency of 20%. The critical components are the chip and the inductor. A ground plane on the back side of the PCB services to cool the chip down, through thermal vias. The inductor is cooled through conduction by the shield, which is filled with thermal grease and is soldered via four contacts to the PCB. An overtemperature protection circuit in the AMIS4 ASIC switches the chip off when its temperature increases above 75-80 $^{\circ}\text{C}$.

The temperatures of the inside of the inductor as well as of the chip QFN32 package have been measured using thermistors. Figure 6 (left) shows a measurement of the inductor temperature, with the cooling block at room temperature. The presence of the shield reduces the coil temperature by

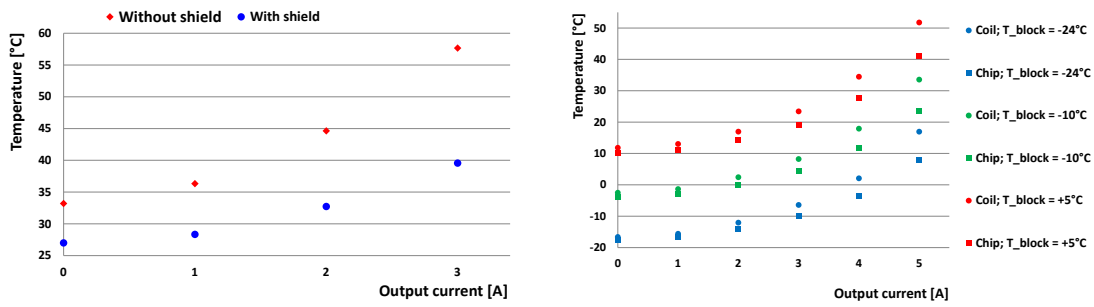


Figure 6. Left: temperature as measured inside the inductor coil, with (blue circles) and without (red diamonds) the shield mounted. Right: temperature of the chip package (squares) and inductor (circles) for different cooling block temperatures: -24°C (blue), -10°C (green), and $+5^{\circ}\text{C}$ (red).

up to 20 K, depending on the output current of the DC-DC converter. This proves the viability of the cooling concept.

The chip package temperature and inductor temperature are shown in Fig. 6 (right), as a function of the output current, for three different cooling block temperatures. Even for output currents as high as 4-5 A and a cooling block temperature of $+5^{\circ}\text{C}$, the measured chip and inductor temperatures are well below any critical value.

3.4 The DC-DC Bus Board

The bus board distributes input and output voltages as well as control signals and sensor bias lines. The 8-layer board has a size of 488 mm x 40 mm x 1.6 mm. A prototype version serving twelve DC-DC converter pairs has been developed, and its electrical and thermal behaviour extensively studied. In particular, good control of output voltage drops is important, as no remote sensing is used at the DC-DC converters' output. Calculated and measured voltage drops agree well, and no degradation of resistances was observed after 120 thermal cycles between -10°C and $+40^{\circ}\text{C}$, under full load.

3.5 Cold Test of a Fully Equipped Bus Board with CO_2 Cooling

In the pixel system, the DC-DC converters will be screwed to aluminium cooling bridges, which in turn will clamp around the cooling pipes (Fig. 7 (left)). The cooling bridges consist of two parts: the lower parts are glued to the bus board, and the upper parts are screwed onto the lower parts. Two DC-DC converters are screwed to the upper part of each cooling bridge. This concept was tested in the lab, using a recirculating CO_2 cooling system [3] and a prototype bus board equipped with 24 DC-DC converters. The pipes and the bus board were installed in an evacuated box. Pipes with an inner and outer diameter of 1.7 mm and 2.0 mm, respectively, were used. The CO_2 temperature was set to -20°C , and thermistors were used to measure the temperatures on the pipes, the cooling bridges and the DC-DC converters. A programmable load was used to mimic the load of the DC-DC converters due to the pixel modules.

The result of this cooling test is shown in Fig. 7 (right). All DC-DC converters operated properly and temperatures were stable. For the maximum nominal load of 3 A per converter, the temperature

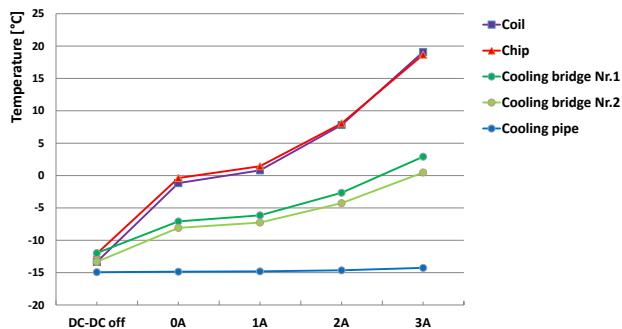
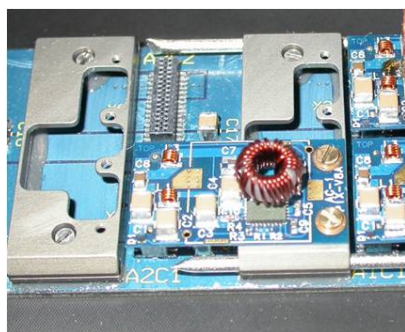


Figure 7. Left: a mock-up illustrating how the cooling bridges clamp around the cooling pipes, and how the DC-DC converters are screwed to the cooling bridges. Right: thermistor temperatures versus load as measured during the CO₂ cold test. The curves show the temperature of the chip (violet) and coil (red) of a DC-DC converter that was equipped with a shield, the temperatures of two cooling bridges (dark and light green), and the temperature of the cooling pipe (blue).

difference between the DC-DC converter chip or coil and the cooling bridges is about 20 K, a value that is compatible with earlier test bench measurements with single converters (Sect. 3.3). However, there is an additional temperature difference of about 15 K between the cooling bridges and the pipe. Finite Element simulations have been launched to understand the potential for improvement in the cooling bridge design.

3.6 System Tests with CMS Pixel Modules

System tests with real pixel detector modules have been performed to investigate potential degradation of detector performance due to the use of DC-DC converters. Since pixel modules with the new readout chip are not available yet, all system tests have been performed with present pixel modules, which are very similar to the future ones.

AC_PIX_V8 DC-DC converters provided the required 3.0 V and 2.4 V. Eight DC-DC converters were plugged into a small version of the prototype bus board. The original pixel power supplies and supply cables were used, and the cabling between the DC-DC converters and the pixel modules was made as realistic as possible. A threshold scan was performed and the S-curve of each pixel was fit with an error function to determine its width, as a measure of the pixel noise. Arrangements with one or two pixel modules and up to eight DC-DC converters were studied. In measurements with two pixel modules, these were powered either both from the same pair of DC-DC converters or each from its own pair. All measurements are compared with measurements in which the modules were powered conventionally, i.e. directly from the power supply. An active load was used to investigate different load conditions: just the load from the two connected pixel modules; a constant load of 2 A applied to all digital DC-DC converters, so that they operate under nominal load; and fast digital load changes between 0 A and 2 A, as expected from the time structure of the LHC beam (3 ms abort gap every 89 ms), due to the sparsified readout of the pixel modules.

As an example, Fig. 8 shows the result of a measurement where both pixel modules were powered from the same DC-DC converter pair. For constant loads, no difference is observed between conventional powering and powering with DC-DC converters. Also for fast load changes, powering

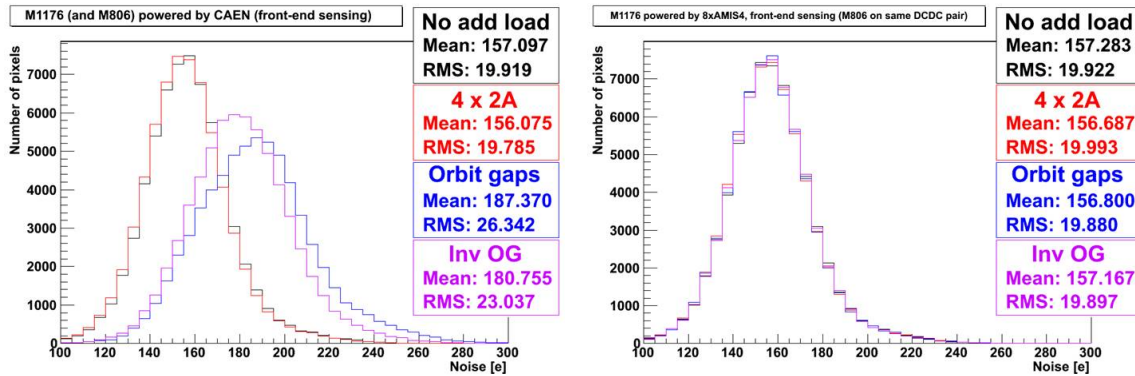


Figure 8. Distributions of the noise (width of the S-curve) of all pixels of one pixel module, in an arrangement with eight AC_PIX_V8 DC-DC converters, from which one pair was used to power two pixel modules. Measurements have been performed without (left) and with (right) DC-DC converters, for the following four cases: no additional load (black); an additional constant load of 2A on each digital line (red); a variable load as expected due to orbit gaps on each digital line (blue); and a variable load corresponding to an inverted orbit gap pattern on each digital line (pink).

with DC-DC converters does not increase the module noise, and the DC-DC conversion powering scheme appears to be more stable than conventional powering. This is believed to be due to their local regulation relatively close to the pixel modules, and due to the filters on the PCB.

System tests with two pixel modules and 24 DC-DC converters on a bus board have started, and show no noise increase so far.

3.7 Thermal Cycling of DC-DC Converters

DC-DC converters have been subjected to thermal cycles for two purposes. First, depending on the DC-DC converter’s power state and on the CO₂ temperature, the DC-DC converter temperature can vary over a wide range. Second, thermal cycling leads to accelerated aging in electronic components, which is useful for the assessment of the long-term reliability of these components.

Eight AC_PIX_V8 DC-DC converters were operated in a dedicated cold box, equipped with fast Peltier-based cooling. Within 17 hours, 15 cycles between -30 °C and +35 °C cooling block temperature were performed. All DC-DC converters worked well both during and after the thermal cycling.

3.8 Synchronization of DC-DC Converters

Oscillators of all types can lock in frequency and phase, if they are sufficiently well coupled. Many examples for such a synchronization exist in nature. The DC-DC converters on one bus board are also coupled to each other, e.g. through the common input power line or through the system ground. Their synchronization, if present, could increase the noise on the input power line.

A couple of tests have been performed with the purpose of observing, inducing and studying such an effect. The DC-DC converters’ switching frequency was measured with a pick-up probe and a spectrum analyzer. An oscilloscope was used to measure the relative phase between the switching of two DC-DC converters.

While the nominal switching frequency is 1.5 MHz for all converters, parallel operation of eight DC-DC converters showed that the converters' switching frequencies have a considerable spread. On the other hand, by chance, two pairs of DC-DC converters showed very similar frequencies. Tests were performed to study a potential influence, i.e. instability or change in switching frequency, between adjacent DC-DC converters with similar frequencies. For example, the switching frequency of one converter was changed with a potentiometer. No effect was observed when the switching frequency of this variable converter approached or crossed the (fixed) switching frequency of the other converter. An attempt was also made to influence the converter behaviour through external disturbances. Both radiative disturbances, through an external coil, and conductive disturbances, by means of a current probe clamped around the input power cable, were attempted. The frequency of the converter under test was not shifted or disturbed, and it did not lock to the disturbance signal.

In all realistic test conditions, no frequency or phase locking between DC-DC converters or of DC-DC converters to external signals was observed.

4. Conclusions

A DC-DC conversion powering scheme is foreseen for the CMS Phase-1 pixel upgrade. DC-DC converter prototypes, based on the AMIS4 ASIC, were developed and characterized. Test results are very positive; in particular, efficiencies above 80 % are reached, and no negative effect on the performance of the pixel modules has been found so far in system tests. First thermal and electrical tests with a fully equipped bus board were also successful.

The next step is to move to the AMIS5 ASIC, the successor of the AMIS4. Tests will be repeated, and, if successful, mass production will be launched in late 2013.

Acknowledgments

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