A new portable test bench for the ATLAS Tile Calorimeter front-end electronics

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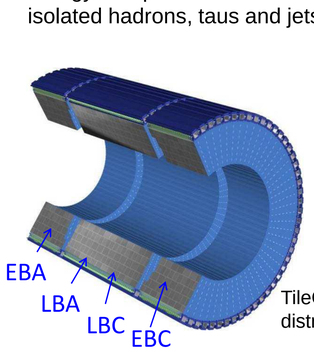
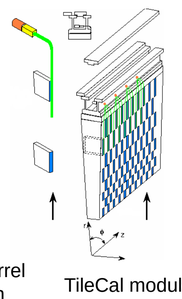
The ATLAS Tile Calorimeter

Background

The ATLAS Tile Calorimeter (TileCal) is the central section of the hadronic calorimeter of the ATLAS experiment at the CERN Large Hadron Collider. It provides accurate energy and position measurements for electrons, photons, isolated hadrons, taus and jets.



TileCal barrel distribution



TileCal module

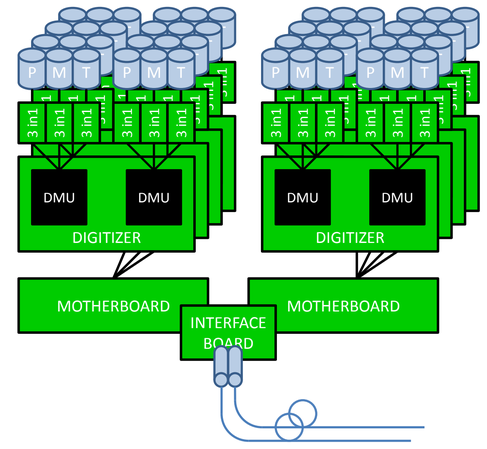
Front-end electronics

TileCal is a sampling calorimeter with steel as absorber medium and scintillating tiles as active material. The calorimeter readout is divided in four cylindrical partitions: two central sections (Long Barrels LBA and LBC) and two endcaps at higher pseudorapidity (Extended Barrels EBA and EBC). These four partitions are azimuthally segmented in 64 instrumented wedges (modules) where the scintillating plastic tiles that produce light in the interactions with the particles are arranged in 3D geometrical cells.

One module hosts up to 48 photomultiplier tubes (PMTs), that convert the light collected in their correspondent cells to an electrical pulse, which is digitized on a subsequent step. The total number of read-out channels is 9856. Data on these channels are transmitted to the back-end electronics for their processing.

The front-end electronics is housed at the outermost region of the modules in so-called super-drawers. The base element in a super-drawer is the Motherboard. It provides low voltage power and digital control signals to four digitizer boards, one interface board and the circuits needed for the L1 trigger summation and distribution. Two Motherboards form a TileCal super-drawer, which includes all the electronics for reading a complete module.

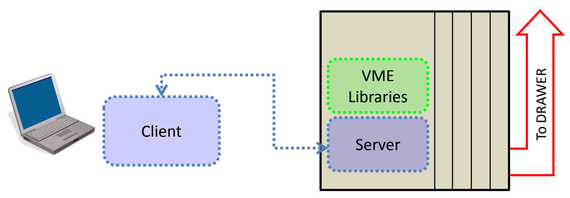
There is a 3-in-1 card connected to each PMT that provides power, control, calibration and pulse shaping functionality. The digitizer boards are in charge of the analog to digital conversion, implement pipeline memories and host a TTCrx chip for the Timing Trigger and Control signals reception. An Interface board collects the sampled data from the all the digitizers, serializes and transmits them to the back-end electronics using optical links.



Current Test Bench

Introduction

MobiDICK (Mobile Drawer Integrity Checking system) is a test bench designed to certify the TileCal super-drawers during maintenance periods. The functionality of the test bench relies on a set of hardware, with a total weight of 20 kg.



VME crate

Hardware

Previous versions of the test bench were based on a custom aluminum box containing a VME crate populated with boards, and a laptop as user interface. The VME modules deploy the functionalities needed to control and read-out the super-drawers.

Module	Function
RIO2 VME Processor	System manager
SLINK **HOLA** cards	Optical interface for super-drawers data
VME **CANbus** interface	Communication with detector infrastructure system
TTCvi/TTCex	Distribution of configuration timing and trigger commands to the super-drawer
CAEN VME **ADC** module	Digitization of trigger analog signals for muon and hadron selection.
HV power supply	+12 V /-830 V power supply for PMTs operation
LED driver board	Generation of LED pulses for calibration PMTs

Software

The MobiDICK software is based on a client/server architecture that communicates using TCP/IP.

The operator interfaces the system through the client software. The client requests the tests, the server performs them and returns the results. The client displays the results on the laptop in a friendly way.

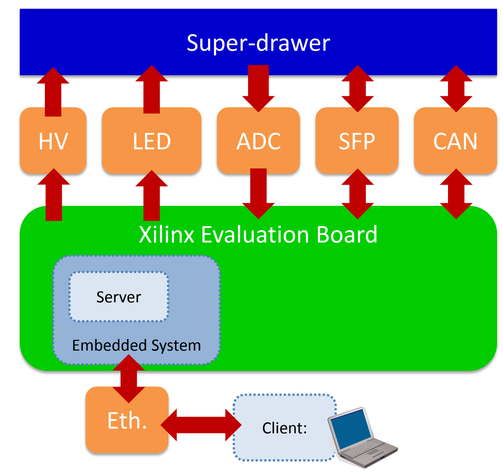
	Server	Client
Platform	VME processor	Laptop
Language	Written in C	Written in C++
Operative system	LynxOS	Linux

Why a new test bench?

- At the present time there are three available units. A fourth one is required for the long shutdown of 2013 to test the four barrels at the same time.
- There is no replacement for some old VME modules.
- Aim for a reduction of size with a total weight of 3 kg.
- Evaluation of new technologies for the future upgrade of the Tile calorimeter electronics.

Basics of MobiDICK4

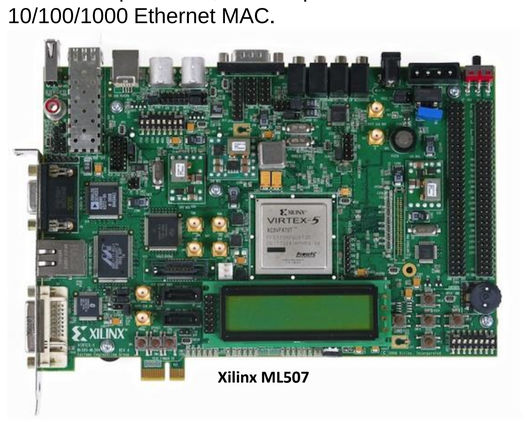
MobiDICK4 substitutes the VME crate of the previous versions with a Xilinx FPGA evaluation board. The functionality of the VME modules is replaced using an embedded system, programmable logic and some custom made PCBs.



MobiDICK4

Motherboard

The motherboard of MobiDICK4 is a Xilinx ML507 evaluation platform, which is based on a Virtex-5 device. Besides the programmable logic, this FPGA populates hardwired resources as a PowerPC 440 RISC microprocessor, 4.25 Gbps GTX transceivers or a 10/100/1000 Ethernet MAC.



Xilinx ML507

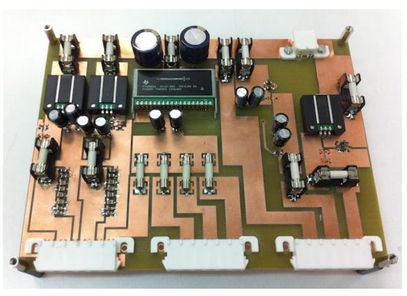
The ML507 also includes 256 MB of DDR2 RAM, as well as configuration storage solutions like platform flash devices or a CompactFlash card-based system configuration controller (System ACE Controller).

To communicate to the outside world, the motherboard has serial ports, SFP socket, RJ45 and USB host and peripheral connectors.

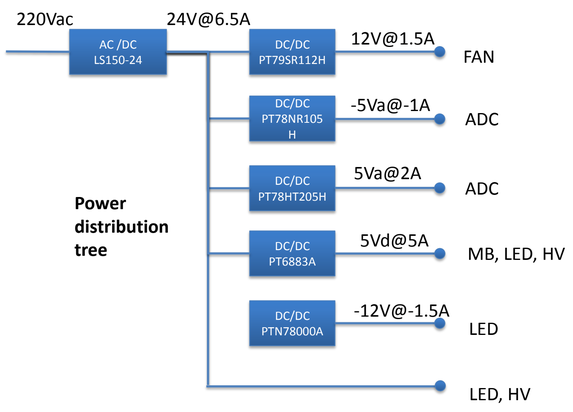
Power distribution

A commercial AC/DC converter and a custom PCB populated with many DC/DC converters provide the different voltages to the rest of the devices of the test bench.

AC/DC converter

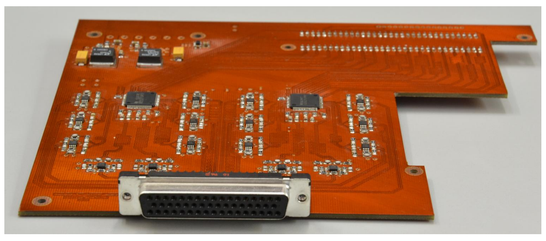


Power distribution board

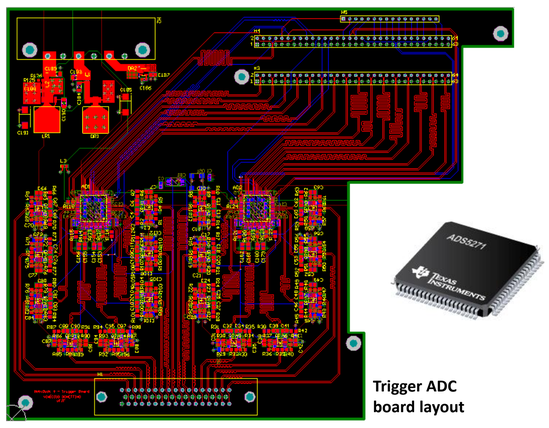


Trigger ADC board

A custom card receives and digitizes the analog trigger outputs of the super-drawer with the LHC 40.08 MHz clock. It is a four-layer PCB that hosts two Texas Instruments 8-channel 12-bit ADC chips (ADS5271), the analog differential input stages for every channel, clock oscillator and buffers.



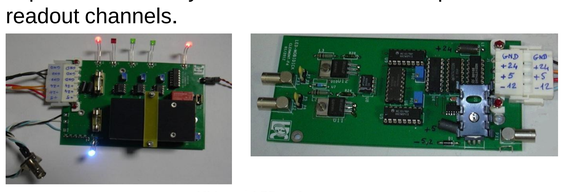
Trigger ADC board



Trigger ADC board layout

HV and LED driver

A HV board turns on the -830 V power supply using a TTL controlled relay. A LED driver board outputs the 20 V pulses necessary for calibration of the super-drawer readout channels.



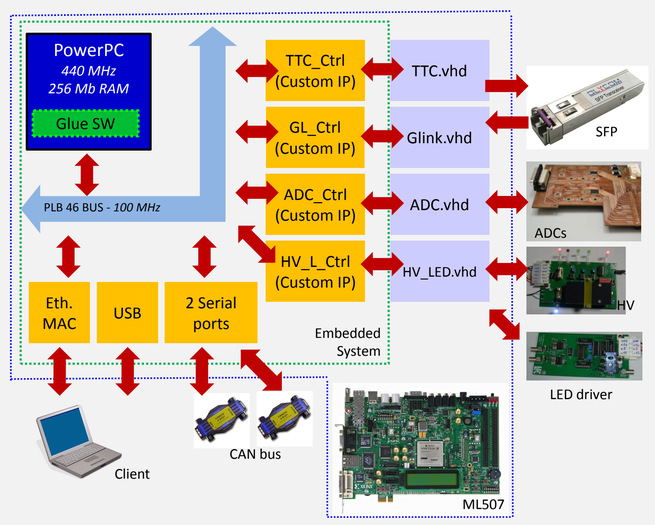
HV and LED driver

CANbus

Two commercial adapters and a custom cable convert the RS232 output ports of the motherboard to the CANbus interface of the super-drawers.

Serial-CAN adapter

CANbus connection



The embedded system

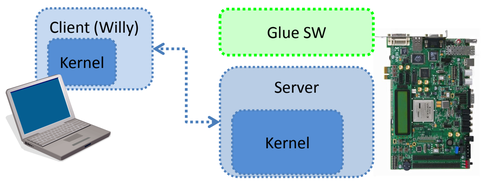
An embedded Linux with Kernel 2.6.39 has been chosen as OS for the PowerPC, mainly because of the big support to the microprocessor and the availability of drivers for Xilinx IP cores. An automatic boot of the whole system (bitstream + kernel + root file system) is performed from the CompactFlash using the System ACE Controller. The ELDK 4.2 cross compiler tools are used for building the Linux OS image and develop the applications.

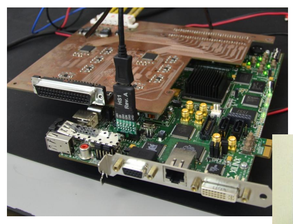
The processor is connected to its peripherals using a PLB 4.6. These peripherals are modeled as IP cores, some of which are commercial and provided by Xilinx and the rest being HDL-written custom IPs, developed to satisfy the test-bench specific needs.

The different custom boards of the test bench are interfaced to the embedded system by means of HDL firmware modules in the FPGA in one side, and required libraries for the applications that run on the server on the other side.

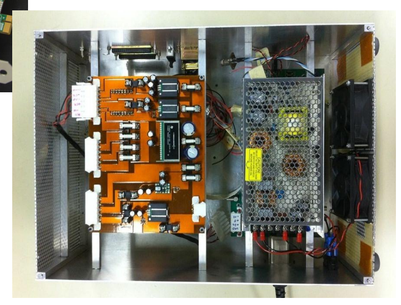
Software

The software follows the previous test bench versions client-server architecture. Now the server runs on the FPGA embedded processor instead of the VME processor. Besides, glue software substitutes the VME libraries.





Lab setup: ADC trigger board plugged into the Motherboad



Mechanics and assembly: first prototype of MobiDICK4. Boards installed on the aluminum box.