



Instrumentation of the Upgraded ATLAS Tracker with a Double Buffer Front-End Architecture for Track Triggering

David Wardrope,
on behalf of the ATLAS Collaboration

3rd May 2012

Workshop on Intelligent Trackers, Pisa



The Experimental Challenge

LHC upgrades foreseen for 2022 will increase the instantaneous luminosity to $\sim 5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$

Enables searches for extremely rare processes and high precision studies

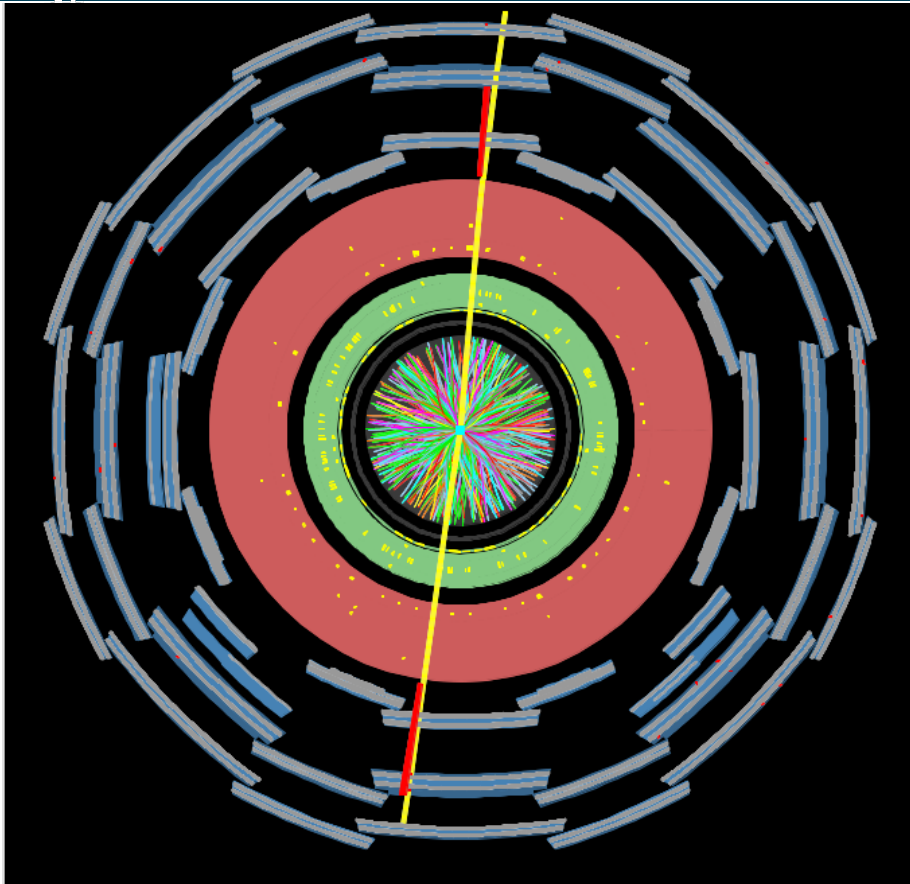
e.g. $H \rightarrow \mu \mu$, WW scattering, Higgs couplings, SUSY

Potential physics programme requires that ATLAS can trigger efficiently on single leptons with $p_T \sim 25 \text{ GeV}$

Challenging, since higher luminosity means

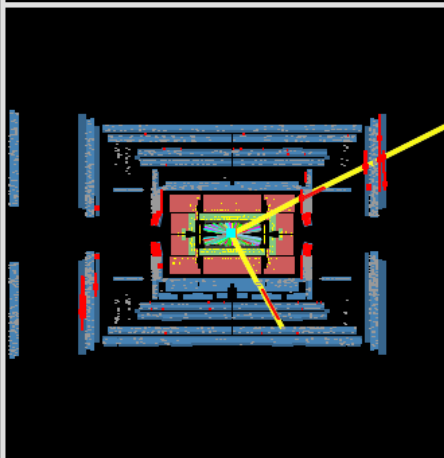
Higher rates

More difficult environment – ~ 150 collisions per bunch crossing!



Run Number: 201289, Event Number: 24151616

Date: 2012-04-15 16:52:58 CEST

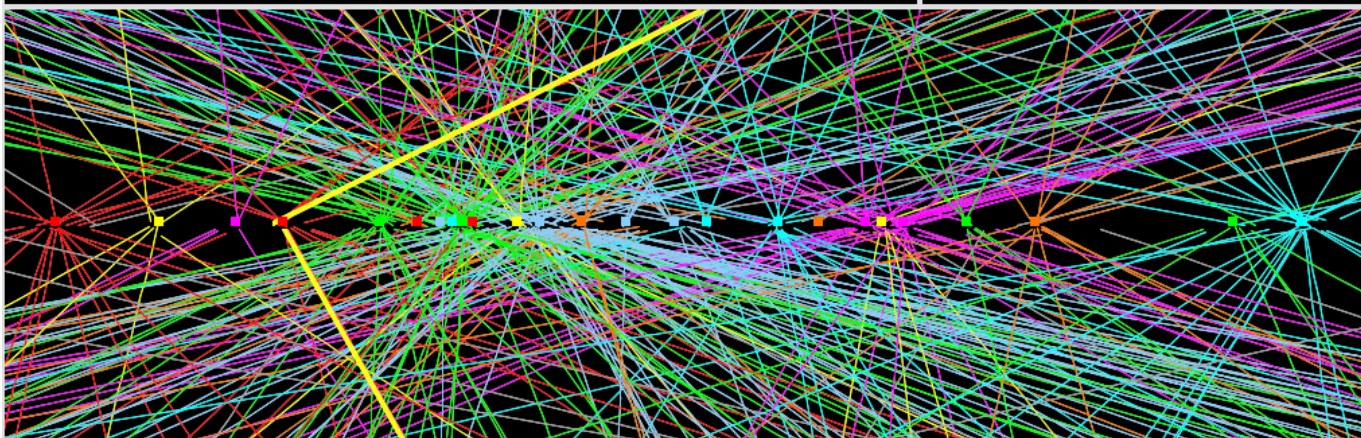


2012 collision
 $Z/\gamma^* \rightarrow \mu\mu$
candidate
event

25 interaction
vertices
reconstructed

>6× more
expected
after upgrade

Can trigger
rates be
controlled in
such an
environment?





Current ATLAS Trigger System

3 level system

Hardware-based Level 1 (L1)
Software-based Level 2 and
Event Filter

Level-1 identifies objects
passing programmable p_T
thresholds

EM clusters, muons, taus etc.

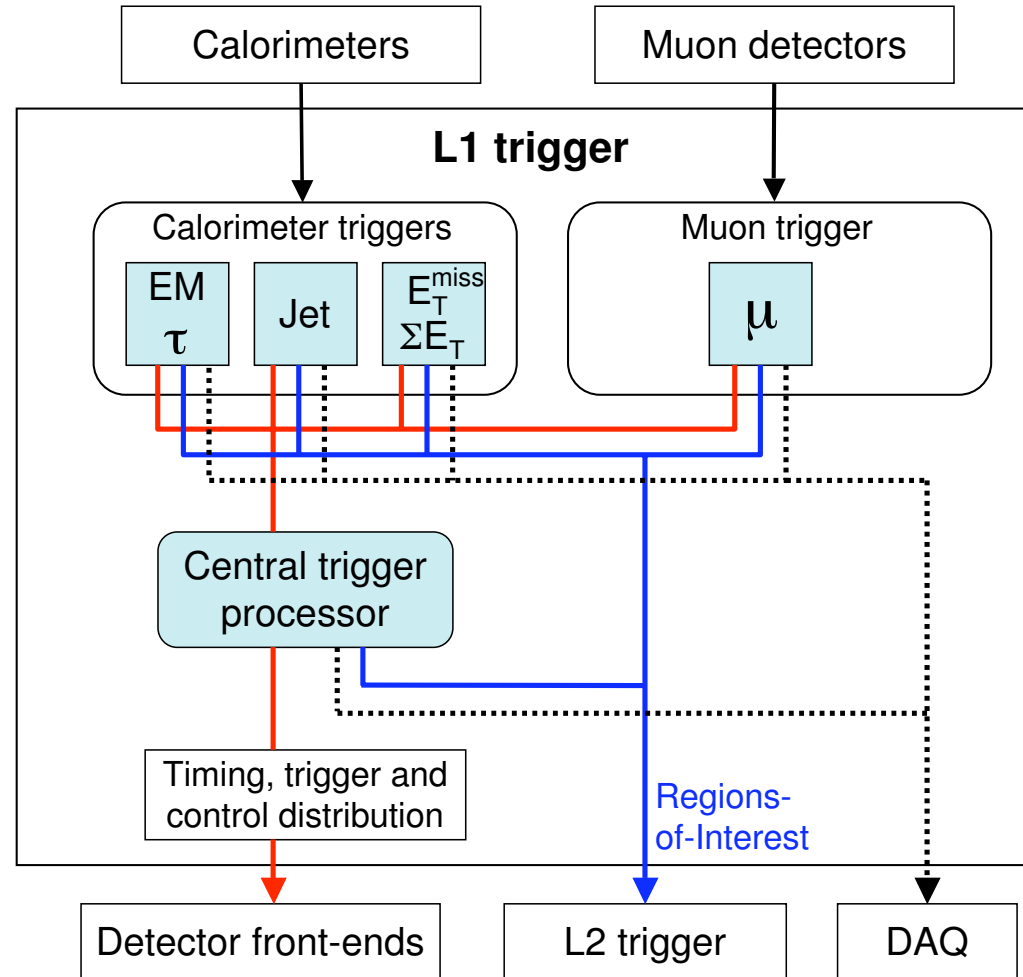
Decision to accept event
based on multiplicity of
these objects

Latency $< 2.5 \mu s$

Limit imposed by on-detector
pipeline memories

Tracking information cannot
be used at Level-1

L1 Accept (L1A) rate $\lesssim 75 \text{ kHz}$





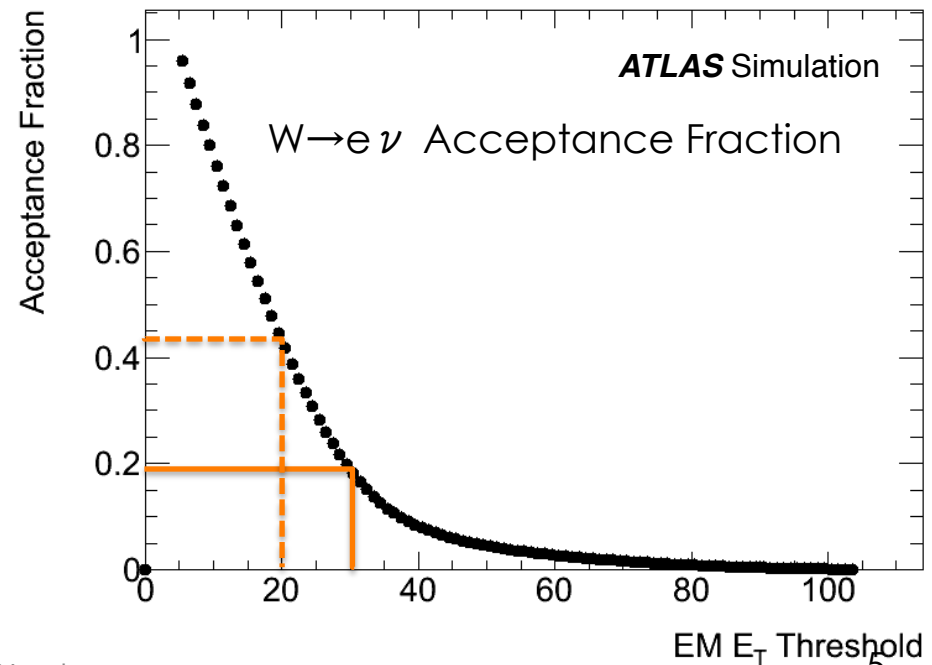
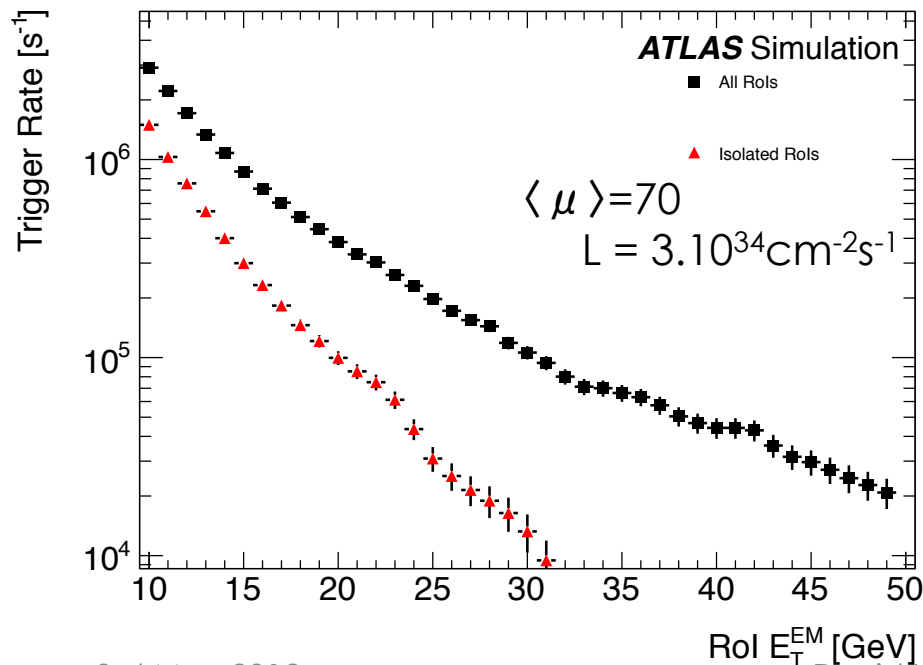
Current ATLAS L1 Trigger at High Luminosity

L1 trigger is operating well during current data-taking but cannot meet challenge posed by HL-LHC

e.g. single electron trigger rate with $E_T > 18$ GeV

At $\sqrt{s} = 7$ TeV and $L = 1 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, Rate = 20 kHz

At $\sqrt{s} = 14$ TeV and $L = 7 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, Rate = 380 kHz





Proposed ATLAS Upgrades

2018 – Phase I upgrades

New Muon Spectrometer small wheels (Endcaps)

Improved trigger p_T resolution and reduced fake rate

Higher granularity Level-1 calorimetry

Level-1 Topological Trigger processing

Selections based on topological variables, resolve object overlaps

2022 – Phase II upgrades

Inner detector replacement

TDAQ system upgrade

Upgrade of most FE electronics

Some muon spectrometer Monitored Drift Tube chambers are inaccessible

Use of full calorimeter granularity and resolution at Level-1

Use of muon precision tracking chambers at Level-1

Level-1 track trigger

Inaccessible muon FE electronics limits

L1 latency $\lesssim 20 \mu\text{s}$ and L1A rate $\lesssim 200 \text{ kHz}$

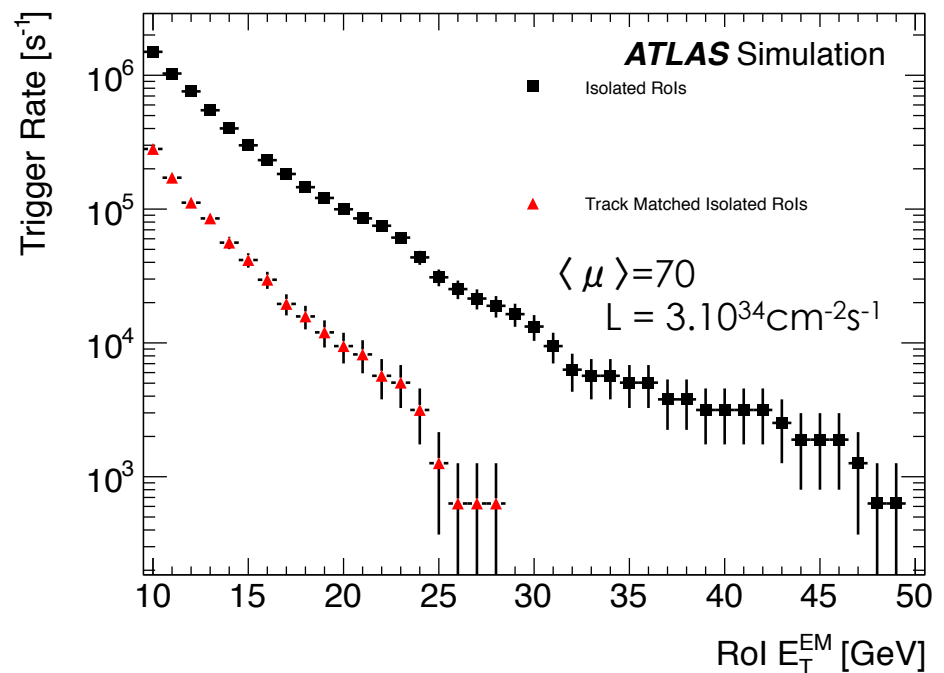
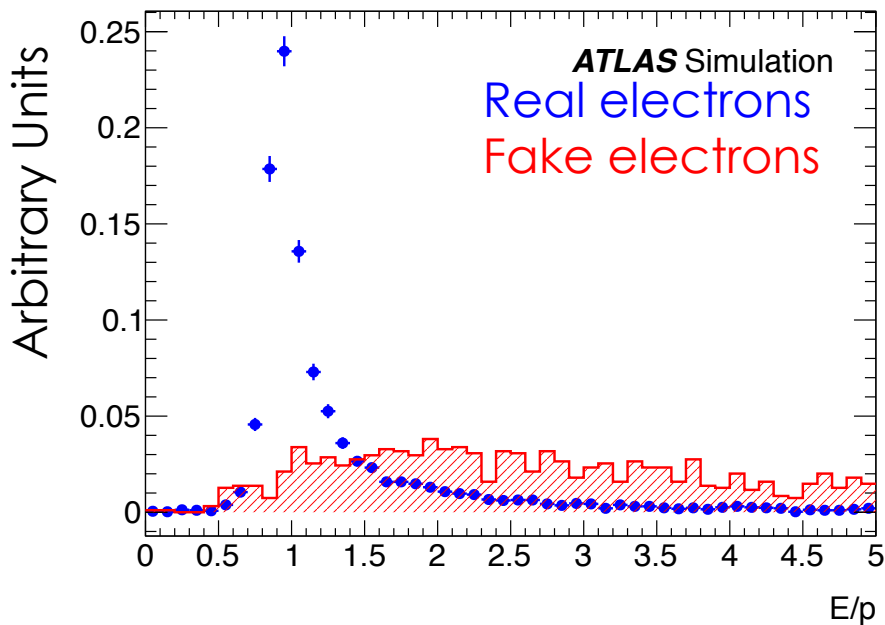
Incorporation of Tracking Information

Tracking information can greatly reduce trigger rates by

- Rejecting fakes

- Improving p_T resolution

- Ensuring objects come from common vertex



Single electron rates could be reduced by factor 10



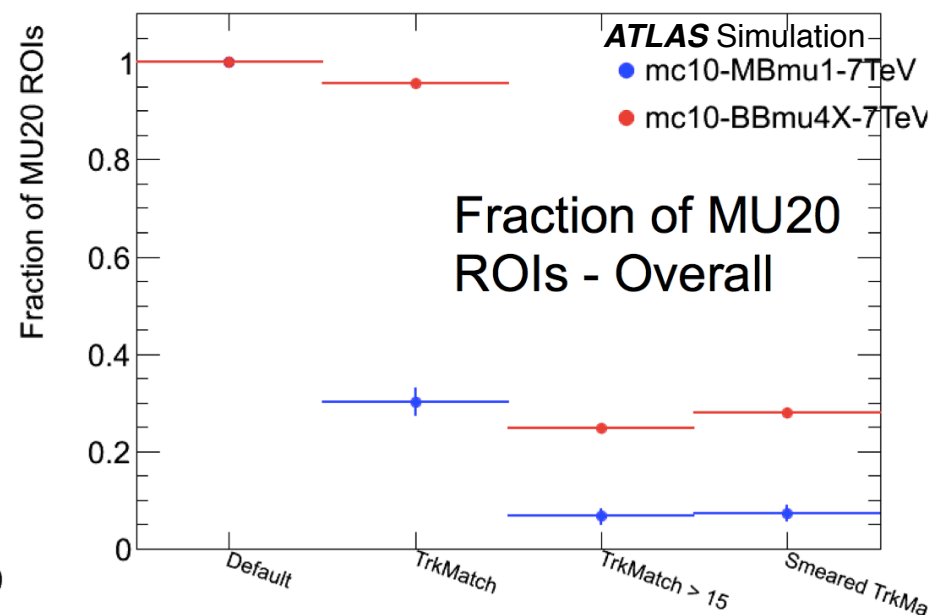
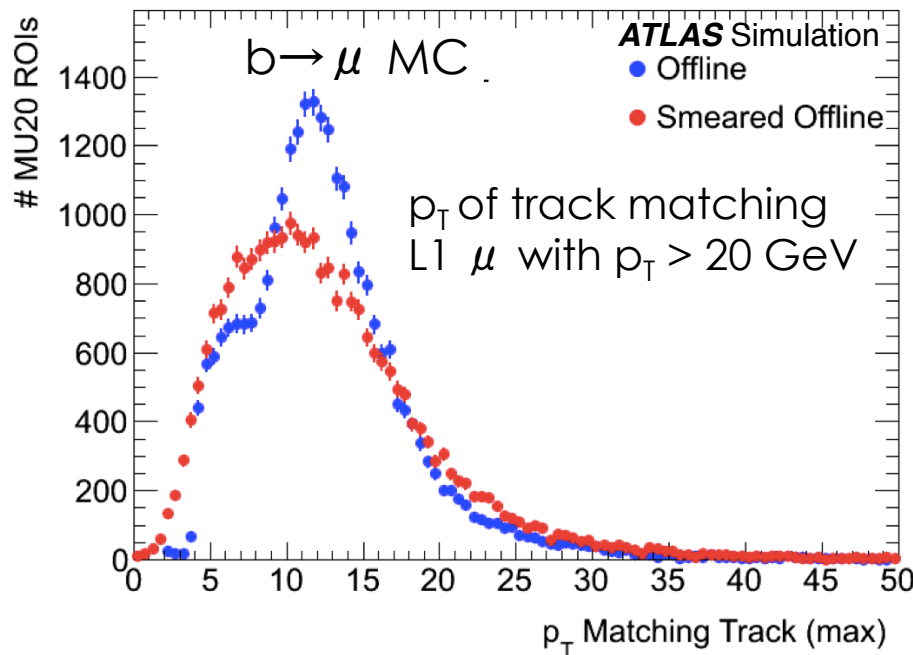
Incorporation of Tracking Information

Tracking information can greatly reduce trigger rates by

Rejecting fakes

Improving p_T resolution

Ensuring objects come from common vertex



Single muon rates could be reduced by factor 3-10



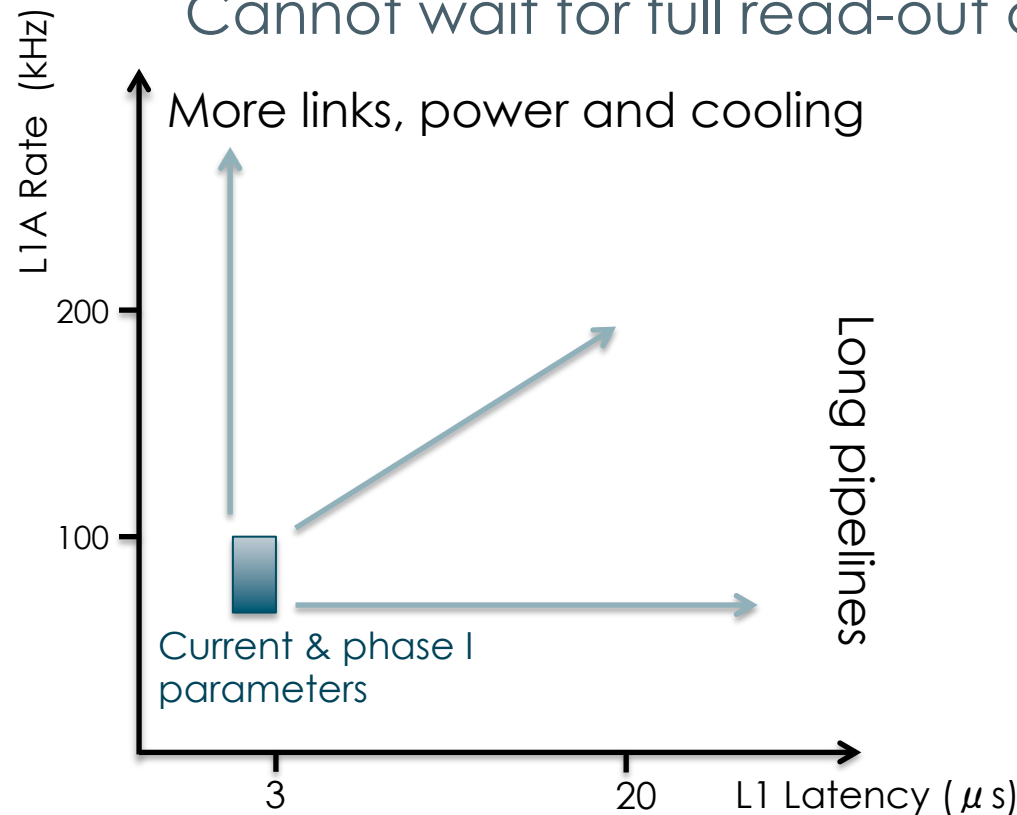
Difficulties of a Track Trigger

Cannot read out entire inner detector at 40 MHz

Need to reduce bandwidth requirements

Longer latencies pose problems

Cannot wait for full read-out of other detectors



A two stage scheme,
“Level-0 + Level-1”
offers a solution

Self-seeded tracking is
another option

See

[Saturday's presentation
by Andre Schoening](#)



Track Trigger Using a Two Buffer Scheme

The “L0+L1” scheme

Level-0:

Coarse calo and muon data

Rate 40 MHz \rightarrow 500 kHz

Latency $< 6.4 \mu s$

Defines Regions of Interest (Rols) for L1

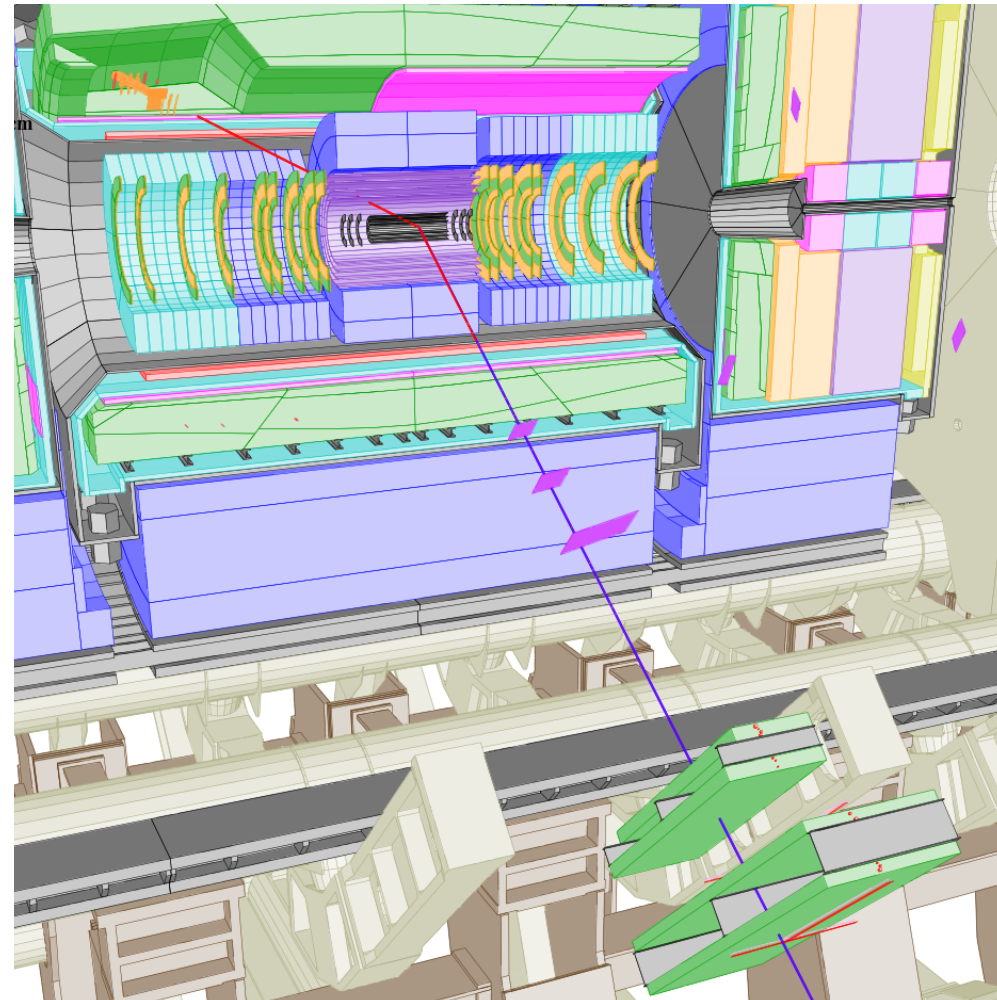
Level-1:

Tracker data only from Rols

Refined information from calorimeters and muons

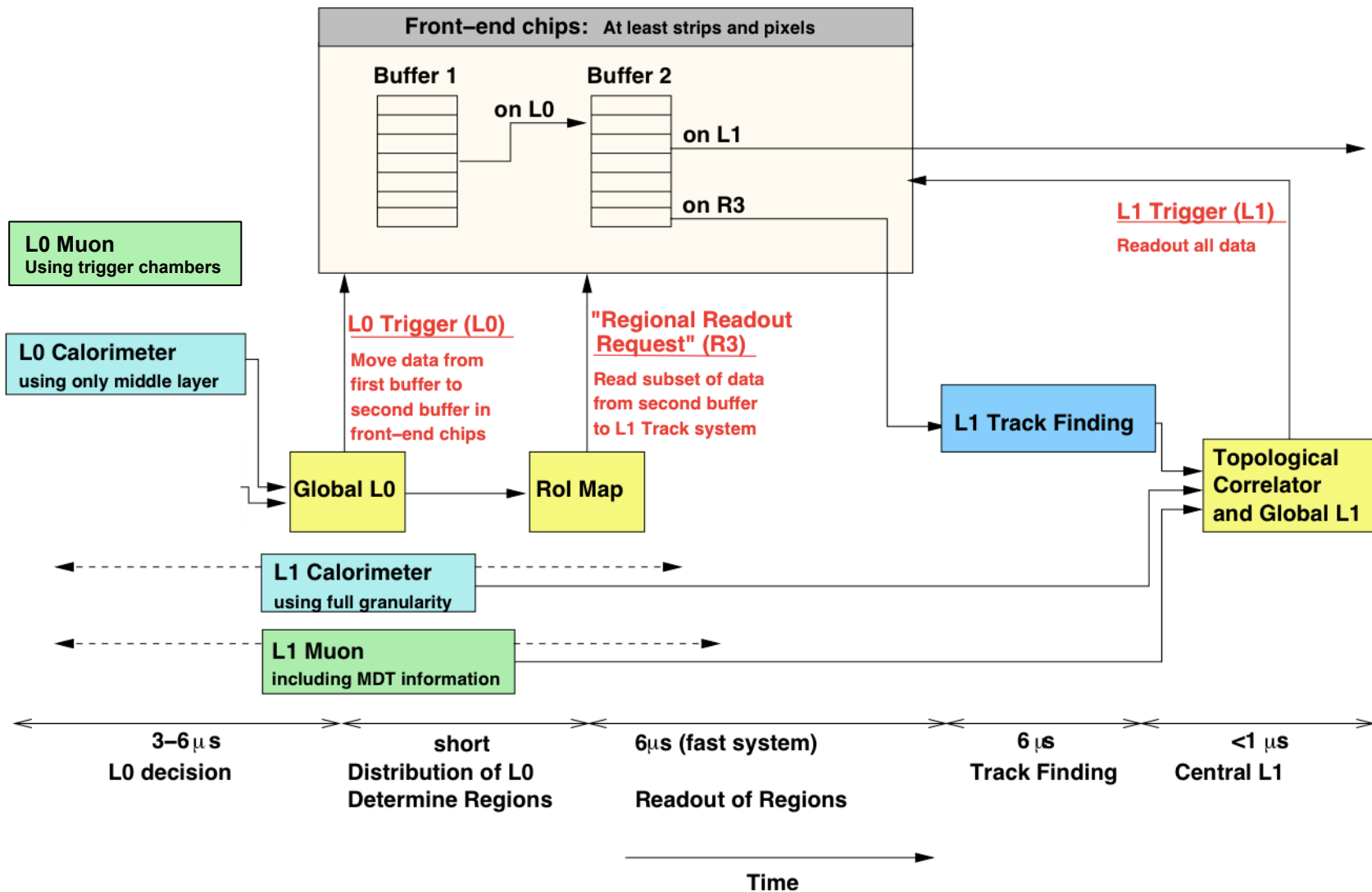
Rate 500 kHz \rightarrow 200 kHz

Latency $< 20 \mu s$

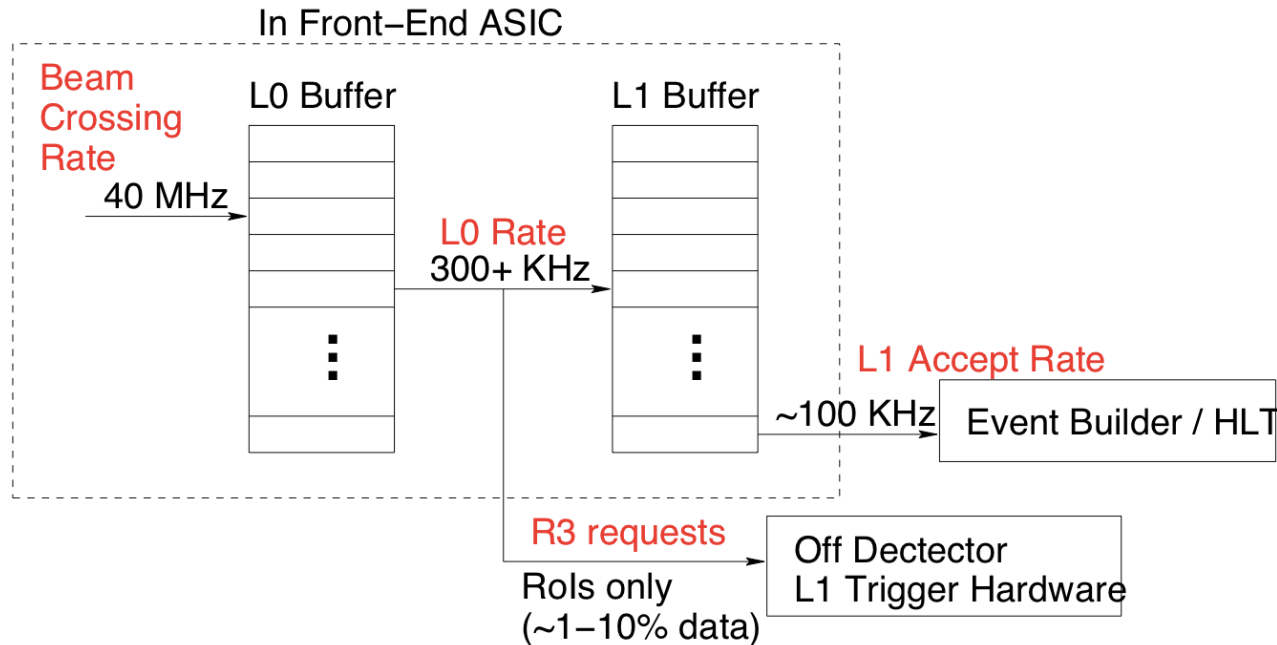




Possible Implementation of Two Buffer Scheme



Front-End – Latencies and Bandwidths



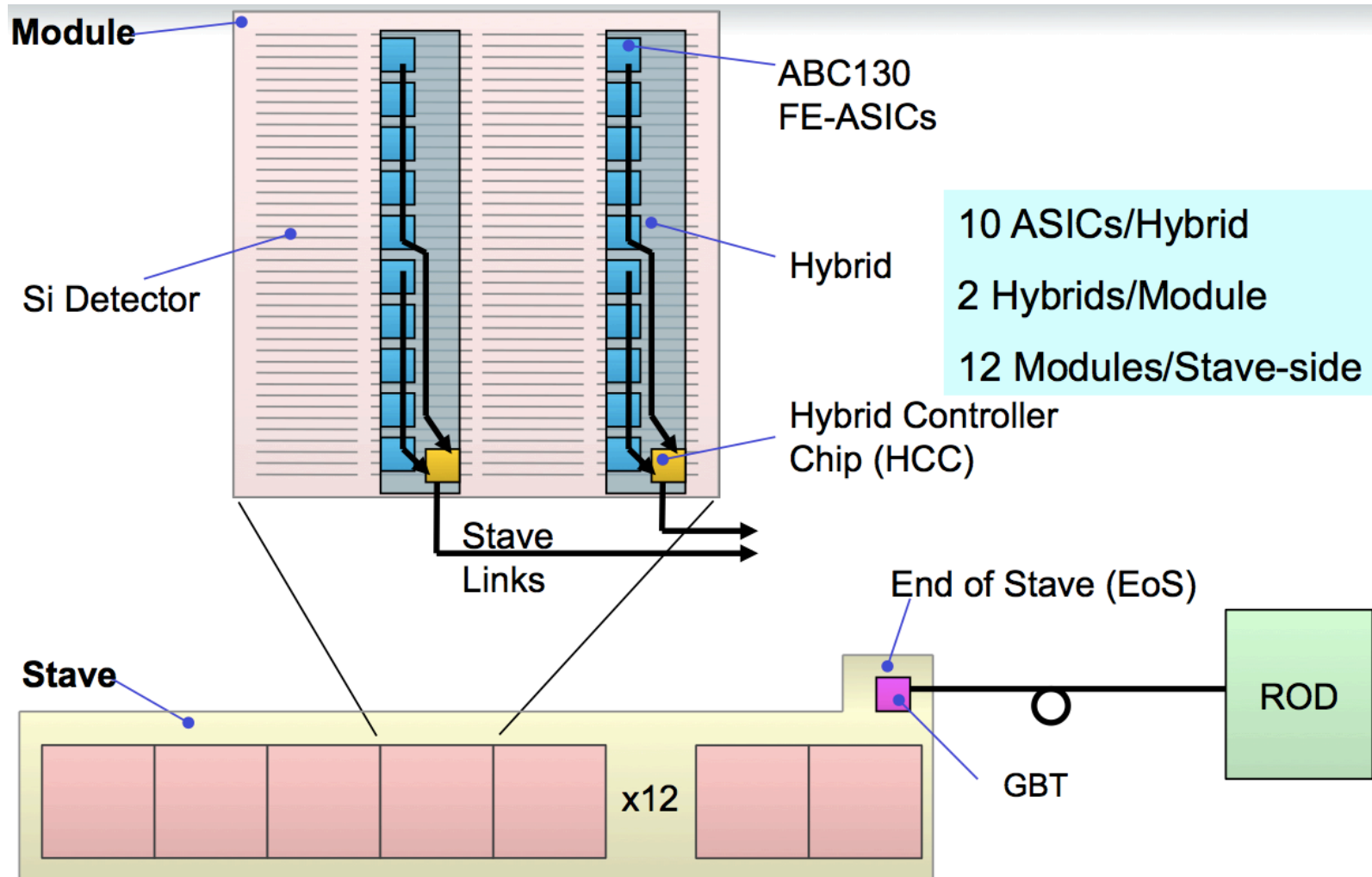
Bandwidth = (L1A rate + Rol data fraction × L0A rate) × event size
 e.g. L1A = 100 kHz, L0A = 500 kHz, 10% Rol frac. ⇒ 150 kHz × ev. size
 Bandwidth requirement is not great

L0 Buffer Length = $6.4 \mu s \times 40 \text{ MHz} = 256$ events long

L1 Buffer Length = $20 \mu s \times 500 \text{ kHz} = 10$ events long

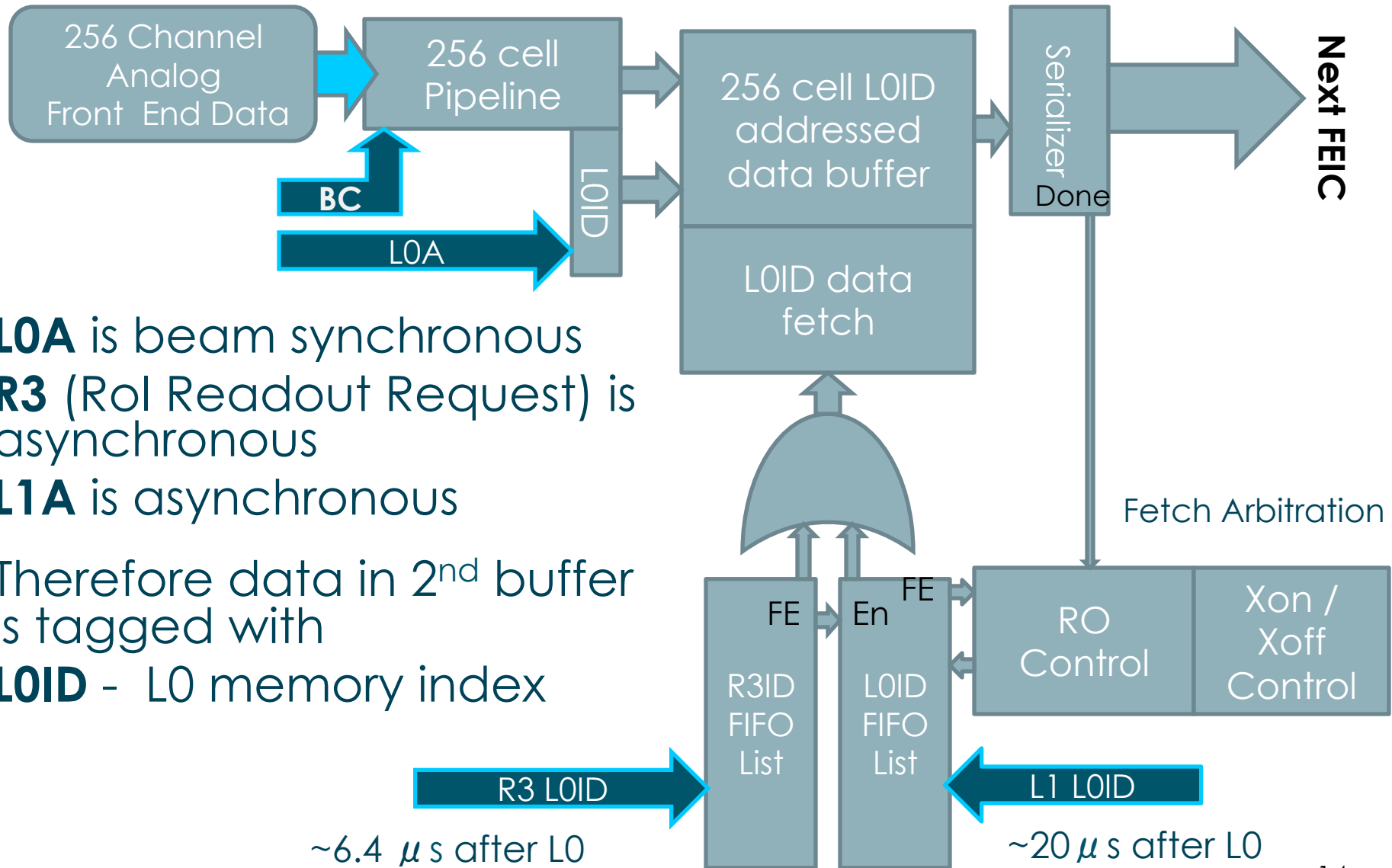
Two buffer scheme greatly reduces buffer length needed

Proposed ATLAS Strip Tracker Architecture





Front End ASIC Readout Architecture



LOA is beam synchronous
R3 (RoI Readout Request) is asynchronous

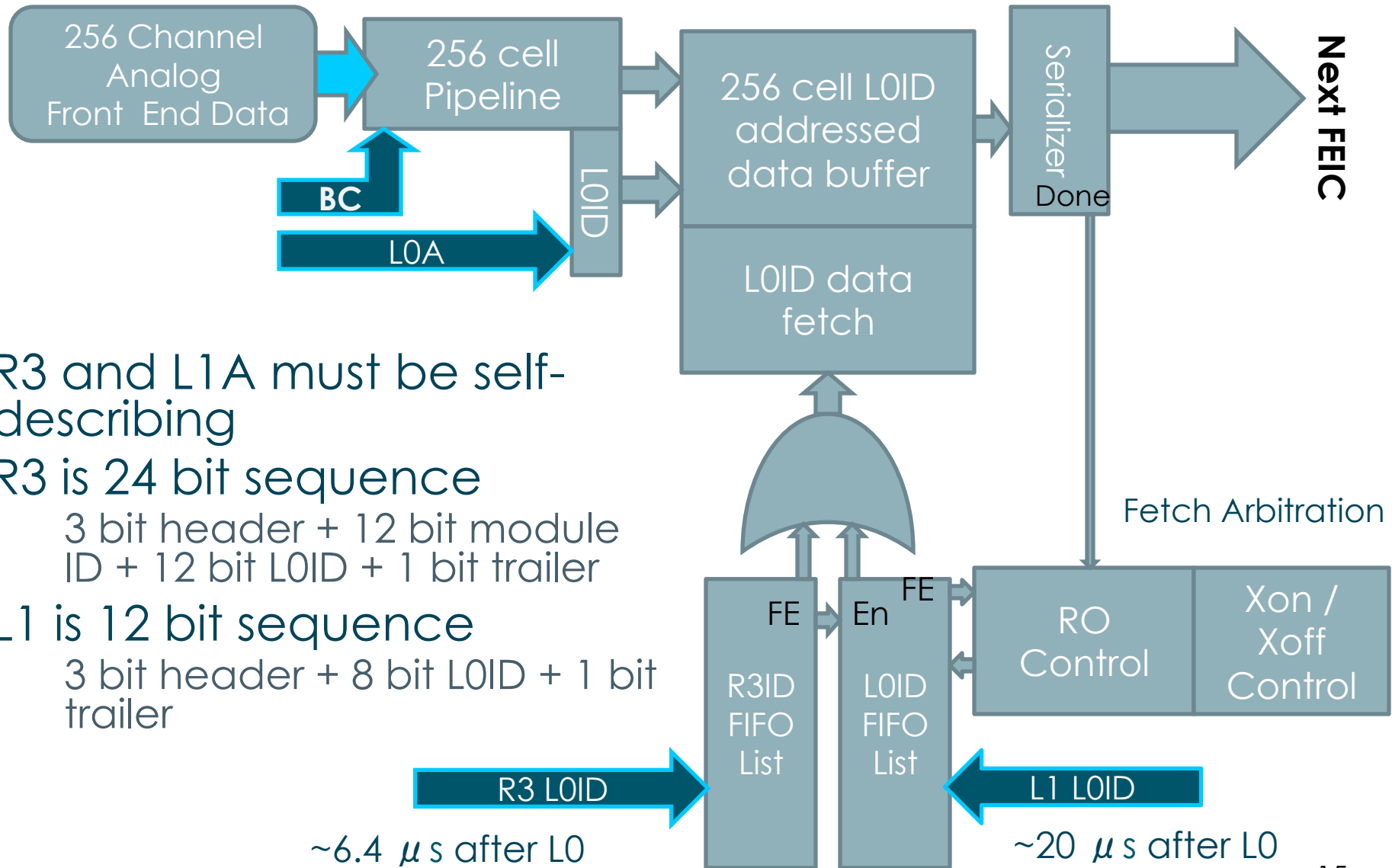
L1A is asynchronous

Therefore data in 2nd buffer is tagged with

L0ID - L0 memory index



Front End ASIC Readout Architecture



R3 and L1A must be self-describing

R3 is 24 bit sequence

3 bit header + 12 bit module ID + 12 bit L0ID + 1 bit trailer

L1 is 12 bit sequence

3 bit header + 8 bit L0ID + 1 bit trailer

Data Flow

Each hybrid is connected to a ROD on a (virtual) private link

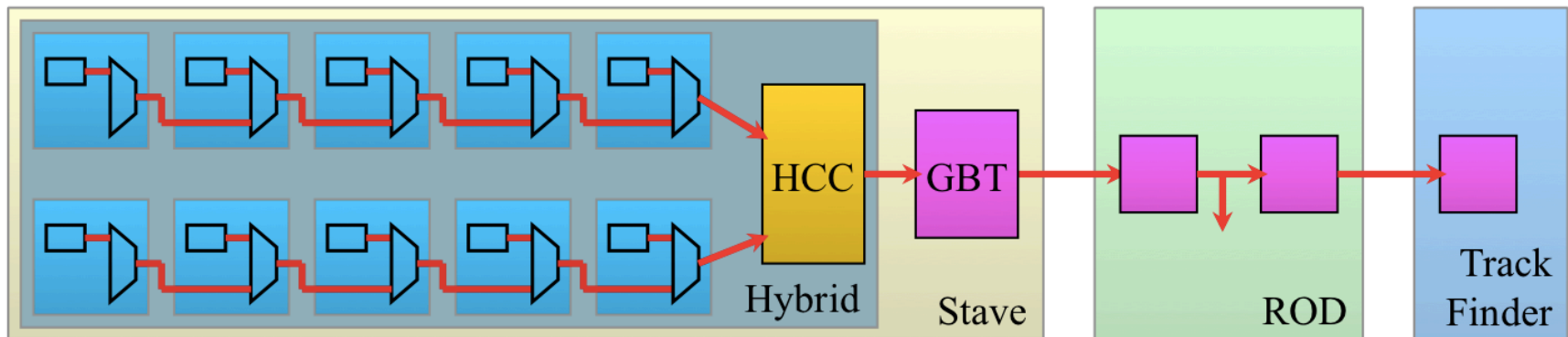
Bandwidth allocated per link

Bandwidth is the same along the whole chain

Each FE-ASIC generates packets and passes them to its neighbour, in 2 groups of 5

FE-ASICS decide to pass their own packet or their neighbour's based on priority level set by their position in the chain

R3 packets must wait for earlier packets to clear



Is it possible to read out the regions within $6 \mu s$?



Results from Discrete Event Simulation

Parameters

LHC bunch pattern (long/short gaps)

200 overlaid PU events

L0 rate = 300 kHz, L1 rate = 75 kHz, R3 rate = 3 kHz

Data packet size = 60 bits

Examine various configurations

80 Mb/s links, 160 Mb/s links

160 Mb/s is consistent with tracker baseline design

Separate links (real or virtual) for R3 and L1 data

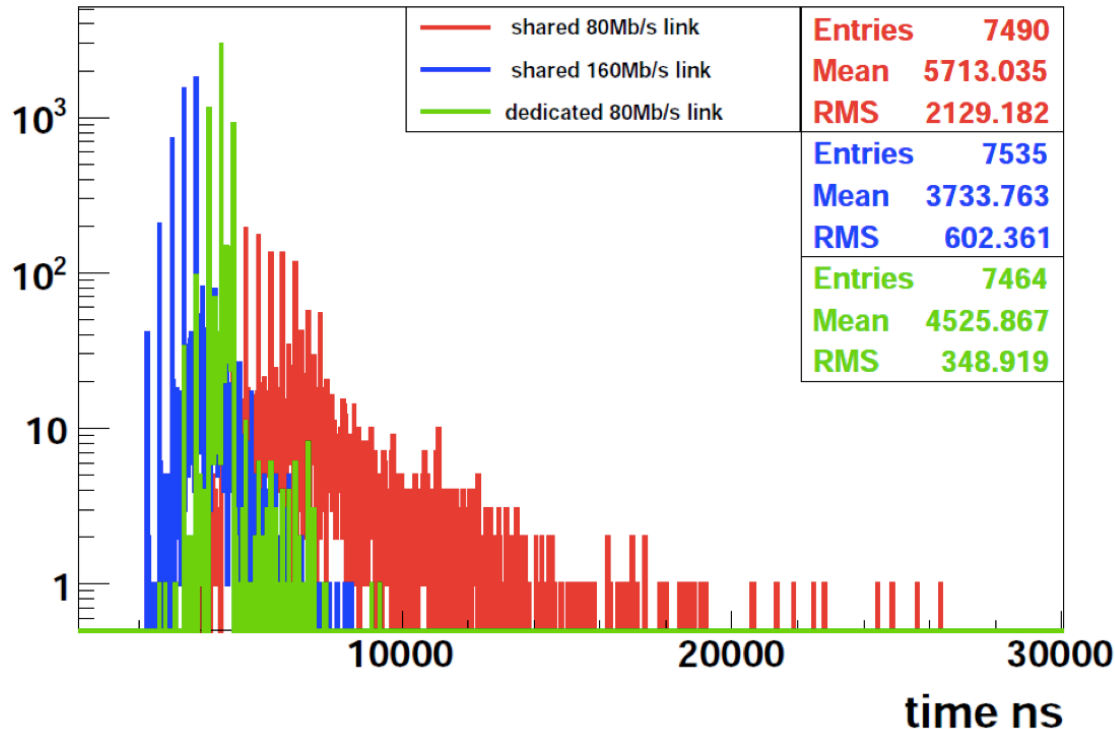
Allows R3-optimised data packet (33% smaller)

Separate R3 and L1 buffers on HCC

R3 data can queue-jump L1-data

Dedicated vs Shared Links

R3 data ABC to stave xfer



On average, 160Mb/s common R3-L1 link is faster than dedicated 80 + 80 Mb/s links

98.5% of R3 data is received in $< 5.5 \mu s$

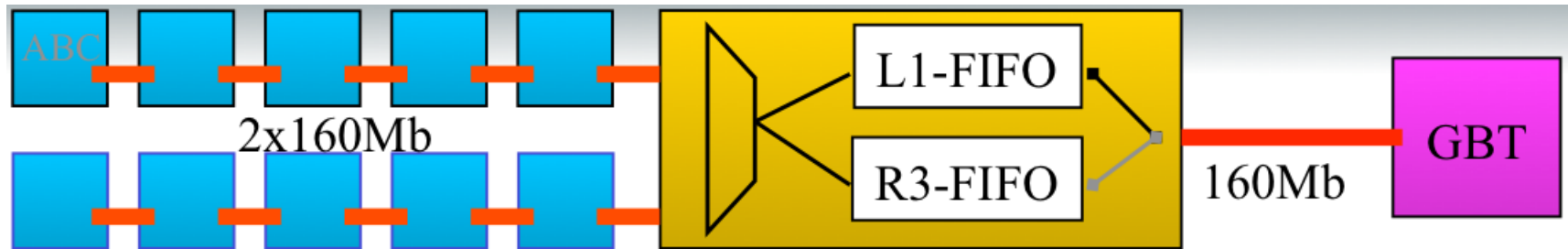
Optimal Configuration

2 × 160 Mb/s links feed the HCC

With a single 160 Mb/s Stave GBT output link

HCC FIFOs fill faster than they drain

Use a dedicated R3 buffer so R3 data can be prioritised



Increased output bandwidth is beneficial, but not necessary:

| Chip | Bandwidth Mb/s Stave | % of R3 data received in | | | |
|----------------------|-------------------------|--------------------------|---------------|---------------|---------------|
| | | < 4.0 μ s | < 4.5 μ s | < 5.0 μ s | < 5.5 μ s |
| Shared 160 × 2 = 320 | Shared 160 | 71.7 | 92.7 | 96.6 | 98.5 |
| Shared 160 × 2 = 320 | Shared 240 | 94.6 | 97.4 | 98.8 | 99.5 |



Optimal Configuration vs Different Rates

| Rates (kHz) | | | % of R3 data received in | | | |
|-------------|-----|----|--------------------------|---------------|---------------|---------------|
| L0A | L1A | R3 | < 5.0 μs | < 5.5 μs | < 6.0 μs | < 6.5 μs |
| 300 | 75 | 3 | 95.4 | 97.9 | 99 | 99.5 |
| 300 | 75 | 15 | 92.9 | 96.4 | 98.2 | 99.2 |
| 300 | 75 | 30 | 89.6 | 93.7 | 96.5 | 98.1 |
| 500 | 100 | 5 | 93.6 | 97 | 98.5 | 99.2 |
| 500 | 100 | 25 | 88.8 | 93.3 | 96.3 | 97.9 |
| 500 | 100 | 50 | 82.6 | 88.3 | 92.8 | 95.5 |

It is possible to get most R3 data out within 6 μs for a wide range of scenarios

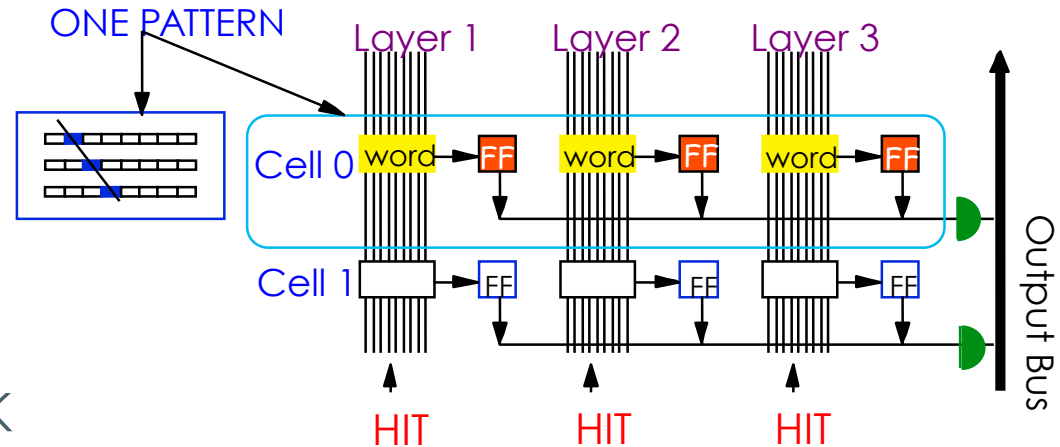
Track Finding

Pattern recognition performed using associative memory

Tests many patterns (e.g. 10^9) in parallel

Extremely fast

Used in CDF SVT, ATLAS FTK

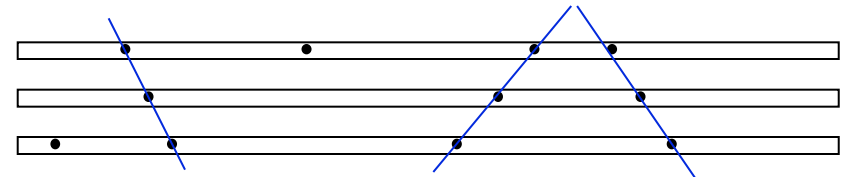


Hardware track fitting carried out in roads

Fast linear approx. algorithm gives near ideal precision

In principle, tracks can be found for all momenta

Limited by number of patterns stored





Plans

Hardware

ABC130 is being designed in 2012

Submission of ABC130 and HCC planned for Spring 2013 in an engineering run

First chips expected in autumn 2013

3D AM chip for track pattern recognition in R&D

[See presentation by Tiehui Ted Liu on Saturday](#)

More generally

Physics studies will determine requirements on track measurement quality, efficiency and fake rates

ATLAS Phase II Upgrade Letter of Intent will be submitted to the LHCC in 2013



Conclusions

Two-Buffer “Level-0 + Level-1” track trigger allows for use of track information at Level-1

- Reduces data output bandwidth from tracker
 - Less power, less cooling, fewer output links

- Reduces buffer size needed

Two-buffer scheme does not compromise offline tracker performance

- No change of layout, little (if any) extra material

Use of track information at Level-1 should enable the ATLAS trigger system to meet the challenges of $L = 5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$

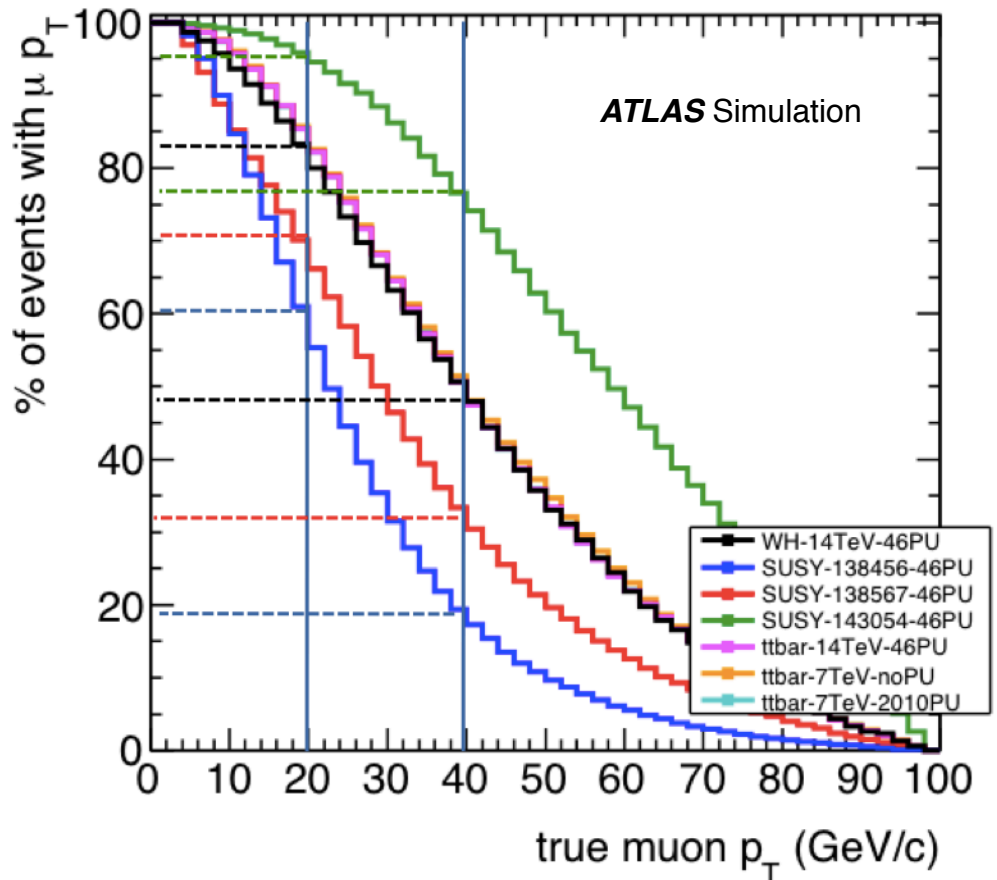


ADDITIONAL SLIDES

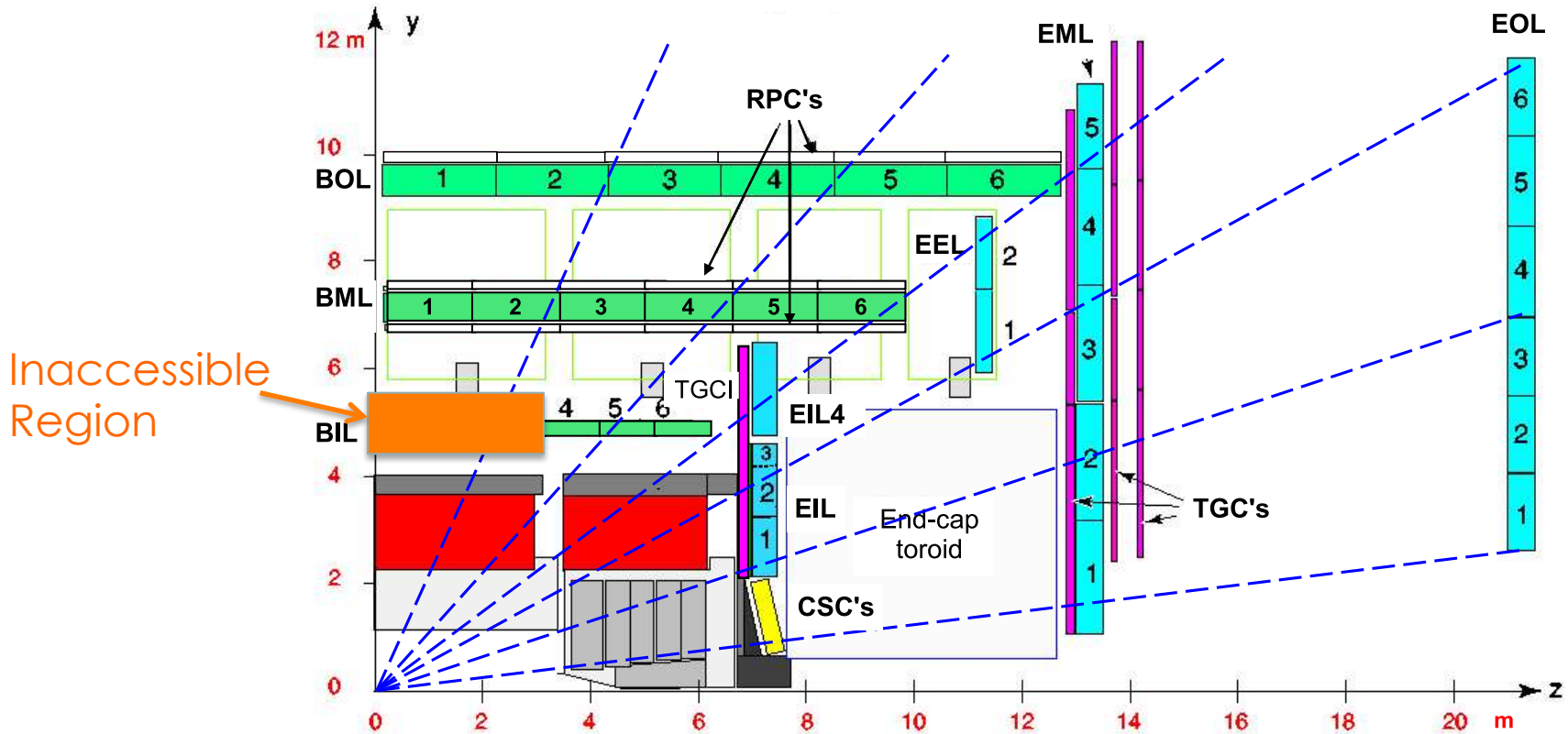
Impact of Raising Thresholds on Physics

hep-ph/0204087: “Physics potential and experimental challenges of the LHC luminosity upgrade”

Most channels include single lepton, $p_T > 20$ GeV



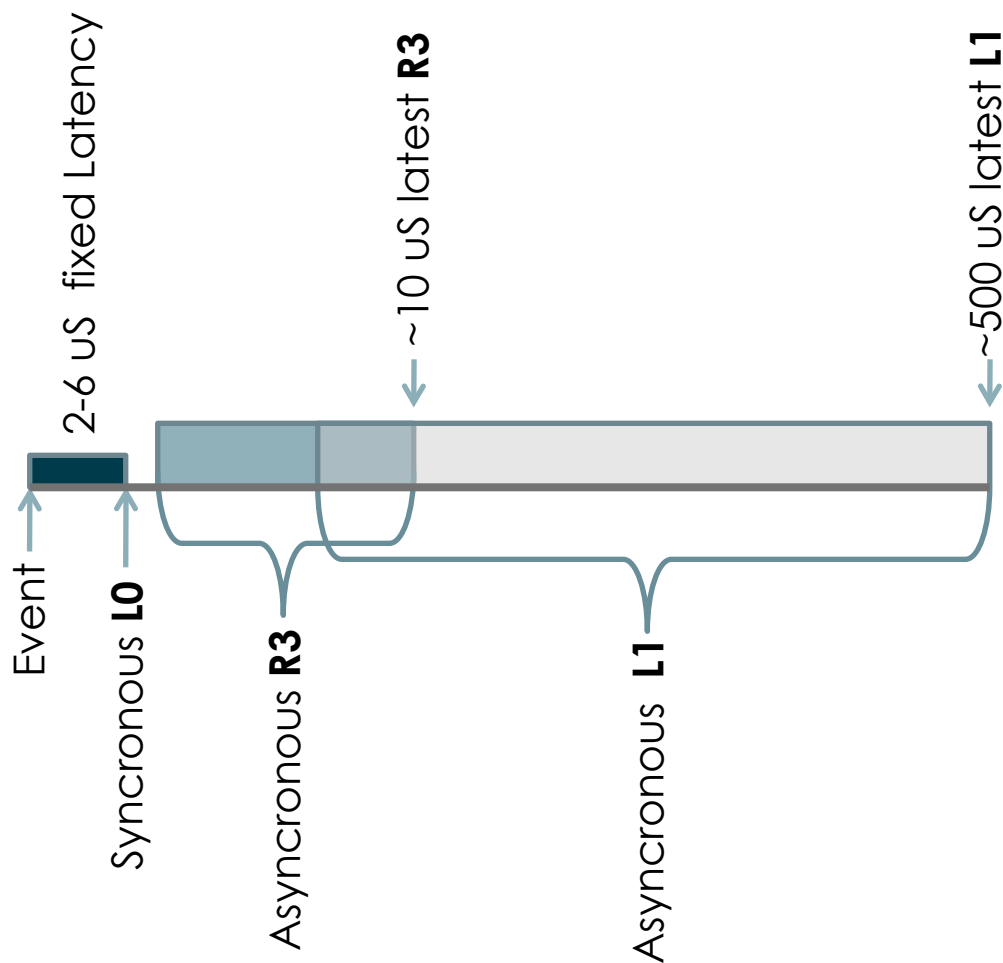
Inaccessible Muon Chambers



Changing FE electronics in region shown extremely difficult
Requires dismantling MDT chambers



Data Transfers





Associative Memory

