A Readout System for the LHCb Outer Tracker

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Abstract

The LHCb Outer Tracker is composed of 55 000 straw drift tubes. The requirements for the OT electronics are the precise (1 ns) drift time measurement at 6 % occupancy and 1 MHz readout. Charge signals from the straw detector are amplified, shaped and discriminated by ATLAS ASDBLR chips. Drift-times are determined and stored in the OTIS TDC and put out to a GOL serializer at L0 accept. Optical fibres carry the data 90 m to the TELL1 acquisition board. The full readout chain performed well in an e- test beam.

LHCb-PROC-2006-033
29/09/2006

I. Overview

55 000 straw drift tubes of 5 mm diameter mounted perpendicular to the bending plane behind the magnet form the Outer Tracker of LHCb [1]. A track resolution of 200 µm in the bending plane leads to a demand for a drift time resolution of better than 1 ns. The readout electronics is based on three ASIC chips, the ASDBLR [2][3][4][5][6] amplifier from ATLAS, the OTIS TDC [7][8] developed at the ASIC lab in Heidelberg and the GOL [9] (gigabit optical link) serializer from CERN EP. All on-detector electronics for one module end is housed in a shielded metal box.

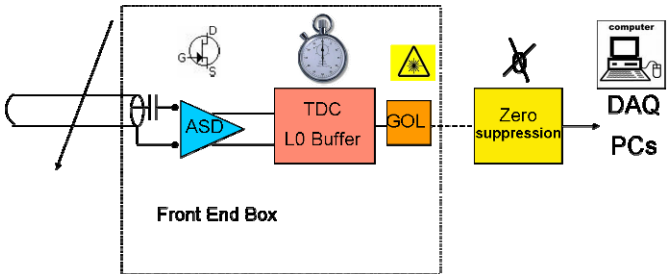

Figure 1: Block Diagram of OT Electronics

The charge signal from the straw anode wires is amplified, shaped and discriminated by an 8 channel ASDBLR chip with 12 ns shaping time. Four ASDBLRs on 2 PCBs are connected to one OTIS TDC. The relative time between the discriminated hit signal and the bunch clock is determined by the OTIS TDC with the help of a delay locked loop. The 64 inverters in the DLL lead to a time resolution of 25 ns/64 = 390 ps. Drift times are 6-bit encoded and written to a 240 bit wide L0-buffer. At L0-accept hits within a 75 ns window are readout and a header containing OTIS location, L0-id, Bunch-Id plus status is prepended. L0 accepted data from 4 TDCs runs to the GOL chip. The GOL serializes 32 input bits to a 1.6 Gbit/s output, driving a VCSEL diode. Optical fibers carry the data 90 m to the TELL1 [10][11] acquisition board. On the TELL1 daughter boards with 12 inputs each convert the optical serial data back to parallel electrical data. FPGAs on the TELL1 are programmed to synchronize, zero suppress and reformat the data. At 1 MHz events are transmitted through multiple Gigabit ports to a more than 1000 CPU computing farm.

The newly developed outer tracker electronics was used for data taking in an e- test beam. Reading out 512 channels the full chain proved excellent performance.

II. Amplifier

The ASDBLR Amplifier Shaper Discriminator with Base Line Restoration is an ASIC developed for the ATLAS TRT straw detector by Michael Newcomer (University of Pennsylvania). It is implemented in the DMILL bipolar process. Basic characteristics are the fast peaking time of 7 to 8 ns, radiation hardness withstanding 3 MRads of ionizing particles and 10^{14} Neutrons/cm^2, low cross talk of 0.2% and low noise of < 1fC equivalent charge.

After a pre selection discarding chips with malfunction such as broken channels the analogue performance is tested. In a threshold scan with fixed charge injection sensitivity-spread and noise of each channel is measured and the best 30% of the working ASDBLRs are chosen, see Figure 2:

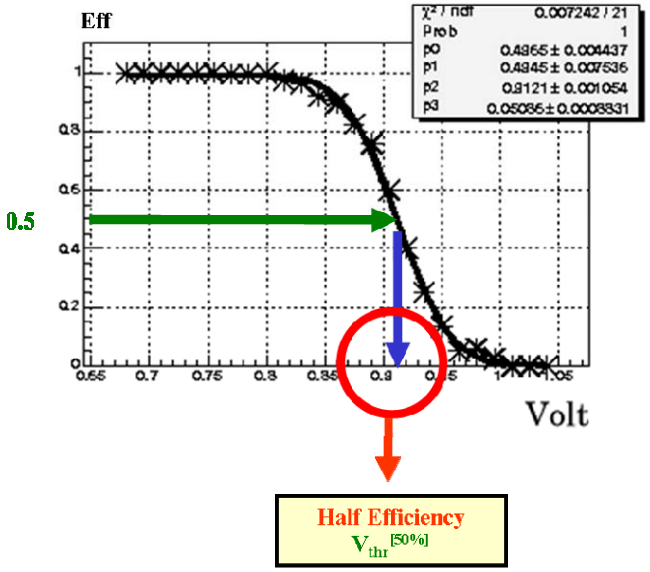

Figure 2: Amplifier Threshold Scan

The sensitivity is measured by the position of the 50% efficiency (vs. threshold) and the noise level can be deduced from the steepness of the step function.

Two ASDBLR chips share the same board, see Figure 3:

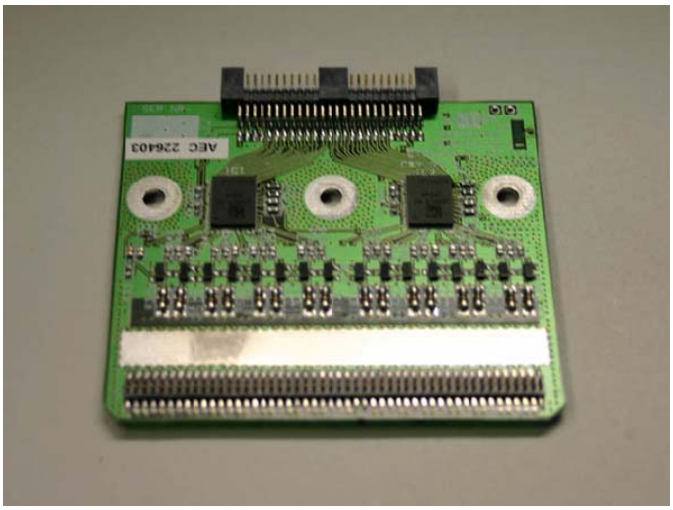

Figure 3: Amplifier Board

The board design was optimised for grounding and good heat dissipation. To achieve better grounding the 16 input signals are connected via a 100 pin connector, all non signal pins carrying ground. Non standard 100 µm copper planes inside the PCB and numerous cooling via allow operation of the chip at below 45 °C with standard water cooling of the electronic box.

III. Time to Digital Converter

The TDC called Outer Tracker Time Information System OTIS is a 0.25 µm CMOS ASIC.

It allows the drift time measurement of 32 detector channels with an accuracy of better than 1 ns.

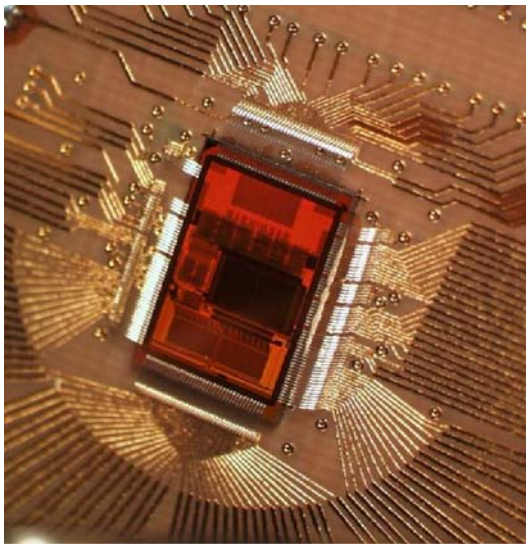

Figure 4: OTIS TDC

The bunch clock of ca. 40 MHz is running through a delay locked loop with 32 delay elements of two stages each, with a tab after each stage. Each tab delivers a time reference shifted in respect to the bunch clock. This leads to an intrinsic resolution of 25ns /64 = 390 ps. When one of the 32 differential inputs of the OTIS senses a hit signal, the state of all tabs is latched into the hit registers of this channel and the first 0 1 transition is encoded into 6 bit. Every 25 ns a bit signalling if a hit was sensed in this channel, the timing information, and the bunch counter are input to the L0 pipeline. The L0 pipeline is implemented as radiation hard dual port SRAM [12] of 164 rows and a width of 240 bit. At a positive trigger decision the relevant data is copied to the derandomizer buffer. The OTIS chip allows the readout of 3 consecutive bunches at one L0 accept such covering 75 ns. The data is reorganized into a header containing the number of the bunch crossing, the event number and error conditions followed by the drift time information. In the standard scheme 32 header bits are followed by 32 bytes of drift time information. In this scheme each byte carries the drift time of 1 channel. The data of one TDC is send through 8 differential CMOS outputs to the serializer chip (GOL).

Each OTIS is bonded to one PCB, interfacing to two ASDBLR amplifier boards and the GOL auxiliary board. The TDC has an I^2C [13] control bus interface and carries eight digital to analogue converters supplying the threshold voltages to the four connected ASDBLR and the settings for the initialization and monitoring of the delay locked loop.

The performance of the TDC has been studied both using random hit signals and signals with a well defined delay in respect to the bunch clock. The relation between input signal delay and measured drift time is shown in Figure 5:

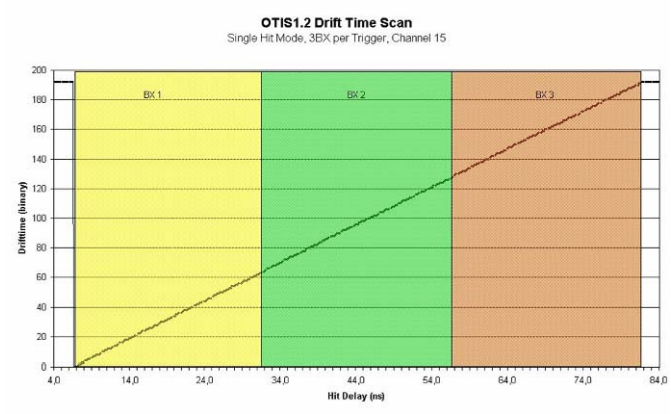

Figure 5: Delay [ns] vs Drift Time [bin]

IV. Gigabit Optical Link

The data accepted by the L0 trigger is output by the TDC in 36 bytes @ 40 MHz. Data from four TDC chips is serialized with the help of one Gigabit Optical Link (GOL) chip, resulting in incoming 32 bits parallel. The GOL is used in Gigabit Ethernet mode, encoding all bytes in 10 bit words that are chosen to balance the number of high and low bits at the serial output. The data is finally fully serialized and output to a Vertical-Cavity Surface-Emitting Laser (VCSEL) at 1.6 Gbit/s. The VCSEL diode is a type from ULM photonics (ULM850-05-TN-USMBOP). The bias current for the VCSEL can be set via the I^2C bus interface of the GOL chip, a good choice was 1.8 mA. The GOL output was moved as close as possible (<3 mm) to the VCSEL, the connection is impedance matched to 22 Ohm. The performance of the optical link is determined by a bit error rate test BERT. The GOL chip has a build in 16 bit counter that can be activated as data source via I^2C. Alternatively the optical signal was measured with the help of an optical probe [15][16]. Sampling a few thousand bit transitions into an eye diagram shows how good the high and the low value of the digital signal are separated, see top left in Figure 6:

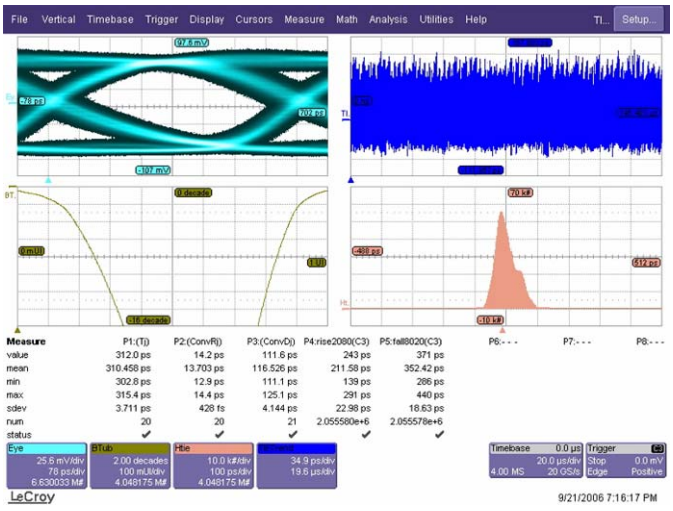

Figure 6: Eye Diagram of Serial Data

The GOL chip is mounted in a 100 pin BGA package on the GOL auxiliary board [17]. In order to guarantee the performance of the GOL chip a clock filter QPLL [18] and a four transistor power switch CRT4T have been added on the GOL auxiliary board. The QPLL filters the clock signal driven by the TTCrx [19] fast control receiver chip to below 50 ps peak to peak. The lock rage of the QPLL is 3.7 kHz around the reference frequency of 40.0786 MHz. Especially its connection to the controlled quartz must carefully respect pad and line capacities. The CRT4T switches the power at the GOL inputs fully off, so avoiding partial powering of the phase locked loop.

The GOL auxiliary board also distributes low voltage, fast control signals and I^2C slow control bus. The low voltage 2.5V, 3V and -3V regulated by three radiation hard power regulators from ST microelectronics, type 4913 [20] and 7913 [21][22]. The input voltage is +6V and -6V. The water cooling line of the front end electronic Box (FE-box) is directly under these power regulators. To reduce the risk of oscillation of especially the negative type 7913, extra 100 µF capacitors have been placed both at the ±6V inputs and at the -3 V output. The 2.5V serves as supply for the OTIS TDC, the GOL, the QPLL and the CRT4T while the +3V and -3V are used for the ASDBLR amplifiers. As a few LVDS receivers and the VCSEL diode need +3V too, their supply voltage is decoupled by series resistors (C-R-C-R-C low pass).

The fast control signals clock, trigger, test pulse and synchronous resets for bunch and event counters arrive as LVDS signals on the GOL auxiliary board and are distributed to the 4 OTIS boards using current dividing resistors.

I^2C is transmitted via LVDS lines from and to the control box on the detector frame and converted to a single ended signal on the GOL auxiliary card.

V. Front End Box

The front end electronics consisting of 4 HV boards, 8 ASDBLR board, 4 OTIS boards and 1 GOL auxiliary board is mounted in the FE-box see Figure 7:

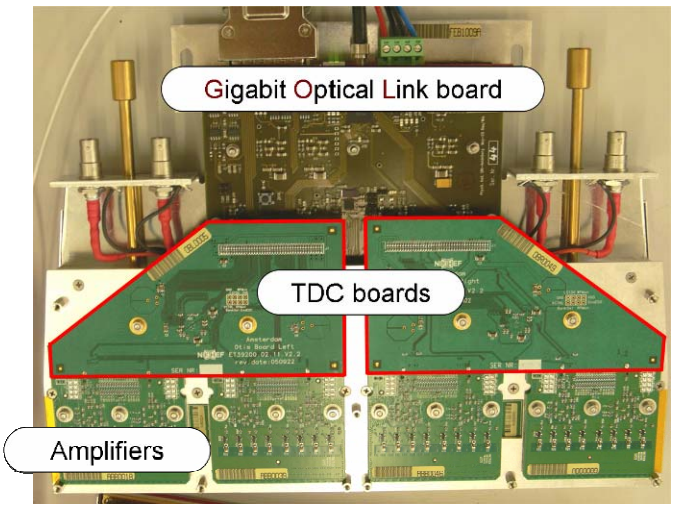

Figure 7: Front End Electronic Box

Each front end electronic box serves the 128 channels on one end of a straw detector module. It has 4 HV inputs, a 50 pin SCSI controls input, a 4 pin LV input, but only one optical

fibre data output. The FE-box is mechanical and electrical protection and conducts the heat to the water cooling.

VI. TELL1 BOARD

The data from the Outer Tracker on detector electronics is transmitted over 432 fibres to the counting house. There a LHCb wide established 9U DAQ board (TELL1) receives the data, does zero suppression and reformatting before sending it at the same rate of 1.1 MHz over four Gigabit Ethernet ports to the CPUs of the online filter farm. The TELL1 board is based on four FPGA chips on the input and one FPGA for the data output see Figure 8:

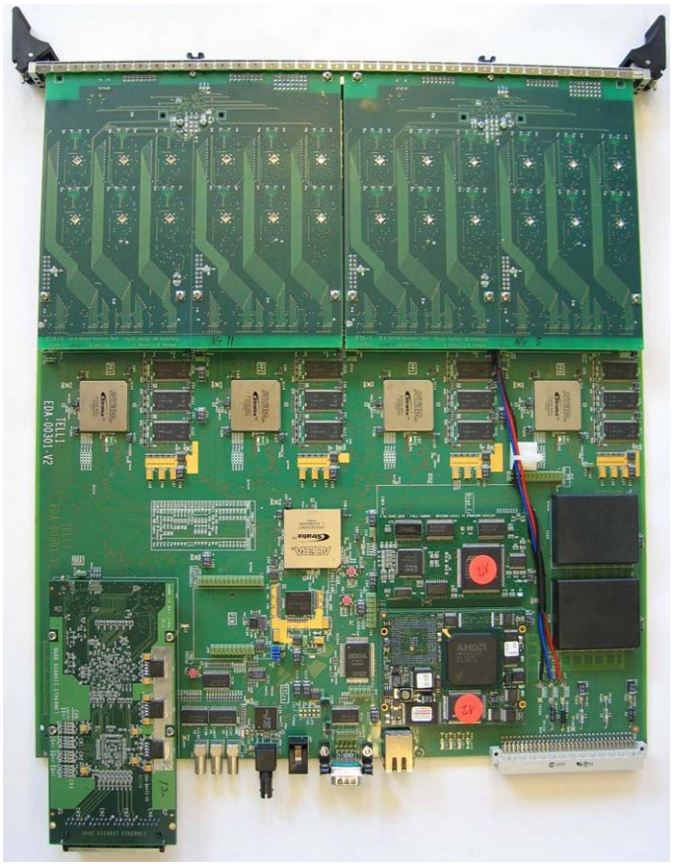

Figure 8: TELL1 DAQ Board (Lausanne)

As both analogue and digital data transmission from the detector to the counting house are implemented in LHCb two different input cards have been developed. The OT uses the optical receiver Card (O-RxCard). The O-RxCard [23] houses a 12 way optical receiver and 12 TI TLK2501 [24] deserializers. The O-RxCard has been developed in Heidelberg and produced in Beijing. As the OT has a high average occupancy only 9 out of 2x12 optical inputs will be used per TELL1 board.

VII. PERFORMANCE AT TEST BEAM

In the beginning of 2005 a test of the full OT electronics took place at DESY using a 5 GeV electron beam. 4 short detector modules from the series production have been mounted and read out. The electronics consisted of FE-boxes from the preproduction, the TTC [25] system, I^2C slow control and a FPGA based DAQ [26][27] using the O-RxCard and a commercial PCI acquisition board [28]. The trigger and time reference was coming from scintillators in the beam axis after the detector modules. After a few days of setup the electronics was running stable until the end two weeks later. The numerous data sets where used to validate the noise, x-talk and timing of the electronics as well as to study the tracking resolution of the overall detector [29].A histograms of the drift time can be seen in Figure 9:

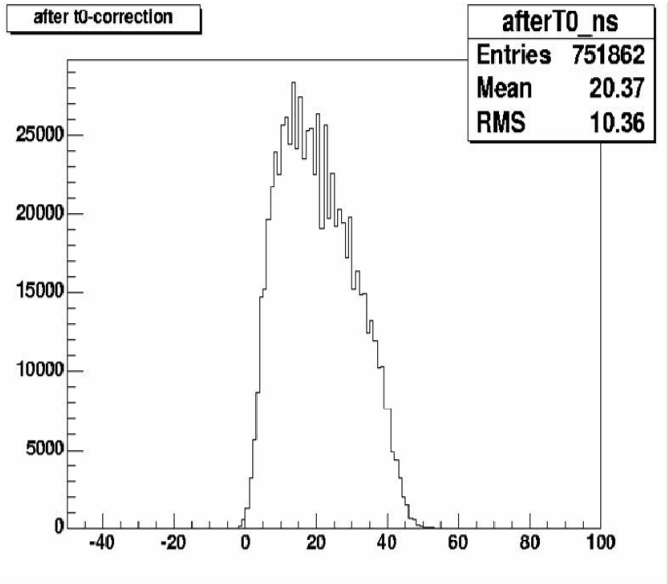

Figure 9: Drift Times t0 corrected

The efficiency was above 94%, the timing resolution better than 0.5 ns and the spatial resolution better than 175 ns.

VIII. SUMMARY AND OUTLOOK

The readout electronics of the LHCb Outer Tracker has been developed and successfully tested to achieve good resolution at a high efficiency and low noise. All ASIC chips have been produced and tested by now. The production and test of the boards is reaching the 20 % level at the moment and the installation and commissioning has started in the LHCb cavern.

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