A Fully Bidirectional Optical Network With Latency Monitoring Capability for the Distribution of Timing-Trigger and Control Signals in High-Energy Physics Experiments

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***Abstract*—The present paper discusses recent advances on a Passive Optical Network inspired Timing-Trigger and Control scheme for the future upgrade of the TTC system installed in the LHC experiments' and more specifically the currently known as TTCex to TTCrx link. The timing PON is implemented with commercially available FPGAs and 1-Gigabit Ethernet PON transceivers and provides a fixed latency gigabit downlink that can carry level-1 trigger accept decisions and commands as well as an upstream link for feedback from the front-end electronics.**

***Index Terms*—Field-programmable gate arrays and gigabit links, fixed and low latency serial links, passive optical networks in high energy physics experiments, timing trigger and control applications.**

I. Introduction

POINT-TO-MULTIPOINT optical links are extensively deployed in the Large Hadron Collider (LHC) for Timing-Trigger and Control (TTC) applications, [1]–[5]. These links are unidirectional and carry the level-1 trigger accept (L1A) decision as well as individually addressed or broadcast commands for the various detector sub-partitions [1]–[3]. In the reverse direction, a separate electrical, "throttle/busy" link is responsible for communicating the status of the front-end buffers to the trigger control system (TCS), [4]. Prior to reaching TCS, the "throttle/busy" signals from all front-end buffers within the same partition are logically combined to generate a single signal per detector partition, introducing yet another layer of complexity. TTC links will be upgraded in the future as some of its key components, such as the TTC laser transmitter, have already started becoming obsolete and in addition, it is desirable to simplify the network and to enhance the system's functionalities. A significant simplification in the network architecture and the number of transmission cables and components needed to be installed and maintained would occur if the TTC could be made bidirectional and "throttle/busy" networks were consolidated over the same transmission medium infrastructure. The objective of this work is to develop a general purpose *bidirectional*, serial optical link for TTC and feedback signal distribution, by exploiting the rapidly emerging, passive optical network (PON) transceiver technology in conjunction with field programmable gate arrays (FPGAs). The current paper presents the main features of the developed PON-inspired TTC prototype, as well as reports on the limitations of such a scheme and future work to overcome them.

A number of papers have reported on FPGA based synchronous optical links, some of which are utilizing PON transceivers. Authors in [5] have proposed a TTC distribution optical tree with FPGAs at the end nodes which guarantees fixed latency. However, the reference clock is made available to both ends of the link, a feature that is not available in the TTC systems we are targeting, and, in addition, the implemented optical link is unidirectional. The same authors proposed another FPGA based synchronous implementation, [6], for the replacement of the obsolete GLink chip-set in the ATLAS experiment at CERN, but yet again this link is unidirectional. The White Rabbit consortium, [7], has developed fixed latency, bidirectional optical networks by exploiting the synchronous Ethernet protocol and Gigabit-PON (GPON) transceivers. This scheme implements gigabit serial links; recovers the clock at the destination with low jitter; and constantly monitors the latency. However, signals are routed to the various destinations with Ethernet switches, which are expensive and might introduce an intolerable amount of latency in the delivery of the L1A signal, if used in a TTC context. Finally, authors in [8] also propose a bidirectional optical link with latency monitoring and correcting capability. However, their specific system design allows them to lock both source and destination clocks to a common reference which, as mentioned previously, is not the case in our system.

The paper is organized as following. Section II briefly summarizes the TTC system already installed in the LHC.

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TABLE I
NOMENCLATURE

ASIC	Application Specific Integrated Circuits
BER	Bit Error Rate
CDMA	Code Division Multiple Access
CDR	Clock and Data Recovery
DCM	Digital Clock Management
FIR	Finite Impulse Response
FMM	Fast Merging Module
FPGA	Field Programmable Gate Array
FTTH/P	Fiber to The Home / Premises
GTX	Gigabit-Transceiver
L1A	Level1 trigger Accept
OLT	Optical Line Terminal
ONU	Optical Network Unit
PISO	Parallel In Serial Out
PRBS	Pseudo-Random Bit Sequence
QPLL	Quartz crystal - Phase Locked Loop
SFP	Small Factor Packaging
SIPO	Serial In Parallel Out
SMA	Sub-Miniature version A
SMF	Single Mode Fiber
TCS	Trigger Control System
TDMA	Time Division Multiple Access
TTC	Timing Trigger and Control
TTS	Trigger Throttle System
WDM	Wavelength Division Multiplexing

Section III gives an overview of the proposed PON-TTC concept, approaching it from a system level. Details of the FPGA specific transceiver developments are presented in Section IV. Section V describes the tests carried out to qualify the proposed PON-TTC scheme. Section VI provides a list with potential future developments and improvements and finally, Section VII concludes.

II. LHC Timing Trigger and Control System

The existing TTC architecture in LHC is shown in Fig. 1(a) [1]–[3]. It consists of a TTCex module which communicates with a number of TTCrx receiver application specific integrated circuits (ASICs), [9], [10], via a passive optical tree. TTCex receives information from two channels activated by the trigger control system; Channel A contains the level 1 trigger accept (L1A) decision and channel B carries general purpose commands for the synchronization and calibration of the subdetector partitions. TTCex multiplexes the two channels in time, encodes them and uses the data to drive a bank of up to 10 Fabry-Perot lasers. Data are transmitted through an optical fiber which is about 100 m long and are distributed to a maximum of 32 TTCrxs via an optical fan-out. The downstream data rate is 40 Mb/s and the bi-phase mark format is used to encode the data.

TTCrx acts as an interface between the TTC system and the detector partitions. Its function is to recover the LHC clock and distribute it to the front-end detector electronics. The clock is de-skewed to compensate for variable particle times of flight and cleaned before distribution. The clock can be tuned in fine steps of 104 ps and in coarse steps of 25 ns. The jitter of the recovered clock in the TTCrx, is $\sim$30 ps RMS and a QPLL (TI CDCL6010) filters it to $<$7 ps RMS. TTCrx also demultiplexes channels A and B and delivers the synchronization commands, the L1A trigger-accept decisions and their associated bunch and event identification numbers to the front-end electronics.

A separate electrical "busy/throttle" link delivers feedback on the status of the front-end readout buffers and the data acquisition system to the trigger control system. In fact, the "busy" signals from all sub-partitions are merged in the fast merging modules (FMM) in the CMS case [11] or in the ROD Busy modules in the ATLAS case [12], so that only one signal per detector partition finally reaches TCS. If a front-end buffer is ready to overflow a "warning" signal is issued and TCS inhibits the L1A trigger-accept until the occupancy in the buffers falls below a predefined threshold and a "ready" signal is issued.

III. PON-TTC System

A. Commercial Passive Optical Networks

Passive optical networks are bidirectional, point-to-multipoint optical networks which are employed in the last mile of commercial telecommunication networks to deliver high bandwidth to the end users, [13]–[15]. A typical PON is shown in Fig. 2(a) and consists of a master node or optical line terminal (OLT) which communicates with up to 64 slave nodes or optical network units (ONUs) with the aid of a feeder fiber that can reach 20 km in length, a passive optical splitter and a number of shorter distribution fibers. Two directions of propagation are distinguished; in the downstream, the OLT broadcasts packets to all ONUs, which then decide whether to process them based on an address field embedded in the packets. The transmission medium is shared among the ONUs in the upstream direction and a channel arbitration mechanism is adopted to avoid collisions from multiple ONU transmissions. The arbitration method of choice in the first generation commercial deployments has been time division multiple access (TDMA), [16], [17], but prototypical, symmetric bandwidth PONs based on wavelength division multiplexing (WDM) [18], sub-carrier multiplexing (SCM) [19], optical code division multiplexing (OCDMA) [20] and others have been extensively reported in the literature. PONs are also known as Fiber-To-The-Home/Premises (FTTH/P) networks and are now formally part of the of the Ethernet protocol, (EPON), by IEEE [21]. A second protocol called Gigabit-PON (GPON) by ITU, [22], designed along the principles of asynchronous transfer mode (ATM) and which satisfies more stringent timing requirements also exists.

The work in this paper concentrates on TDMA-PONs, an important feature of which is that data are transmitted in the two opposite directions using two different wavelengths; 1490 nm in the upstream and 1310 nm in the downstream. The two wavelengths are combined/separated by dielectric optical filters in the transceivers, Fig. 2(a), and they co-propagate in a single optical fiber with insignificant interference. A reduction by a factor of 2 in the number of fibers and connectors is gained by basing the

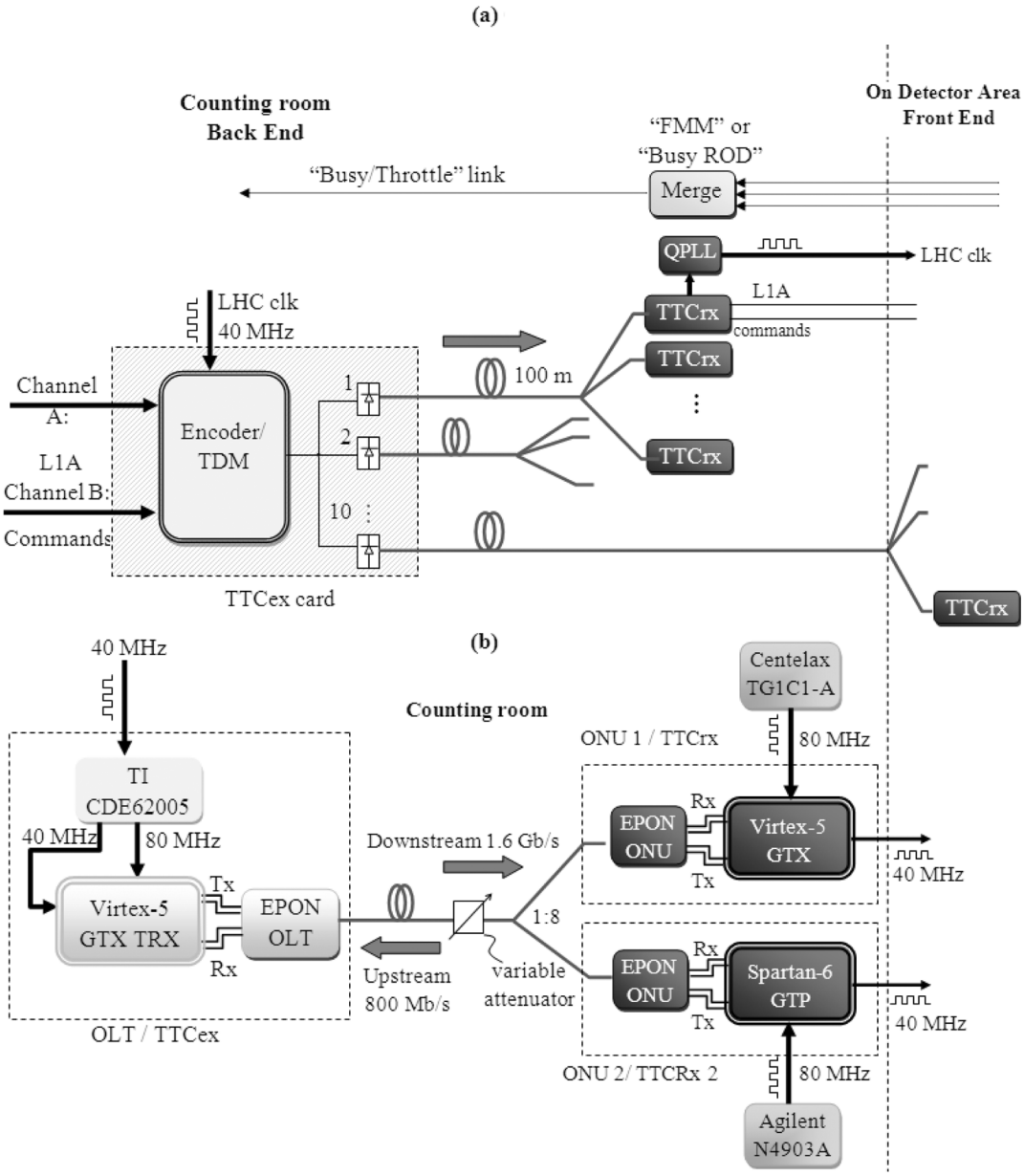


Fig. 1. (a) TTC system currently installed in LHC and, (b) block diagram of PON-TTC prototype.

modules on this design rather than on the popular small factor packaging (SFP) technology, Fig. 2(b).

B. PON-TTC Prototype

The developed PON-TTC system has the following characteristics: i) the downstream link is a low and fixed latency, gigabit link which is capable of carrying the L1A and commands. ii) The 40 MHz LHC clock is recovered from the serial data in the receiver and a deskewing process based on the FPGA digital clock management (DCM) module makes it possible to fine tune its phase. iii) The recovered clock can be used to drive a high-speed serializer for further distribution of data to the detector front-end components and, iv) communication is bidirectional with the upstream link being used to deliver feedback information and monitor the feeder fiber latency. The main properties of the PON-TTC system are summarized in Table II.

A simplified block diagram of the prototype PON-TTC system developed in PH-ESE at CERN is shown in Fig. 1(b). An equivalent TTCex instance has been realized by combining a Virtex-5 FPGA and a commercially available 1G-EPON OLT transceiver (OBL4333F by OESolutions) while two equivalent TTCrx instances have been realized by using a Virtex-5 FPGA and a Spartan-6 FPGA respectively and 1G-EPON ONU transceivers (OBN3433F by OESolutions). A photo of the actual PON-TTC prototype is shown in Fig. 3.

Trigger and Command Distribution Network: A RocketIO GTX transmitter tile of Virtex-5 FPGA in the OLT implements the TCCex logic, which receives the reference 40 MHz LHC clock and generates synchronous frames containing the L1A trigger accept and the commands for the various detector partitions. The frames are serialized in the GTX Tx at a rate of 1.6 Gb/s and are routed out from the FPGA fabric onto a pair of

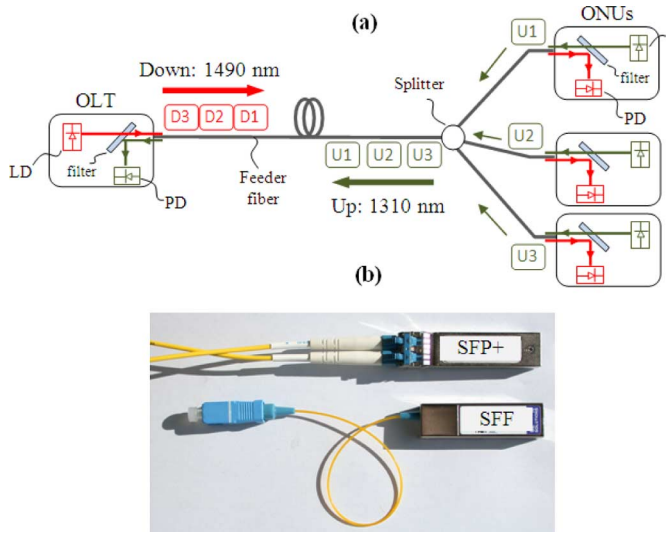


Fig. 2. (a) Commercial TDMA PON, (b) SFP+ and EPON OLT optical transceivers.

TABLE II
PON-TTC CHARACTERISTICS

Property	Value
Clock Rate	40 MHz
Distance	100 m ÷ 1000 m
Encoding	NRZ 8b/10b
Splitting Ratio	64
BW Allocation	Round Robin
Bit Rate Downstream	1.6 Gb/s
Wavelength Downstream	1490 nm
Bit Rate Upstream	800 Mb/s
Wavelength Downstream	1310 nm
Latency Downstream	Fixed and Deterministic

differential SubMiniature version A (SMA) connectors, Fig. 3. This electrical serial data stream is subsequently used to drive the laser in the 1G-EPON OLT transceiver whose optical output is then delivered to the two TTCrxs via a 1 km single mode fiber (SMF). For practical reasons, only two equivalent TTCrx have been implemented in the ONUs of our prototype, but we have emulated the losses of a system that supports 64 ONUs by using a 1:8 splitter and a variable optical attenuator. Note that the implementation of two ONUs only is not introducing any limitations as all properties of interest in a bidirectional optical tree can be investigated with two end nodes.

Optical data received by the 1G-EPON ONU transceivers are converted into electrical data and then routed to the two FPGAs that emulate the TTCrx logic, whose main purpose is to recover a high quality clock from the input datastream and to separate commands from L1A triggers, as mentioned in Section II. The system has to operate under strict timing mandates. The latency through the TTC link must be kept as small as possible to prevent the front-end buffers from overflowing and, in addition, it should be both deterministic and fixed to maintain the stability of the phase of the recovered clock under power cycling or resets of the various electronics in the system pipeline. On the other hand, ONUs should be able to respond to the OLT by sharing the same transmission medium in the upstream direction. To avoid

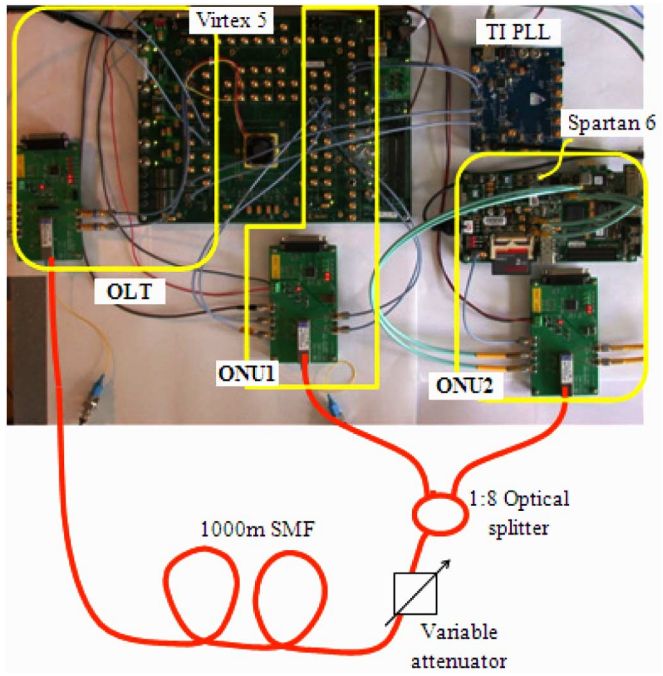
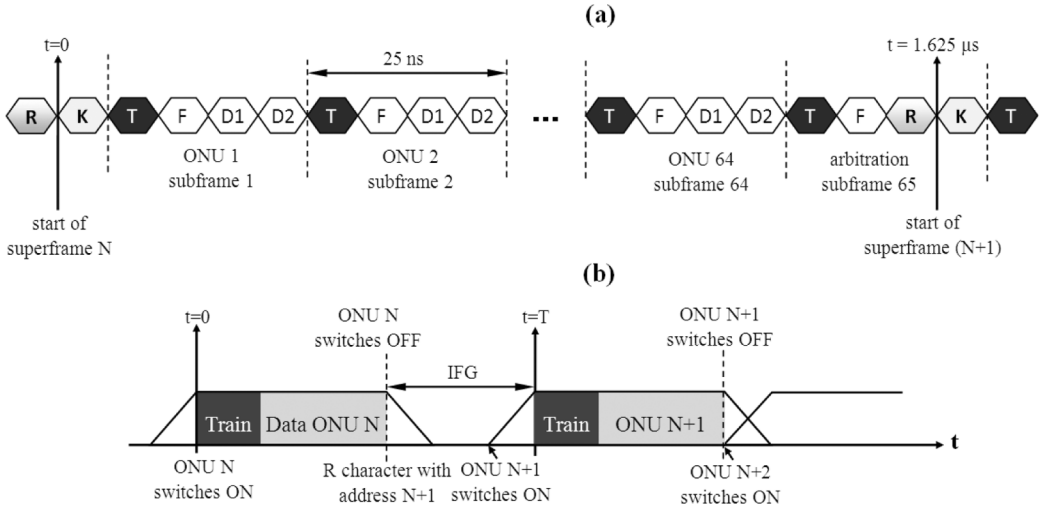


Fig. 3. Photo of PON-TTC prototype.

collisions, a time multiplexing mechanism based on a simple round robin algorithm has been implemented, which has the advantage of keeping the logic in the ONU simple. According to the algorithm, the OLT passes a token to each ONU sequentially and the ONU that holds the token transmits its data over a predefined window in time. These data arrive at the OLT side in bursts, as the distribution fiber lengths cannot be guaranteed to be equal. The bursts have random phases between them and the receiver in the OLT should quickly adjust its decision point in time to be able to reconstruct the incoming data stream with a very low error rate.

C. Protocol of Communication

We begin with the latency critical downstream direction where superframes are continuously transmitted, Fig. 4(a). Each superframe starts with a comma, $\langle \mathrm{K} \rangle$, special character which is used for frame alignment at the receiver. A 1-byte long $\langle \mathrm{T} \rangle$ field follows which carries the L1A trigger decision. A single bit was sufficient for this purpose in earlier implementations, [1], as the trigger decision field was simply signaling whether an interesting event had occurred or not. However, it is expected that it will become necessary to distinguish between different types of events in future experiments and so the trigger field has been extended to satisfy this requirement. An auxiliary $\langle \mathrm{F} \rangle$ field is then transmitted, whose functionality is left open to be defined in the future. Then the $\langle \mathrm{D1} \rangle$ and $\langle \mathrm{D2} \rangle$ fields follow, that carry the commands for the TTCrxs in the ONUs. The commands can be of broadcast type in which case they need to be executed by all ONUs instances or they can be addressing individual ONUs. The distinction between broadcast or individually addressing commands is possible due to the synchronous nature of the superframes. The $\langle \mathrm{T}, \mathrm{F}, \mathrm{D1}, \mathrm{D2} \rangle$ fields constitute a subframe the duration of which is precisely 25 ns at 1.6 Gb/s, so that triggers arrive to the ONUs at a 40



Field	Operation
<K>	Frame alignment and synchronization
<T>	L1A trigger accept decision
<F>	Auxiliary, to be defined in the future
<D1>, <D2>	Broadcasted/individually addressing commands
<R>	Upstream channel arbitration

Fig. 4. (a) Frame structure in the downstream direction, Downstream Superframe (b) upstream channel occupation process. If packets coming from different destinations have similar power levels then a short IFG is sufficient, as can shown between the transmissions of ONU $\mathrm{N}+1$ and ONU $\mathrm{N}+2$, Upstream channel arbitration.

MHz rate, a prerequisite in today's TTC system. There are 65 subframes within each superframe with a total duration of 1.625 μs. Subframes are numbered from 1 to 65 and a local counter implemented in each ONU is incremented with the arrival of each new subframe. Each subframe contains commands for exactly one ONU unless the operation is set to the broadcast mode. This distinction is being made with the first bit in the $\langle \mathrm{D1} \rangle$ field. By referring to the first subframe in Fig. 4(a) as an example, if the first bit in $\langle \mathrm{D1} \rangle$ is 1 then this command is read by the first ONU only, otherwise it is read by all ONUs. Similarly, the commands in the second subframe are intended for the second ONU only, unless we operate in the broadcast mode and so on until the 65th and last subframe is transmitted. The 65th subframe is 3 bytes long to restore the symmetry in the superframe and ends with an $\langle \mathrm{R} \rangle$ character which is used to implement the round robin algorithm in the upstream direction. The local counters in the ONUs are reset at the end of each superframe and they wait for a new superframe. It should be noted that the ONUs recover the commands without errors but take no further action in the present prototype as a TTC system is merely a messenger. It is left to other systems such as the front end detector sub-partitions to react to these commands.

A unique 8-bit address has been pre-assigned to each ONU. The ONUs are continuously receiving the OLT superframes and decode the $\langle \mathrm{R} \rangle$ character which contains the address of the next ONU to occupy the upstream channel. Once an ONU finds a match with the $\langle \mathrm{R} \rangle$ character, it switches its laser on, transmits its data over a predefined window in time and finally, switches its laser off, Fig. 4(b). An interframe gap (IFG) has been introduced between consecutive bursts to allow the burst mode receiver enough time to settle and adjust its decision threshold proportionally to the average power level of the next transmission. Unlike conventional optical links, where lasers are biased above threshold and stay on even when data are not transmitted, the lasers of the ONUs not occupying the transmission medium switch-off. This prevents the accumulation of noise from a large number of sources, which can cause unacceptable signal-to-noise-ratio (SNR) at the OLT receiver. The IFG can last up to a few hundred ns in commercial 1G- and 10G-EPON networks where large dynamic ranges, i.e., the ratio between the average power level of one burst over the average power lever of its preceding burst, of the order of 20 dBs should be tolerated, thus resulting in a considerable amount of upstream bandwidth being wasted. However, since our system will be installed in a well controlled environment, losses are anticipated to be well balanced amongst the various branches of the optical tree and so, the IFG can be minimized by allowing the switch-on and switch-off processes to overlap as shown in Fig. 4(b), significantly saving bandwidth. The minimum IFG was measured to be 50 ns [25], before the quality of the upstream link started degrading for bursts with dynamic range <6 dB, which is a sufficiently large margin for our balanced system. Each upstream frame begins with a training sequence of alternating ones and zeros to assist the receiver in adjusting the position of its vertical sampling point, before the actual payload of the ONU is transmitted.

An important aspect of the PON-TTC is the latency being introduced in the upstream direction. Currently installed "busy/throttle" systems have processing times that range between 2–4 μs, depending on the buffer overflow probability in each detector partition, [2], [4]. On the other hand, each ONU occupies the upstream channel for 1.625 μs in our prototype and in the worst case scenario an ONU might have to buffer its data for a maximum of 102 μs before it is allowed to transmit them. However, such long latencies need not be the case as the much more frequent, auxiliary $\langle \mathrm{F} \rangle$ field can be used for the regulation of the upstream channel in a manner similar to the $\langle \mathrm{R} \rangle$ character, significantly compressing the waiting time. The minimum duration of the upstream frames has been calculated in Table III for the currently used and for other commercially available PON transceiver technologies, where a 4 byte payload has been assigned, as a bare minimum, for the representation of "busy" signals. According to Table III, the upstream frame duration can be reduced to 215 ns, in which case a new ONU address can be carried on

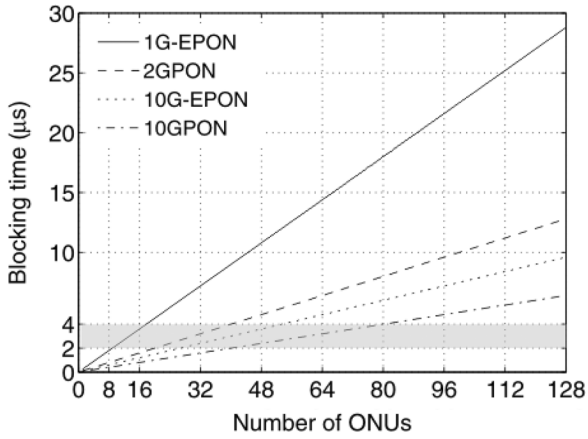


Fig. 5. Upstream blocking time as a function of total number of ONUs for various PON transceiver technologies.

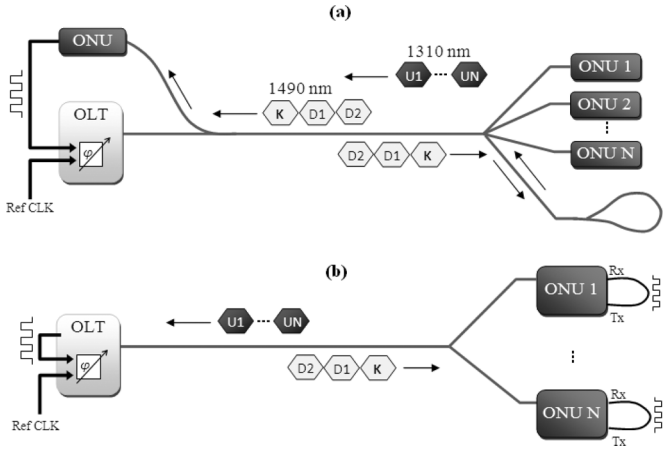


Fig. 6. (a) Feeder fiber latency monitoring scheme and (b) full-ranging latency monitoring scheme.

TABLE III
MIN UPSTREAM FRAME DURATION BREAKDOWN ANALYSIS

Field	1G-EPON (Current)	10G-EPON	2GPON	10GPON
IFG (ns)	50	50	16	16
Training (ns)	125	12.5	125	12.5
Payload (ns)	40	4	40	4
Total per frame (ns)	**215**	**66.5**	**181**	**32.5**
No. of bunch-cycles between transmissions	9	3	8	2

every ninth ⟨F⟩ character. Furthermore, Fig. 5 shows the maximum amount of time that an ONU needs to wait before it occupies the upstream channel as a function of the total number of ONUs in the network and for the calculated minimum frame durations. The requirement for 2–4 μs of upstream latency could be satisfied by the current prototype, if the number of ONUs was reduced to 8–18. Moreover, if next generation 10GPON components were to be used, then 40–80 ONUs could be theoretically served by a TDMA PON-TTC whilst, still complying with the upstream latency requirements. Lastly, there is an additional simplification that a TDMA PON-TTC can introduce to the network architecture; the multiplexing of all "busy" signals over the same fiber presents a natural way to merge these signals, a task currently being undertaken by separate modules. If, for example, all ONUs at the branches of the splitter belong to the same detector partition, then the first upstream frame carrying a "warning" could instantly stimulate a command to throttle triggers. Such a rule is equivalent to the "OR" logical operation being performed by the FMM or the Busy ROD modules. More operations could be implemented for standalone testing and other purposes as well.

D. Latency Monitoring Scheme

The bidirectionality of the PON-TTC can be exploited to monitor variations in the downstream latency due to environmental changes like for example temperature drifts or aging of components. The thermal time delay factor of single mode fibers is ∼25 ps/Km°C [24], mainly attributed to fiber strain, which could introduce a large amount of uncertainty in the phase of the recovered clock, especially in systems using long distribution fibers parts of which might even be installed outdoors.

The latency through the 1 km feeder fiber has been monitored in the PON-TTC by implementing the scheme shown in Fig. 6(a). There are two main modifications compared to the original system presented in Fig. 1(b). The first is that one output of the optical splitter has been looped back to another splitter port and so downstream data are now circulated in the upstream direction. The second modification is that an ONU has been instantiated at the top of the optical tree next to the OLT, and upstream data are now delivered to both of them via a 1:2 splitter. It is reminded that data transmitted in the upstream and downstream directions are using different wavelengths and therefore, do not interfere. The ONU at the top recovers the clock from the circulated downstream data and rejects transmissions coming from the ONUs at the branches. It then shares the locally recovered clock with the OLT where a fine phase comparator has been implemented. The phase of the recovered clock is compared with that of the reference clock, and so any deviations from initial reference value can be detected. Finally, although not yet implemented, the OLT can instruct the ONUs to dynamically reprogram their look up tables to compensate for these phase deviations.

IV. HARDWARE IMPLEMENTATION

A. OLT Transmitter

A Virtex-5 FPGA is used for the OLT transmitter design, a simplified block diagram of which is shown in Fig. 7(a). The reference 40 MHz LHC clock is fed to a CDCE62005 phase locked loop (PLL) by Texas Instrument, which generates an exact copy of the LHC clock as well as multiplies its frequency by 2 to produce an 80 MHz clock. This frequency multiplication step is necessary as the Virtex-5 GTX transceivers require a minimum clock frequency of 60 MHz to operate. The 40 MHz clock is then routed to a frame generator which generates one 32-bit frame every 25 ns to be transmitted in the downstream. Before these bits are allowed to be routed to the Tx-PCS part of the GTX transceiver, the first domain in the GTX transmitter, a gear-box logic has been implemented to perform the transition

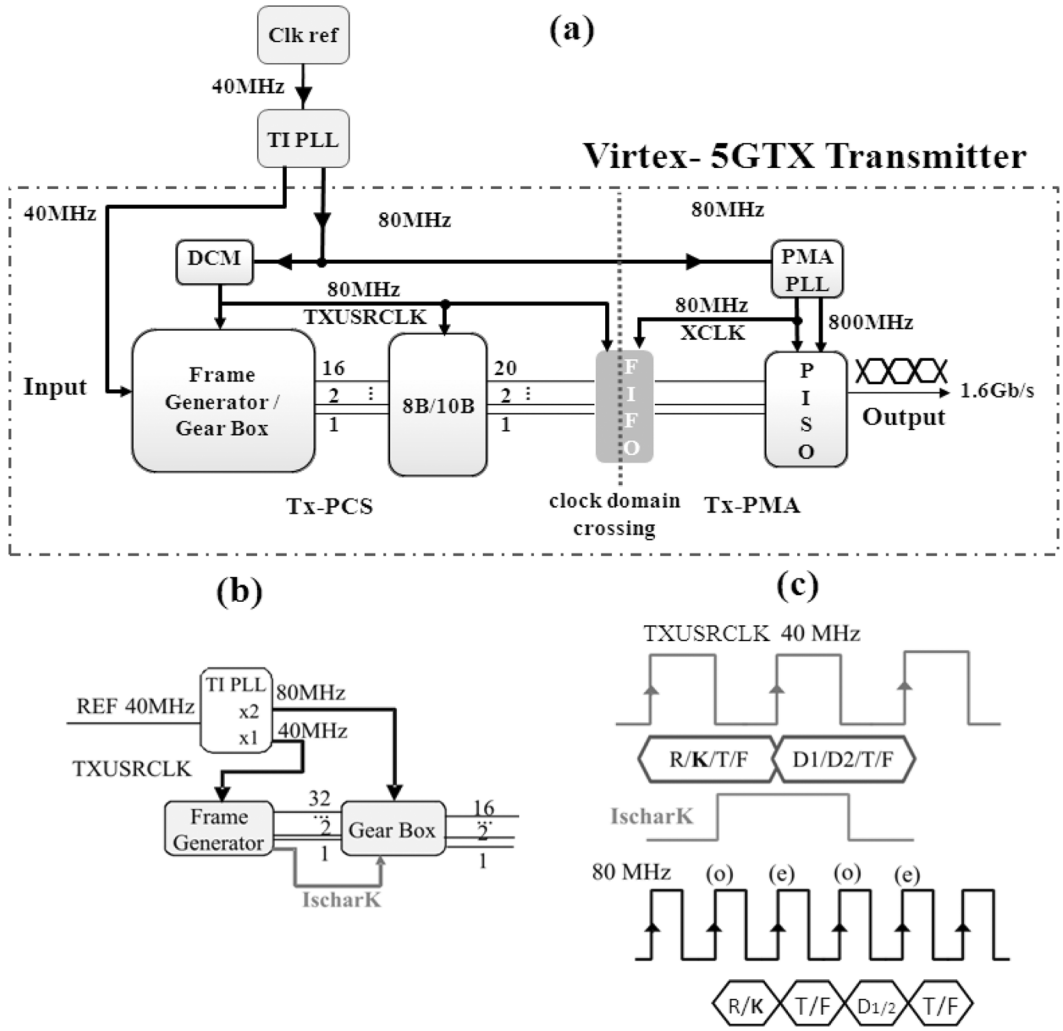


Fig. 7. (a) Simplified block diagram of OLT transmitter, (b) gear-box operation and (c) timing of frames before and after gear-box.

of the operational clock frequency from the LHC 40 MHz to the internal FPGA 80 MHz. The gear box receives the 32-bit frame synchronously with the 40 MHz clock at its input and outputs a 16-bit frame synchronously with the 80 MHz clock. The combined operation of the frame generator and the gear box, which play the role of an equivalent TTCex in our system, is clarified in Fig. 7(b) and (c). The frame generator passes 4 bytes of information to the gear-box on the rising edges of the 40 MHz clock. The operation of the gear-box is equivalent to a multiplexer that outputs the first 2 of the received 4 bytes on the odd edges of the 80 MHz clock and the last 2 on the even edges. Now, every time a comma alignment character is generated, an "IscharK" line is toggled indicating the existence of the $\langle K \rangle$ character to the gear-box. The first edge of the TXUSRCLK (Tx-PCS internal parallel clock) that occurs immediately after the "IscharK" is activated is by convention the first odd edge. In this way, data always exit the gear box in the correct order even after a transmitter reset which might leave the internal counters in arbitrary initial states. The relative timing characteristics and event occurrences are shown in Fig. 7(c).

Next, the 16-bit frames enter an 8b/10b encoder stage which produces parallel 20-bit wide words. A second clock domain transition then occurs between the Tx-PCS domain and Tx-PMA whose main task is to serialize the data. The Tx-PCS and Tx-PMA domains are clocked by TXUSRCLK and by XCLK (Tx-PMA internal parallel clock) respectively, which are not phase aligned, although they need to be for the correct operation of the serializer. The usual method to resolve phase differences between clocks is by employing an elastic buffer on the data path. However, since this buffer may introduce an amount of non-deterministic latency it has been bypassed and the dedicated phase alignment circuit of the GTX transceiver has instead been used that performs the desired alignment by utilizing the PMA PLL. Finally, data enter the PISO (parallel-in-serial-out) block, which serializes them with the aid of an 800 MHz double data rate clock, also coming from the PMA PLL, to generate the 1.6 Gb/s downlink serial datastream.

B. ONU Receiver

A block diagram of the ONU receiver is shown in Fig. 8(a). Although two different FPGA families, Virtex-5 and Spartan-6, were used to implement the two ONUs in order to emulate a real system implementation where more than one technologies

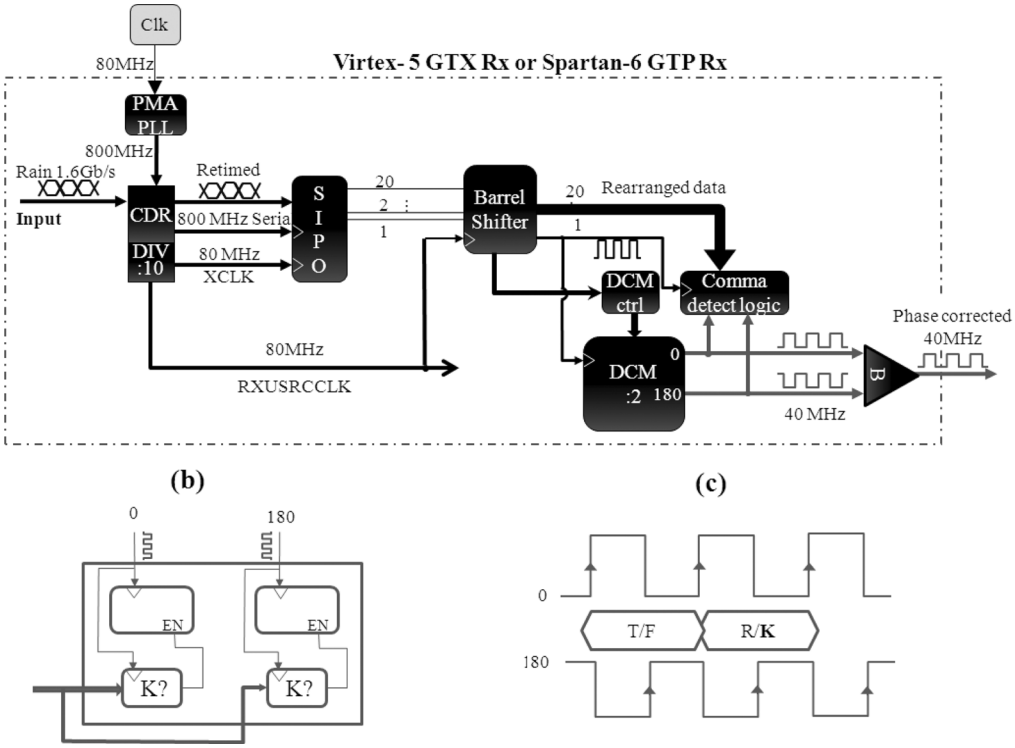


Fig. 8. (a) Simplified block diagram of ONU receiver, (b) comma detect logic implementation and (c) timing of incoming frames relative to the two versions of the recovers 40 MHz clock.

can coexist, both receiver designs are similar. Data are first converted in electrical form in the 1G-EPON ONU receiver and the 1.6 Gbit/s serial datastream is presented to the input of the FPGA receiver clock and data recovery (CDR) circuit. The CDR takes a serial clock from the locally shared PMA PLL, which approximately matches the frequency of the serial data, and adjusts its phase and frequency until it matches the transitions in the incoming data. In this way, a serial 800 MHz double data rate clock is recovered from the data. The CDR then retimes the data and passes them on to the deserializer block or the serial-in-parallel-out (SIPO) circuit. Following, the PMA PLL divides the serial clock to generate the GTX/GTP receiver internal 80 MHz XCLK parallel clock, which is also fed to the SIPO. Serial data are entering the SIPO block one by one on both edges of the 800 MHz double data rate serial clock (every 625 ps) and leave the SIPO in groups of 20 parallel bits every 12.5 ns. The operation of the divider is the most vulnerable part in the receiver with regards to achieving deterministic latency. This is because the 80 MHz XCLK parallel clock can itself in 20 different states after a reset as it can lock on any arbitrary edge of the serial 800 MHz clock. The phase of the XCLK clock can therefore vary in 20 discrete steps of 625 ps each as $\Delta\varphi = N \times 625\,\text{ps}, N = 0 \ldots 19$. In order to detect the exact state of the parallel XCLK clock, a barrel shifter and comma character detection logic has been introduced after the SIPO, Fig. 8(b). Frames transmitted in the downstream always begin with a comma alignment character and therefore, in the event that the parallel clock is initiated on the first edge of the serial clock the first bit of the comma character should come out from the first parallel line of the SIPO. However, if the parallel clock lags behind the serial clock then the first bit of the comma character is transferred to a different from the first parallel line of the SIPO. By shifting the bits in the barrel shifter and counting how many steps it took before the first bit of the comma character reached the most significant bit (MSB), the state of XCLK is precisely determined. To demonstrate the operation of the barrel shifter the phase of a reference, invariant 80 MHz clock has been plotted in Fig. 9 against the phase of the recovered in the two ONUs clocks for all possible barrel shifter values. The relative phase difference between reference and recovered clocks follows a linear trend with the slope of the two lines being 625 ps for both ONU implementations, proving the validity of our method. The information from the barrel shifter is then provided to a control logic which instructs the digital clock management (DCM) block to shift the phase of the 80 MHz clock back into alignment with the reference clock, with the shift values taken from a pre-constructed look-up-table. The DCM must be dynamically reconfigured, as every time the receiver is reset a different value of the barrel shifter might occur. The final step is to halve the 80 MHz clock to derive a copy of the original LHC 40 MHz clock. This step also contains an element of non-deterministic latency as there are two different versions of the 40 MHz that can be recovered differing by 180° as shown in Fig. 8. A final "comma detect" logic has been implemented in order to resolve this ambiguity. The "comma detect" logic samples the data from the barrel shifter with both versions of the 40 MHz clock and looks for the $\langle \mathrm{K} \rangle$ character. When a $\langle \mathrm{K} \rangle$ character is found a counter is incremented, Fig. 8(b). The operation of the whole concept is based on the fact that only one of the two copies of the 40 MHz will see the $\langle \mathrm{K} \rangle$ character, Fig. 8(c), causing its corresponding counter to increment, which is the version that is finally selected with the aid of a multiplexer. A copy of the 40

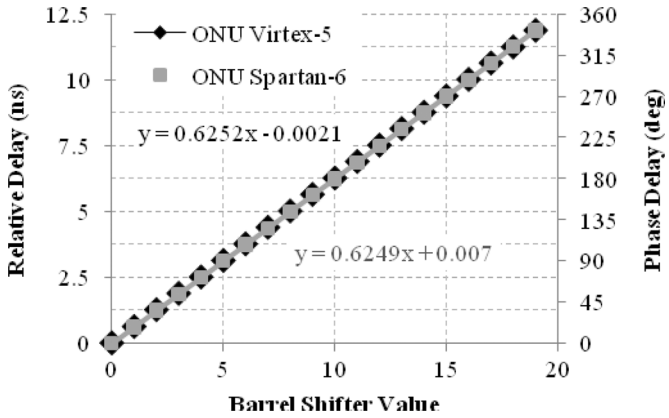


Fig. 9. Relative phase difference between ONU recovered and reference clocks as a function of barrel shifter value.

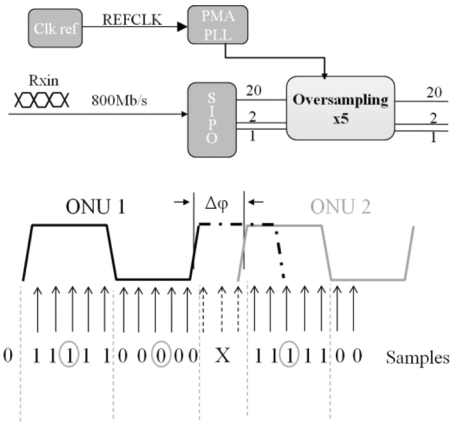


Fig. 10. Block diagram of OLT burst mode receiver based on oversampling circuit of the Virtex-5 GTX receiver.

MHz clock whose phase always remains unchanged even after power cycles or FPGA resets in either transmitter or receiver side, is obtained with this method. After the phase is corrected, data are fed to an 8b/10b decoder (not shown in Fig. 8) and are then available for further processing.

C. OLT Burst Mode Receiver

Data from each ONU are transmitted in the upstream in bursts. The OLT receiver has to be able to retrieve the information from all ONU bursts, a feature which excludes using the same receiver architecture in the OLT as the one implemented in the ONUs. This is because data coming from different ONUs might have an arbitrary phase difference between them causing the CDR to lose lock. Each time the CDR needs to relock to a new burst, a reset process which lasts for 5 μs is instantiated, leading to an excess waste of bandwidth. We are therefore forced to pursue a different architecture, which is based on the oversampling capability of the GTX receiver. GTX receivers have 5x digital oversampling circuits built-in, Fig. 10. If these are used the CDR circuit is not trying to lock on the incoming datastream but instead it is bypassed and data recovery takes place by making use of the blind oversampling technique, [25]. In this case, the incoming data are blindly oversampled at 5x their nominal data rate generating 5 distinct samples per bit. A decision logic subsequently collects all samples from

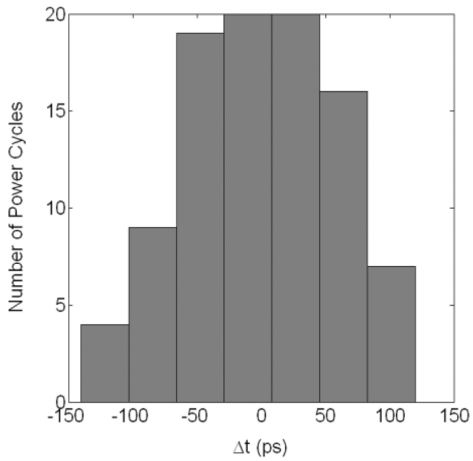


Fig. 11. Histograms of latency stability in Spartan-6 based ONU after 100 system resets.

a predefined window of incoming bits and implements a majority voting algorithm to identify these samples which occur closest to the center of each bit. Since the decision points are continuously updated at the end of each window of bits, data from different ONUs can be correctly received even though two sequential bursts might have random phase differences between them. A clock needs not be recovered from the data nonetheless, it is important to provide a sufficient number of transitions in the upstream data to facilitate the operation of the oversampling circuit. This condition is satisfied by incorporating the training sequence in the upstream frame shown in Fig. 4, which should be longer than 100 bits to ensure error free operation [25].

V. PON-TTC System Characterization

The experiments that were performed to characterize the quality of the recovered clocks are now presented.

A. Latency and Phase Stability of Recovered Clocks

The latency in the downstream direction has been measured and the results are presented in Table IV. The transmitter side contributes 77.11 ns which corresponds to the cumulative time through the GTX transmitter and the 1G-EPON OLT transceiver and evaluation board. The latency through the EPON ONU transceiver board and FPGA receiver at the other end of the link is 139.65 ns, whereas the optical fiber adds another 5 ns/m. The total latency of the PON-TTC system, excluding the optical fiber, is therefore 216.77 ns, which is almost twice that of the current TTC system with a total latency of 90–110 ns, [8]. The excess PON-TTC latency implies that data need to be stored for longer in the detector before they can be read out which is not an option in the LHC currently due to the limited front-end buffer depth. However, this prototype has not yet been optimized to achieve lowest latency. In Section VI we present a strategy of how to reduce the PON-TTC latency to bring it down to a level comparable to the current's system. The phase stability of the recovered clocks in the ONUs has also been characterized after 100 system resets. A system reset is a sequence of a power cycle of the TI CDCE62005 PLL, a reset of the OLT transmitter and a reset of the ONU receiver. The phase of the recovered clock is compared to the phase of the reference

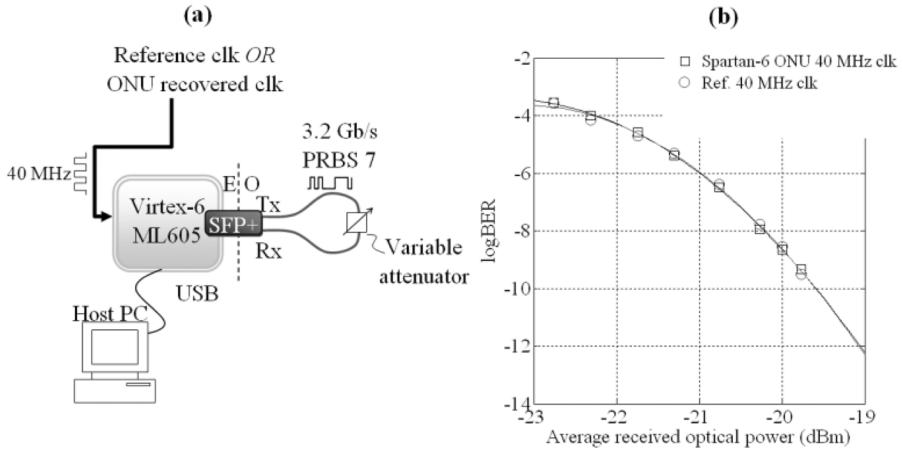


Fig. 12. (a) Set-up used to characterize the quality of the ONU recovered clock based on BER measurements. (b) BER curves of serial data generated by ONU recovered clock and reference clock.

TABLE IV
CURRENT TTC AND PON-TTC LATENCY CHARACTERISTICS

Current TTC	Latency	PON-TTC	Latency
TTCex	25 ns	GTX Tx	75 ns
TTCrx	65-85 ns	EPON OLT Tx	2.11 ns
		EPON ONU Rx	2.16 ns
		GTX – GTP Rx	137.5 ns
Total	**90-110 ns**	**Total**	**216.8 ns**
Optical Fiber	5 ns/m	Optical Fiber	5 ns/m

40 MHz clock after each system reset and a histogram has been built as shown in Fig. 11 for the Spartan-6 based ONU. The peak-to-peak variation of the recovered clock's phase is $<\pm 150$ ps. The uncertainty to the average phase of the recovered clocks should, in theory, equal the DCM step used to perform the phase alignment task, which in our case is ~ 50 ps. The residual uncertainty is due to the implementation of the look-up-table in the ONUs, and it should be possible to be eliminated.

B. Quality of Recovered Clocks

Jitter characterization measurements have also been performed on the recovered clocks in the two ONUs and the results are summarized in Table V. The recovered clocks in the two FPGAs are of similar quality before they are phase shifted and frequency divided by the DCM as both have ~ 17.5 ps of RMS jitter. However, there is a rather large discrepancy between the jitter values for the two FPGAs after the DCM. The 40 MHz recovered clock from the Virtex-5 ONU has a cycle-to-cycle jitter with an RMS value of 36.6 ps while the RMS jitter of the clock from the Spartan-6 ONU is 53.12 ps. Both of these values are too high for the purpose of driving high-speed links, for example National Instrument's DS25C400 Quad 2.5 Gbps SERDES requires an input clock with an RMS cycle-to-cycle jitter of <5 ps, [27] to operate. An external PLL had to be incorporated in the link for this reason, in order to clean the jitter. By using the CDCL6010 PLL by Texas Instrument, [28], RMS jitter values of <4 ps were achieved in both cases. In order to further qualify the use of the recovered clocks to drive a multigigabit serial link we performed a loop-back bit error rate (BER) measurements the set-up of which is shown in Fig. 12(a). The reference 40 MHz clock was used to generate a serial 3.2 Gb/s, pseudo-random bit sequence (PRBS) with $2^7 - 1$ bits, looped-back to the receiver part of the SFP+ via an optical attenuator and the BER was measured as a function of the average received (optical) power. Once this experiment was finished, the reference 40 MHz clock source was replaced with the recovered 40 MHz clock from the Spartan-6 ONU, which had shown the worst performance between the two ONUs, and the BER measurements were repeated. The BER tests were performed by using hardware design containing an integrated bit error ratio test (IBERT) core running in a Virtex-6 FPGA, [26]. The parameters of the experiment and monitoring of the results were performed with the aid of the ChipScope pro analyzer's IBERT console running on a PC and interfacing to the Virtex-6 evaluation board through a USB cable. The objective of the two experiments was to reveal any potential penalties introduced to the BER curves due to the expected degradation of the recovered clocks compared to the BER curves obtained with the reference clock. The results presented in Fig. 12(b) show indistinguishable performance of the examined serial link when the reference 40 MHz and the recovered in the ONU clocks, with no power penalties introduced by the process of transmitting the clock downstream and recovering it from the data, thus qualifying our clock recovery scheme for use in gigabit serial links. It is noted that all experiments to qualify the recovered clocks were performed with the upstream channels being active in order to include the effect of optical and electronic cross-talk.

C. Latency Monitoring

The feeder fiber was placed in a CTS T40/50 climate chamber and the phase of the recovered in the local ONU clock was compared with the phase of the reference 40 MHz clock in the OLT for temperatures in the range $-10°\text{C} \div 50°\text{C}$ with a $5°\text{C}$ step. The phase difference between the two clocks as a function of temperature is presented in Fig. 13 in both phase comparator DCM values, which is the output of our system, and in ps measured separately on an oscilloscope. Measurements are referenced to room temperature which assumes that the two clocks are perfectly aligned at $20°\text{C}$. The phase between the two clocks

TABLE V
PON-TTC JITTER CHARACTERISTICS

Point of Measurement	RMS Cycle-to-Cycle Jitter (ps)
Ref 40MHz	**3.17**
Input OLT FPGA	4.48
ONU1 before DCM	17.33
Recovered 40 MHz, ONU1	36.72
Filtered 40 MHz, ONU1	3.6
ONU2 before DCM	17.5
Recovered 40 MHz, ONU2	53.12
Filtered 40 MHz, ONU1	3.8

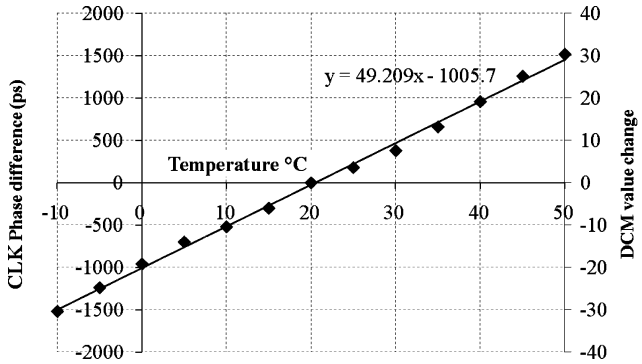


Fig. 13. Phase difference, in ps and in relative DCM values, between reference 40 MHz clock and ONU recovered clock as a function of the temperature in the feeder fiber. Room temperature (20°C) was taken as reference.

increases linearly as temperature increases with the slope of the curve being 49.21 ps. Since the round trip length of the fiber is 2 km (the feeder fiber is 1 km and is traversed twice), the temperature delay gradient of the fiber is 24.5 ps/°C/km, which almost perfectly matches earlier measurements. The DCM was incremented by 6 steps on average every time the temperature in the chamber was changed by 5°C and the phase between the two clocks was increasing by 280 ps. Therefore, the sensitivity of the implemented phase monitoring scheme is 47 ps or $\sim$1°C for the given feeder fiber length.

VI. FUTURE DEVELOPMENTS

Some potential directions for the PON-TTC project will now be presented

Downstream Latency: As mentioned in Section III the latency in the downstream direction is 216.8 ns. This is almost twice that of the current TTC's whose development is based on ASIC electronics which can be optimized by the designer for minimum latency. In contrast, FPGA based architectures involve a number of standard blocks which even when not used they are still introducing excess latency, as for example happens when the elastic buffers are bypassed. As all individual block latencies in the FPGAs are measured in clock cycles, the most straightforward path to reduce it is by doubling the internal clock frequency from 80 MHz to 160 MHz which also implies the increase of the serial data rate from 1.6 Gb/s to 3.2 Gb/s. This is feasible after the recent emergence of the 10G-EPON standard [23], which has made available optical transceivers running at these speeds commercially available.

Full Ranging: The PON-TTC system has a feeder fiber latency monitoring capability built-in, nevertheless, the ultimate goal is to perform a full ranging scheme which is described in Fig. 6(b). In the full ranging scenario, the clock recovered in the ONU receiver from the downstream data is looped-back to the ONU transmitter to generate the upstream data. The OLT then recovers the clock from the upstream data and compares it with the reference LHC 40 MHz clock. The advantages of the full ranging scheme are obvious, both feeder and distribution fiber latencies can be monitored and be corrected for, on an ONU per ONU basis. In addition, initial look up tables do not need to be stored in the ONUs, since they can be constructed and updated on-line as the full ranging algorithm runs. There are two major development steps need to be undertaken in order for the full ranging scheme to be realized. At first, an external clock needs to be fed to the OLT transmitter to kick-off its operation and so a dynamic transition from this external clock to the recovered from the downstream data clock needs to be implemented. Secondly, the latency in the upstream direction must be constant as well in order for the ranging to be meaningful, which is not a requirement that can be guaranteed with the oversampling circuit. Probably, the optimum solution in this case is to split the operation of the system in two phases one dedicated to the ranging mechanism and a second to data transmission.

Non-blocking Upstream Architecture: ONUs have to wait to receive the "token" before they occupy the upstream channel, a process that introduces excess latency. In order to reduce the upstream blocking time, TDMA schemes with faster transceivers can be used as proposed in Section III and/or alternative multiplexing techniques. As only low rate, management data are flowing in the upstream direction, a spread spectrum technique such as the electronic code division multiple access (CDMA) algorithm [27] can be used in a PON-TTC application. According to the CDMA algorithm, data from each user are encoded by using a unique pseudo-random code which runs at a faster rate than the original data. The codes are orthogonal to each other and data from different sources can be separated at the destination by means of cross-correlation digital signal processing. Since ONUs transmit in bursts, an asynchronous CDMA [28] version is required in the PON-TTC context. If N users were to be multiplexed, then each pseudo-random code should contain N bits according to the Walsh-Hadamard [29], or Gold sequences [30], typically employed in asynchronous CDMA systems. CDMA based passive optical networks have already been demonstrated for commercial fiber-to-the-home applications. A bidirectional CDMA PON that supports 32 users at 62.5 Mbit/s over 100 km has been reported in [31], while a faster CDMA PON system that can potentially support 64 users at 280 Mbit/s over 10 km has been demonstrated in [32]. The previous two systems were implemented with ASICs but an FPGA based CDMA PON with potential to support 64 users at 10 Mbit/s over 10 km has been reported in [33]. It is noted that CDMA cannot increase the bandwidth available to each user, but it rather aims to eliminate the blocking time on the ONU side, at the expense of more complex receiver architecture in the OLT. The most important component of a CDMA receiver is the decoder, which in most implementations consists of a phase matched finite impulse response (FIR) filter [27]. Such digital filters can be im-

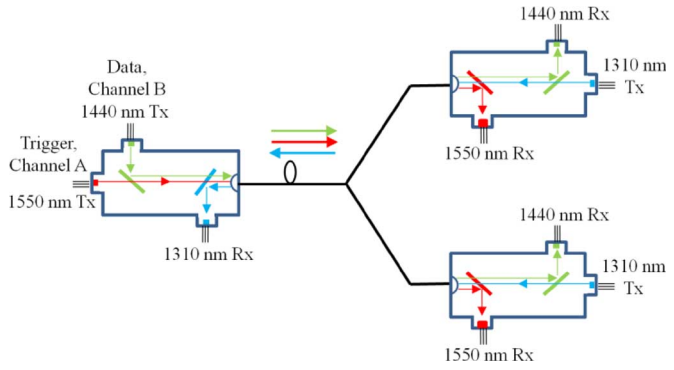


Fig. 14. Clock frequency agnostic TTC implemented with tri-band PON transceivers. L1A are delivered at 1550 nm while commands at 1310 nm.

plemented with high accuracy in FPGAs, while at the same time the decoding process can in principle be restrained to a few clock cycles, by taking advantage of the FPGA parallel distributed arithmetic digital signal processing capability. It is exactly this property that makes CDMA a feasible proposition for PON-TTC systems, as discarding blocking time on one side of the network is *not* traded with an equal amount of processing time on the other. However, a number of issues need to be investigated before such a system can be deployed in a TTC environment. The number of parallel decoders that can be implemented in a single FPGA and the maximum data rate that each user can sustain are still unclear, for example. Such issues will be the subject of future investigations.

Clock Frequency Agnostic TTC: The demonstrated PON-TTC system has been designed to operate with a 40 MHz trigger frequency. If this system is to be used by other experiments running at a different rate, then the communication protocol should change to adapt to the new clock frequency. Another option would be to use the so called tri-band PON transceivers, Fig. 14. Tri-band PONs utilize a 1550 nm band in the downstream in addition to the already existing 1490 nm. Channels A and B can now be multiplexed in wavelength rather than in time and the system can operate free of the trigger rate. Another advantage of using this method is that a conventional protocol, such as Ethernet, can be used to deliver the commands

VII. Conclusion

A bidirectional TTC system has been demonstrated with passive optical network optical transceivers and FPGAs. The developed prototype system satisfies the strict timing mandate of a TTC network - namely fixed and deterministic downlink latency and distribution of a reference clock with low jitter and, also, features a latency monitoring capability. In addition, it has been shown that the main limiting factor for a shared "busy/throttling" uplink to be implemented in a bidirectional TTC is the blocking time that each end-node has to suffer before occupying the upstream channel. In order for this limitation to be lifted, next generation PON transceivers or more advanced, multiplexing techniques would be required, both of which will be subject to future investigations. Finally, although the system has been designed in accordance with the LHC TTC requirements, its implementation is general enough to be considered in other high-energy physics experiments.

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