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ATLAS ABCD Hybrid Fatal Charge Dosage Test

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Abstract:

The Semi-Conductor Tracker (SCT) in the ATLAS experiment at the Large Hadron Collider (LHC) could be subject to various beam loss scenarios. If a severe beam loss event were to occur, it would be beneficial to know how SCT components would be affected. In the SCT detector modules, a key component is the ABCD application specific integrated circuit (ASIC), the onboard readout electronics of the system. This ASIC has design specifications that it should withstand a 5nC charge injection within 25 ns, which is the period of the LHC bunch crossing. The first test performed is designed to test this limit, reaching a maximum of 10nC deposited in 25 ns.

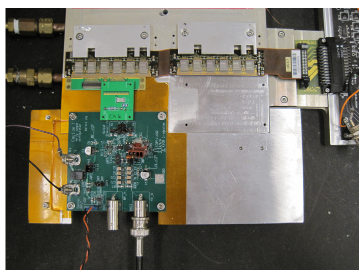
One model for beam loss predicts that a large charge, of the order of 10^6 MIPS, could be incident on the detector. According to detector studies, this causes a local field breakdown between the backplane of the sensor, held at 450V, and the strips. In this case the signal seen on the readout strip has a rise time of about 1μs due to a charge screening effect. A second test is designed to test this discharge scenario, with a maximum of 90nC deposited in 1μs.

Objectives:

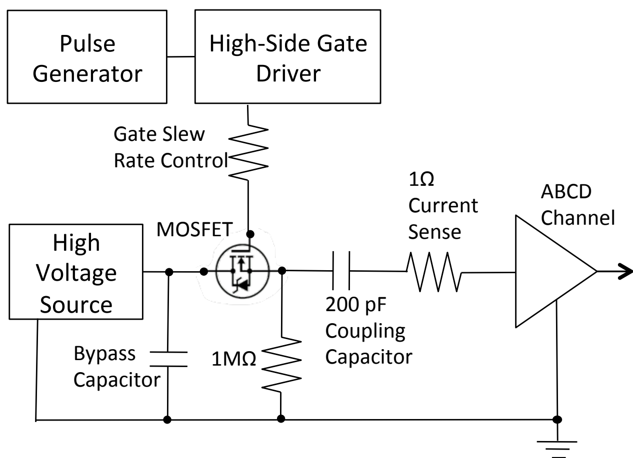
- Validate the 5 nC/25 ns single channel survival specification
- Test beyond this threshold to find point where channel fails
- Test survival of channel when 450 V signal is applied to a coupling capacitor with rise time of approximately 1μs

Experimental Apparatus:

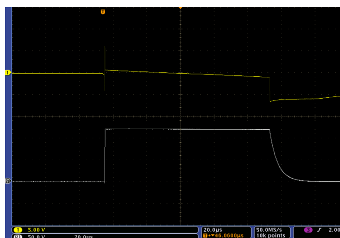
The experimental apparatus is shown in the picture at right. The 12-chip ABCD hybrid is shown at the top, mounted on a cooling block. Two of the chips, each containing 128 readout channels, have been wired for testing. On the bottom left are the charge injection circuits, connected to the hybrid through a jumper board. The data readout cables are seen on the right.

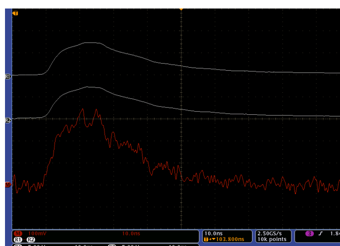


The diagram below shows a simplified version of the charge injection circuit. The MOSFET gate is driven with commercial high-side gate driver ICs, and the 1Ω resistor is used to measure the current flowing into the chip. There are two of these circuits that are used in the study: one that is capable of up to 80V step signal with transition time of 40ns, and another that is capable of up to 450V step signal with transition time of 1μs.



Test Validation:





Two checks were performed to ensure the tests were operating as designed. First, a check was made to show that the current into the ABCD channel from the rising edge of the voltage step is much greater than from the falling edge. Because the magnitude of the charge deposited ($Q = CV$) is equal, and $I = \Delta Q/\Delta t$, the differentiating factor is the duration of the charge deposition. The oscilloscope reading at left shows the voltage step in white and the amplifier input in yellow. It is clear from these measurements that the duration of the rising edge is much shorter than that of the falling edge. Thus, the current from the rise of the voltage step is much greater and the effects of the falling edge can be ignored.

The second check was to make sure the desired amount of charge was deposited into the ABCD channel in the desired amount of time. To do this, the voltage across the 1Ω current sense is measured. This gives a measurement of the instantaneous current dQ/dt. By integrating over a certain period of time, the charge deposited can be found. The oscilloscope reading at left shows this measurement, with the voltage on each side of the 1Ω resistor in white, and the difference in red. In this case, there is about 8nC deposited in 40ns.

Test Procedure/Results:

To test the performance of the chips, the charge injection circuit is connected to the input of a single channel. The pulse generator is turned on for 10s with a 500ms period, resulting in 20 charge pulses delivered to the channel. The charge injection circuit is then disconnected from the ABCD chips. The data readout system, called SCTDAQ, is then used to perform response curve and three-point gain tests to determine whether the chip is still properly functioning.

The first test was aimed at validating the ATLAS collaboration specification that the ABCD survive 5nC deposited in 25ns, or an average of 200mA. In the tests that validated this specification, two different input voltages were used: 40V and 80V. With 80V input, the charge deposited was 16nC in 40ns, which is an average of 400mA, double the specifications. For this test, five channels were tested on one chip, along with two on another chip. No failures were seen on any of the channels.

The second test was aimed at testing a situation where a large charge deposition causes a local field breakdown between the backplane, held at 450V, and the strips. Charge screening effects result in a long signal rise time of about 1μs. With 450V applied to the coupling capacitor of 200pF, the charge applied to the ABCD channel is 90nC. For this test, five channels were tested on one chip, along with two on another chip. Again, no failures were seen on any of the channels.

Input Voltage	Coupling Capacitor	Charge Deposited	Length of Pulse	Average Pulse Current	# of Channels Tested	# of Pulses/ Channel	Test Results
40V	200pF	8nC	40ns	.2A	7	20	Pass
80V	200pF	16nC	40ns	.4A	7	20	Pass
450V	200pF	90nC	1μs	.09A	7	20	Pass

Conclusion:

In the tests performed, no failures were seen in the ABCD ASIC, even for current pulses twice the magnitude specified in the design.

Further tests are currently being explored. In a true LHC beam loss, charge could build up across many channels of the sensor for hundreds of microseconds before the beam is dumped. This could result in large area sensor breakdown, which would lead to the charge stored in the hybrid bias filter to be distributed across the readout channels connected to the affected strips. This could potentially lead to much greater charge injection quantities into a single chip than have been studied thus far.

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