Impact of NBTI Aging on the Single-Event Upset of SRAM Cells

Marta Bagatin, Simone Gerardin, Alessandro Paccagnella, and Federico Faccio

***Abstract*—We analyzed the impact of negative bias temperature instability (NBTI) on the single-event upset rate of SRAM cells through experiments and SPICE simulations. We performed critical charge simulations introducing different degradation patterns in the cells, in three technology nodes, from 180 to 90 nm. The simulations results were checked with α-particle and heavy-ion irradiations on a 130-nm technology. Both simulations and experimental results show that NBTI degradation does not significantly affect the single-event upset SRAM cell rate as long as the parametric drift induced by aging is within 10%.**

***Index Terms*—Electrical stress, heavy ions, negative bias temperature instability (NBTI), radiation effects, single-event upset (SEU), SRAMs.**

I. Introduction

INTEGRATED circuits operating in space must withstand a harsh ionizing radiation environment [1], being subject to total ionizing dose and single-event effects. At the same time, electronic chips are inevitably affected by the same intrinsic degradation mechanisms occurring on Earth during the many years of operation of satellites.

Aging of MOSFETs is one of the hottest topics in CMOS research. In fact, due to the ever-increasing electric field in the insulating layers, the reliability margin of modern devices is rapidly decreasing. There are several phenomena that contribute to the degradation of transistors [2]: channel hot carriers (CHCs), time-dependent dielectric breakdown (TDDB), and negative bias temperature instability (NBTI). The last one, in particular, is considered one of the most pressing threats nowadays [2]. As the name suggests, NBTI is active when a negative bias is applied to a MOS structure (such as in the case of an ON PMOSFET) at high temperature (but well within the operating range of chips). NBTI causes PMOS parameters to change over time due to oxide trapped charge and interface state generation. There are still many open points concerning the underlying physical mechanisms, but a few facts have been established: 1) NBTI is linked to an electrochemical reaction at the Si/SiO_2 interface between holes and hydrogen-passivated bonds; 2) its evolution over time is determined by the rate of this reaction and by the removal of hydrogen from the Si/SiO_2 interface. NBTI has a serious impact on circuit performances. In particular, it has been demonstrated that it degrades SRAM cells in terms of both read and write times and stability [3], [4].

Due to ever-increasing concern about wear-out, several synergetic studies have been carried out over the past years to evaluate possible interactions between ionizing radiation effects and aging. Depending on the studied devices and type of radiation, synergies between electrical stress and radiation effects have been observed or not. In [5], for instance, the authors demonstrate that SRAMs subjected to pre-irradiation burn-in stress feature a smaller total ionizing dose (TID) functional failure level; as far as Flash memories are concerned, Oldham *et al.* recently showed that total ionizing dose has little effect on the endurance of the devices [6]. A few works have analyzed the interplay and the correlation between NBTI and TID [7] and between CHC and TID [8]. These last studies were motivated by the fact that hydrogen is believed to be behind all these phenomena.

In this paper, we look at the implications of NBTI as far as single-event upset (SEU) rate is concerned. To our knowledge, only one work [9] reports on this issue, focusing on the terrestrial environment. To this purpose, we will use a combination of SPICE simulations and experiments. The SPICE approach is adequate for this analysis (as compared to more accurate, but more time-consuming, TCAD simulations) since NBTI is expected to affect the circuit properties of the cell, but not the dynamics of charge deposition and collection.

The paper is organized as follows. Sections II and III describe the simulations setup and results, respectively. Section IV presents the experimental setup, while Section V discusses the irradiation experimental data, and finally it examines the interplay between transistor aging and single-event upset rate for an SRAM cell.

II. Simulation Setup

In this study, we performed simulations of fresh and aged six-transistor SRAM memory cells with HSPICE using models of different technologies (from 180 to 90 nm) freely available through MOSIS [10]. The cells were simulated starting from the 130-nm commercial design (which we experimentally tested) and optimized for the 180- and 90-nm nodes. The characteristics of aged transistors were obtained by changing SPICE parameters using published data and models [11]–[15]. The degradation was set so that the saturation drain current of the aged PMOSFET decreases by 10% when the PMOSFET is constantly on for 10 years (i.e., worst-case condition), which is the maximum parameter drift usually specified by manufacturers.

Manuscript received July 14, 2010; revised August 31, 2010 and September 16, 2010; accepted September 16, 2010. Date of current version December 15, 2010. This work was supported in part by the MIUR under PRIN Project No. 2008K4P7X9, "High reliability fault tolerant digital systems in nanometric technologies: Characterization and design methodologies," and the MAE under Project RAMSES, "Rad-hard memories for storage embedded systems."

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Digital Object Identifier 10.1109/TNS.2010.2084100

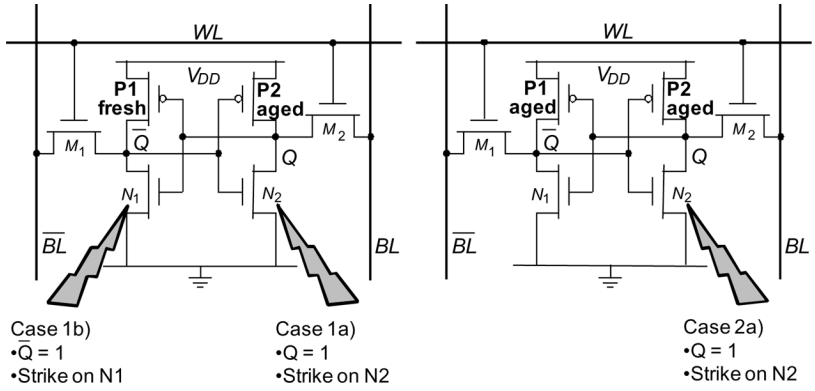

Fig. 1. Schematic of a 6-T SRAM cell depicting the NBTI stressed PMOSFET and heavy-ion struck NMOSFET scenarios analyzed in this paper.

Two different stress combinations were implemented in our simulations:

1) a 10% degradation of a single PMOSFET in the SRAM cell, which mimics the situation in which the cell stores the same logic value for all its lifetime;
2) a 5% degradation of both PMOSFETs in the cell, corresponding to an SRAM that stores zero and one, each for half of its lifetime.

SPICE simulations of heavy-ion strikes were carried out by injecting a current pulse into the drain of the OFF NMOSFET. This is known to be the most sensitive node in an SRAM cell due to the presence of a depletion region that is very efficient in collecting the charge generated by the ion. The ion-induced pulse was modeled through an exponential multiplied by a power law [16]

$$I_{\rm pulse} = \frac{2}{\sqrt{\pi}} \cdot \frac{Q}{\tau_{\rm pulse}} \cdot \sqrt{\frac{t}{\tau_{\rm pulse}}} \cdot \exp\left(-\frac{t}{\tau_{\rm pulse}}\right) \quad (1)$$

where Q is the amount of charge generated by the incoming particle and $\tau_{\rm pulse}$ is the characteristic time of the injected current pulse.

Fig. 1 depicts the SRAM cell and the simulated combinations of stressed PMOSFETs and struck nodes. For simplicity, we considered only strikes on the OFF NMOSFET, which is known to be the most sensitive node. We analyzed the following three scenarios (see Fig. 1). Realistic conditions in which an SRAM cell can operate during its lifetime are in between these.

1) The cell stores a fixed pattern for 10 years, and the ON PMOSFET in the cross-coupled inverter pair (P2 in Fig. 1) is degraded to the maximum level (10%). In this case, the cell loses its symmetry. Afterward:
   a) the OFF NMOSFET (N2 in Fig. 1) is struck by the impinging particle;
   b) the cells are written with the opposite pattern, and the (different) OFF NMOSFET (N1) is struck.
2) The cell stores "0" for half of its lifetime (five years) and "1" for the other half, i.e., both the PMOSFETs (P1 and P2) are degraded to the same level (5%). In this case, the cell remains symmetric after the stress. Afterward:
   a) the OFF NMOSFET (N2) is struck.

Keeping in mind these three possible scenarios, we can simulate the critical charge, which is the most important parameter, at the circuit level, that determines the cell upset rate. To provide a worst-case estimate, parasitic elements due to metal tracks have not been included. Cells belonging to different technology nodes have been simulated (with the supply voltages indicated in Table I) to check the general validity of the results.

TABLE I
$V_{\rm DD}$ VALUES USED IN THE SIMULATIONS FOR EACH TECHNOLOGY NODE

Node [nm]	V_{DD} [V]
90	1.2
130	1.5
180	1.8

For each cell (fresh and degraded), the value of the critical charge, i.e., the minimum injected charge that is required to observe a bit flip, has been extracted. Pulses of different durations $\tau_{\rm pulse}$ have been simulated as well, to emulate particles with different linear energy transfer, hitting the sensitive node with different angles, or strikes occurring more or less near the drain of the OFF NMOSFET.

We also evaluated the time required for the disturbed node voltage to feed back through the cross-coupled inverters and latch the cell in the opposite logic state (cell feedback time) [14].

All simulations were performed with three different technology nodes: 90, 130, and 180 nm.

III. SIMULATION RESULTS

The first step was to degrade the PMOS electrical characteristics by changing the parameters in the SPICE model. The effects of NBTI stress are to induce positive charge trapping and generate interface states in the gate oxide [11]–[15] of ON PMOSFETs. From the point of view of transistor parameters, these give rise to a decrease in the PMOS threshold voltage $(V_{\rm th})$ (which becomes more negative), a decrease in the channel carrier mobility, and a reduction in the subthreshold swing, causing a degradation of both the linear and saturation current.

In this paper, we have chosen to simulate our cells at a maximum degradation level corresponding to a 10% decrease in the saturation drain current $I_{\rm d}$, which is the usual margin specified by manufacturers. SPICE models were altered in order to produce such a degradation with a realistic and consistent change in the threshold voltage and subthreshold swing in order to match the experimental characteristic of an aged transistor [11]–[13].

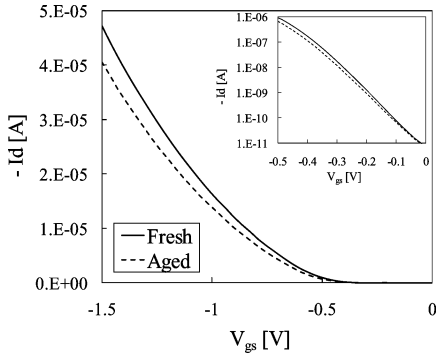

Fig. 2. Simulated $I_{\rm d} - V_{\rm gs}$ ($V_{\rm ds} = V_{\rm dd} = 1.5$ V) characteristics of a fresh and an NBTI-stressed 130-nm PMOSFET (the parameters in the SPICE models were degraded in order to obtain a 10% decrease in the saturation drain current). The inset shows the subthreshold current.

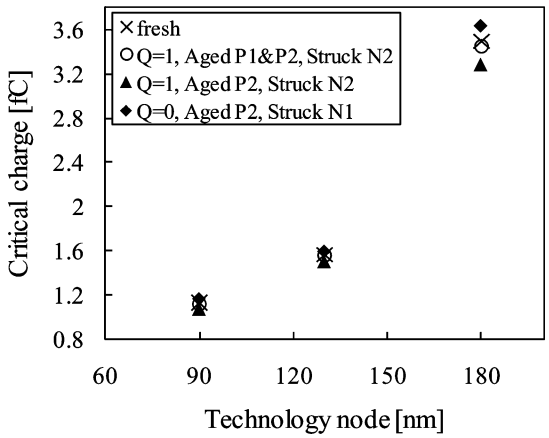

Fig. 3. Simulated critical charge for the SRAM cell as a function of the technology node, in the aging and heavy-ion strike scenarios illustrated in Fig. 1 and with a duration of the ion-induced pulse $\tau_{\rm pulse} = 33$ ps.

The result is shown in Fig. 2, which depicts the simulated $I_{\rm d} - V_{\rm gs}$ curve (with $V_{\rm ds} = V_{\rm dd}$) for an NBTI-aged PMOSFET belonging to 130-nm technology ($V_{\rm dd} = 1.5$ V). The inset in the figure shows the subthreshold current. We can see that $V_{\rm th}$ has become more negative, the saturation current is reduced, and in the inset we observe that the slope of the subthreshold current is degraded in the aged transistor.

Fig. 3 shows the simulated critical charge for an ion-induced current pulse with $\tau_p = 33$ ps in the conditions described in the previous section. As expected, the value of $Q_{\rm crit}$ decreases as the cell size shrinks, meaning that a smaller and smaller charge is enough to flip the latch as technology scales down.

The percentage variations in the critical charge of the aged cell with respect to the fresh cell are illustrated in Fig. 4. As seen in the graph, the critical charge in the stressed cell can either increase or decrease, depending on which of the stress scenarios we consider, but the entity of the variation is always limited below 7%. Two of the main factors whose variations contribute to change $Q_{\rm crit}$ are:

i) the strength of the PMOS connected to the heavy-ion struck NMOS;
ii) the cell feedback time.

In fact, if the struck OFF NMOS is connected to the stressed PMOS, the capability of the aged PMOS to restore the potential

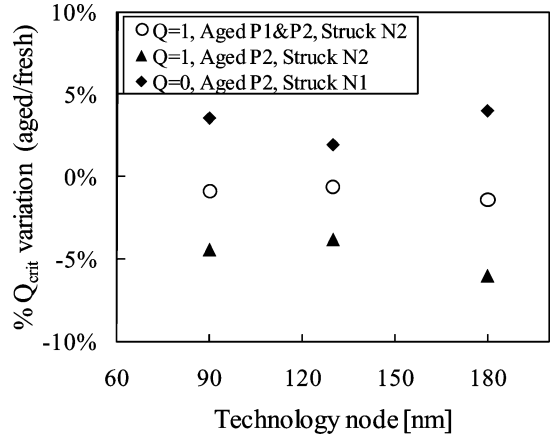

Fig. 4. Simulated percent variation in the critical charge of the SRAM cell with respect to fresh cell ($\tau_{\rm pulse} = 33$ ps), in the aging and heavy-ion strike scenarios illustrated in Fig. 1.

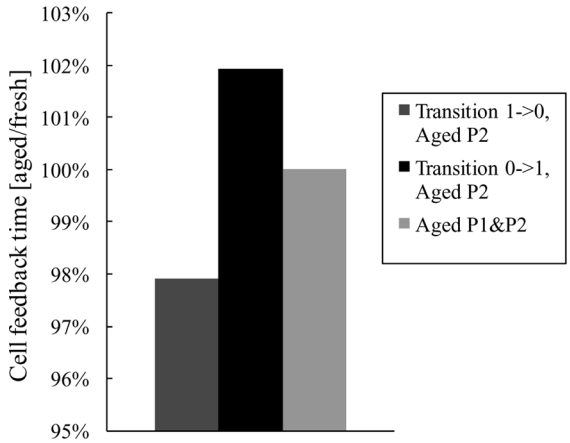

Fig. 5. Simulated percent variation in the cell feedback time. This was evaluated in the three scenarios considered in this work: stressed (10%) PMOS connected to $Q = 1$ (scenario 1.a), stressed (10%) PMOS connected to $Q = 0$ (scenario 1.b), and stressed (5%) both PMOSFETs (scenario 2.a). All variations are expressed in percentage with respect to the fresh cell.

at the struck node is reduced with respect to the fresh cell due to the current reduction caused by NBTI. This has a detrimental effect on the soft error tolerance.

In addition, the cell feedback time can be modified with respect to the fresh cell. It is well known that an increased cell feedback time tends to improve the soft error tolerance, while a decreased feedback time weakens it, because the spurious transients induced by striking particles can be more easily latched by a fast cell [14]. Our simulations prove that, for the stress scenarios considered in this paper, the variations in the cell feedback time are very small, always under 3% in 130-nm cells. As illustrated in Fig. 5, the cell feedback time of the aged cell is slightly increased or decreased with respect to the fresh cell, depending on stress/irradiation pattern combinations. On the contrary, it practically does not change if both P1 and P2 are stressed.

Now, depending on which factor dominates between i) and ii), the critical charge can either increase, decrease, or stay fairly constant. In particular, let us consider the three stress scenarios:

1.a) Both factors i) and ii) go toward the direction of weakening the cell tolerance to soft error. In fact, the PMOS in series to the OFF NMOS is degraded, and thus it has a reduced strength to restore the correct value after the particle strike. In addition, the $1 \rightarrow 0$ cell feedback time decreases (Fig. 5). As a consequence, the critical charge of the cell decreases (see triangles in Fig. 4).

1.b) Factor i) does not come into play because this time the stressed PMOS is not in series to the struck NMOS. On the other hand, factor ii) tends to improve the SEU rate, as the feedback time of $0 \rightarrow 1$ transition is slightly increased (Fig. 5). This explains why the critical charge increases in this scenario (diamonds in Fig. 4).

2.a) Only factor i) determines changes in the critical charge, as the cell feedback time is practically not affected by the stress. The PMOS in series to the OFF NMOS is degraded, but to a lesser extent with respect to case 1.a. As a result, the critical charge remains practically the same as in the fresh cell.

It is worth highlighting that in stress scenario 1), NBTI induces a pattern dependence in the SEU tolerance, 1a) versus 1b). The node to which the degraded PMOSFET is connected is more sensitive because of the lower restoring current, as we have just discussed. In other words, the cell is more sensitive with the stress pattern than with the complementary one.

No clear trend is visible concerning the impact of NBTI on the SEU rate as a function of the feature size (Fig. 4). It must be remarked that in our simulations we considered a 10% maximum degradation independently of the technology, which is a conservative approach. It is well known, indeed, that less scaled devices have an increased lifetime margin with respect to NBTI (i.e., in less scaled devices, 10% degradation will be reached much after 10 years).

The results shown up to now refer to simulations with fixed duration of the particle-induced current pulse ($\tau_{\mathrm{pulse}} = 33$ ps). We also performed simulations with different durations of the current pulse induced by the impinging ion, varying τ_{pulse} in (1), in the range from 3 to 90 ps. In all cases, the simulation results are comparable to the shown case (33 ps). The simulated critical charge tends to increase with increasing τ_{pulse}, but in all cases the variations between the aged and fresh cells are comparable to those we have just shown and always below 6%–7%.

IV. Experimental Setup

For the experimental part of this work, we used 16-kb, 6-T SRAMs manufactured in a standard (non-rad-hard) 130-nm CMOS technology and designed by a leading IP provider, with supply voltage ranging from 1.25 to 1.5 V. The memory was optimized for the specific process and characterized at process corners. One of the most useful characteristics of these memories is the absence of internal voltage regulators, which makes it possible to externally bias the memory cells at the desired voltage, especially during the electrical/temperature stress.

The SRAMs were initially electrically characterized, measuring the supply current and the minimum operating supply voltage. The SEU rate was then assessed on the fresh samples using heavy ions (LET ranging from 2.85 to 54.7 MeV $\cdot$ cm^2/mg) at the SIRAD line of the Laboratori Nazionali di Legnaro (LNL), Padova, Italy [17]. α-particle irradiations of 5.4 MeV (LET < 1 MeV $\cdot$ cm^2/mg) were also performed with a portable 241-Americium source (activity 250 kBq) at the University of Padova, Padova, Italy. The details about all the ion beams we used for this study are reported in Table II.

TABLE II
Details on the Heavy-ion Species Used in This Study

Ion	Energy [MeV]	LET [MeV $\cdot$ cm^2/mg]	Range in Si [μm]	Facility
He	5.4	~0.6	27	^{241}Am source
O	100.9	2.85	109	LNL
Si	121	9.8	44	LNL
Ni	212.8	28.4	33.7	LNL
Ag	256.6	54.7	27.6	LNL

TABLE III
Values Found in the Literature [2]–[4], [11]–[15]

Parameter	Maximum specified	Used during NBTI stress
Supply voltage [V]	1.5	2.5
Temperature [C°]	85	125

Afterward, the samples have been subjected to negative bias temperature instability stress (see Table III): High temperature (125°C) and high voltage (2.5 V, exceeding the nominal supply voltage by 60%) have been simultaneously applied to the memory cells, thanks to the absence of internal voltage regulators, storing a fixed logic checkerboard pattern "AA" (in the following, referred to as stress pattern). The stress was periodically interrupted to electrically characterize the samples and irradiate them with α particles. We chose to focus on α particles because their LET (~ 0.6 MeV $\cdot$ cm^2/mg) is very close to the SEU threshold LET. In fact, the variations we expect from the simulations should be more clearly visible close to the threshold LET than when the cross section is saturated. Finally, at the end of the stress (~150 h), we exposed the memories to heavy ions again. While the pattern stored in the cells during the stress was always the same ("AA"), we measured the soft error rate with both the stress pattern and the complementary pattern ("55"), and changing the supply voltage as well, within the operating range. All irradiations and characterizations have been performed at room temperature, and all heavy-ion exposures (except irradiations with α particles) have been carried out at normal incidence. During heavy-ion exposure, the supply current was constantly monitored to detect possible latch-up events. Three samples were tested in this work.

Particular care was taken in carrying out the measurement as soon as possible (with a delay of some minutes with the Am source, and some hours with the accelerated heavy-ion beam, due to beam setup times) since NBTI has a well-known recovery in the time immediately after the temperature/electrical stress [2]. On-the-fly techniques such as those recently used to characterize MOSFETs are clearly not possible in our case. As a result, the degradation experienced by our stressed samples is actually worse than that shown in Fig. 6. Stress recovery as

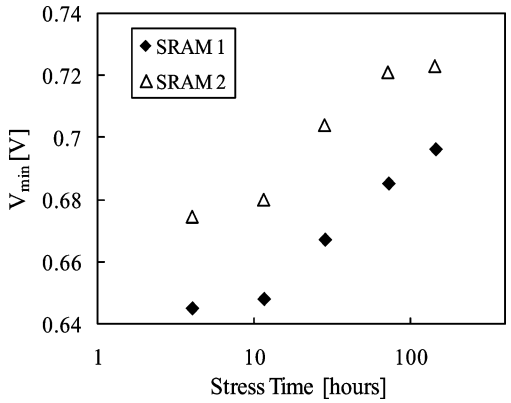

Fig. 6. Minimum operating voltage, i.e., minimum voltage at which no malfunctions (at low speed) are detected in the memory as a function of the stress time. Two samples are displayed in the plot, subjected to the same stress conditions.

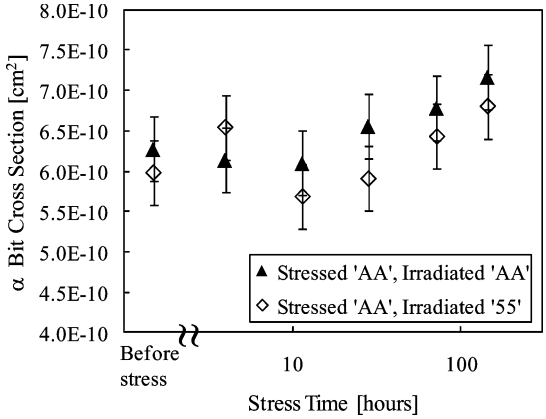

Fig. 7. α-particle sensitivity as a function of the stress received before irradiation, compared to the sensitivity of the fresh sample. "Stressed 'AA', Irradiated 'AA'" and "Stressed 'AA', Irradiated '55'" correspond to scenarios 1a) and 1b) in Fig. 1, respectively.

a function of time is known to saturate at very short times (in the order of tens of seconds) [11], [15], so that waiting a few minutes between the end of the stress and irradiations is not so different from waiting a few tens of seconds. In any case, the difference between $V_{\min}$ at the end of a stress step and at the beginning of the following step was less than 10 mV.

V. Experimental Results

We will now move to the experimental results, discussing the effects of heavy-ion irradiation on NBTI stressed 130-nm SRAM cells. We will focus on scenarios 1.a) and 1.b) since they are the ones that should give the larger variations, according to the results of our simulations.

Some of the samples were stressed at high temperature and high voltage (125°C at 2.5 V), as discussed in the previous sections. The stress voltage, temperature, and time were chosen to generate, at the end of the whole stress, a 10% decrease in the drain saturation current of the ON PMOSFET [11]–[13]. Fig. 6 shows that our devices actually received the desired level of stress. The plot illustrates the degradation of the minimum operating voltage, as a function of the stress time, for two of the memories that have been stressed with a fixed logic pattern stored in the cells. The increase in the minimum supply voltage in stressed samples observed in Fig. 6 is readily explained. As a result of the threshold voltage decrease due to NBTI, the PMOSFET in the cell turns on at a higher voltage (in absolute value). Consequently, the stressed memory starts to malfunction at lower supply voltages. Note that the ~60-mV increase observed in Fig. 6 in the minimum supply voltage is consistent with the stress level we planned to induce on the memory. In fact, a 10% degradation on the PMOSFET drain current corresponds to a $\Delta V_{\rm th}$ of 50–60 mV, as seen in Fig. 2 (no direct measurement of the PMOSFET characteristics in the SRAM is possible on our samples). Note that the experimental data shown in Fig. 6 were collected with the SRAM operated at low speed (of course, performances decrease as we decrease the supply voltage).

Let us now move to the irradiation results. Fig. 7 shows the experimental α-particle bit error cross section for one of the tested memories, as a function of the stress time, for the two

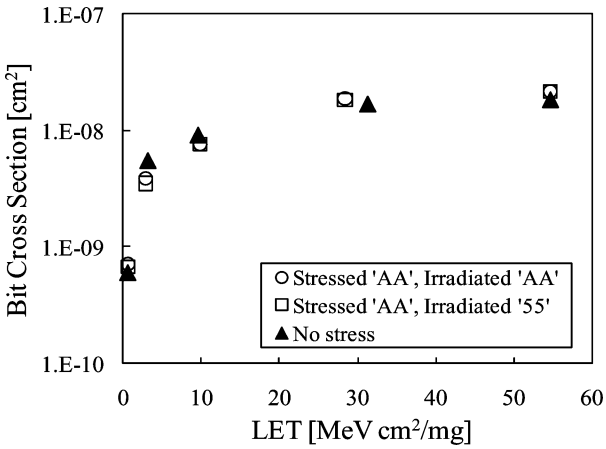

Fig. 8. Heavy-ion bit cross section for fresh and stressed samples. "Stressed 'AA', Irradiated 'AA'" and "Stressed 'AA', Irradiated '55'" correspond to scenarios 1a) and 1b) in Fig. 1, respectively.

logic patterns stored in the cells during α exposure, the stress pattern "AA" and the complementary pattern "55"; this reproduces scenarios 1a) and 1b), respectively.

The cross section in Fig. 7 is constant within the margins of errors. Error bars in Fig. 7 are calculated using Poisson statistics and set at 2σ. They are related to the uncertainty in the error count. The experimental results confirm that NBTI induces small (if any) variations in the SEU rate. Unfortunately, it is difficult to increase the accuracy of the experimental measurement without exposing the samples to a level of TID that alters the results. Nevertheless, we verified that during alpha irradiations, TID effects were negligible and did not affect α bit error cross section for small doses (for each experimental point in Fig. 7, we delivered less than 1 krad(Si) to our samples).

Finally, Fig. 8 shows the data on heavy-ion irradiation. In this case, measurements were done only on fresh samples and after the whole electrical/temperature stress was delivered to the device (~150 h), because of the limited availability of heavy-ion beam time, as opposed to the portable α-particle source. Error bars for heavy-ion cross section are smaller than symbols in the graph, therefore they are not visible in Fig. 8. Once again,

the differences between the fresh and the stressed devices are small and practically within the experimental error. Even in this case, the experimental results do not contradict the conclusions obtained by means of simulation.

VI. Conclusion

Negative bias temperature instability is one of the main reliability problems for current and future CMOS technology. Electronic components used in a space mission are subject, at the same time, to radiation effects and to intrinsic aging phenomena, so it is important to understand how these two reliability aspects affect each other. In this paper, we showed that the parametric shifts induced by NBTI in the range of technologies studied here do not have a large impact on the single-event upset rate calculations, given the uncertainties that already affect these predictions, as long as parametric variations below 10% are considered. Our simulations point to a moderate increase or decrease in the critical charge, hence to a moderate decrease or increase in the soft error tolerance, respectively, depending on the pattern stored in the memory during its lifetime. These small variations ($<7\%$) are very hard to observe experimentally and, in all the studied cases, they are within the experimental errors. According to our findings, neglecting these variations in single-event upset rate calculations is practically of no consequence. We highlight that the results found in this paper are valid for typical devices with standard operating voltage, and larger variations may occur with particular design choices.

Acknowledgment

The authors would like to gratefully thank M. Tessaro, S. Mattiazzo, and D. Pantano for their help with LNL heavy-ion irradiations.

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