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Reliability and performance studies of DC-DC conversion powering scheme for the CMS pixel tracker at SLHC

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ABSTRACT: The upgrades of the Large Hadron Collider (LHC) introduce a significant challenge to the power distribution of the detectors. DC-DC conversion is the preferred powering scheme proposed to be integrated for the CMS tracker to deliver high input voltage levels and performing a step-down conversion nearby the detector modules. In this work, we propose a step-up/step-down powering scheme by performing voltage step up at the CAEN supply unit and voltage step down near the detector. We designed step-up converters and investigate the pixel performance and power loss on the FPIX power distribution system. Tests are performed using the PSI46 pixel readout chips on a forward pixel panel module and the DC-DC converters developed at CERN and Fermilab. Reliability studies include the voltage drop measurements on the readout chips and the power supply noise generated from the converter. Performance studies include pixel noise and threshold dispersion results. Comparison between step-down only and step-up/step-down conversion powering schemes are provided.

KEYWORDS: Voltage distributions; Detector design and construction technologies and materials; Digital electronic circuits

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1 Introduction

The Large Hadron Collider (LHC) will be upgraded to the Super-LHC (SLHC) with increased luminosity by a factor of 5 or more. This imposes an increase in data flow and readout channels. To handle this increase, the detectors have to be updated with finer segmentation or adding more channels which would in turn introduce a significant challenge to the power distribution of the detector. The current powering scheme implemented for LHC based on individual powering for every module, will face challenges due to voltage and current limitations from the power supply units and voltage drop on the power cables. In this work, we analyse the use of DC-DC converters to efficiently distribute power to the detector electronics. Additionally, this paper proposes a power distribution scheme based on the use of step-up DC-DC converters by the power supply unit and step-down DC-DC converters by the detector modules to efficiently distribute power and reduce the power loss on the cables. Step-down DC-DC conversion is the preferred powering scheme proposed for the CMS upgrade pixel detectors [1]. In this work, we provide an in-depth study of the DC-DC powering scheme with step-down only and step-up/step-down converters by investigating the power integrity of the system and pixel performance for the forward pixel detector panel.

2 FPIX power distribution scheme

The current CMS Forward Pixel Tracker [2] has 4320 readout chips or ROCs. The upgraded CMS FPIX will host 10752 ROCs where each power group contains 224 ROCs arranged in 7 blades (each blade has two modules each of 16 ROCs). The power lines pass through several boards and up to 45 meters of cable to reach the pixel modules. For the step-down scheme, figure 1 illustrates the global power distribution from the power supply to the blades.

In this scheme, each power supply unit (A4603 module [3] produced by CAEN, S.A. Italy) powers 224 ROCs which constitute $1/8^{th}$ of the disk for the Forward pixel system. The plan is to use

Figure 1. FPIX power distribution scheme with step-down DC-DC converters.

Table 1. Power analysis when no converters used.

	V (caen)	I (caen)	Pwr (caen)	Vdrop (cable)	Vrocs	Irocs	Pwr_rocs	Pwr_loss
Digital	6.62V	8.6A	57W	3.62V	3V	8.6A	25.8W	31W
Analog	5.2V	5.6A	29W	3.27V	1.9V	5.6A	10.64W	18.3W

Close to 6A limit of CAEN

Surpasses 28W limit of CAEN

Table 2. Power analysis with step-down converters.

	V (caen)	I (caen)	Pwr (caen)	Vdrop Cable	Vin (dc-dc)	In (dc-dc)	Eff	Ratio	Vrocs (out dc-dc)	Irocs (out dc-dc	Pwr (rocs)	Ploss=Pcable+Pconv
Digital	8.3V	5.4A	44.8W	2.3V	6V	5.4A	0.8	2	3V	8.6A	25.8W	18.7W
Analog	5.84V	3.5A	20.4W	2.04V	3.8V	3.5A	0.8	2	1.9V	5.6A	10.64W	9.8W

Surpasses 5.8V limit of CAEN

Surpasses 7V limit of CAEN

two step-down DC-DC converters to power up each group, one for the digital and one for the analog power line. There is a total of 672 step-down DC-DC converters for the complete upgraded FPIX system. We perform analysis of the power distribution scheme before and after any converters are used, in order to understand the constraints of the powering schemes. The current A4603 CAEN power supply unit has the following specifications: Analog Line has Vset=2.3V, Vmax=5.8V, Max Power=28W, Max Current=6A, and Digital Line has Vset=3.3V, Vmax=7V, Max Power=88W and Max Current 13A. In table 1, we show the cable power loss and estimated voltage/current requirements of the CAEN supply unit when no converters are used, based on our current estimate of the analog and digital current that would be needed for the ROCs to operate properly at a luminosity of $2x10^{34}/cm^2$ per sec. In table 2, we show the same analysis when step-down DC-DC converters are used near the detector modules as shown in figure 1.

As shown in table 1, the analog current is close to the CAEN limit and analog power surpasses the CAEN unit specifications. This analysis clearly shows that the current powering scheme will be not be applicable for the SLHC upgrades due to the larger current and power demand of the detector modules. In table 2, we show the same analysis when step-down DC-DC converters are used on the powering scheme. We make the assumptions that the converter efficiency is 80% and conversion

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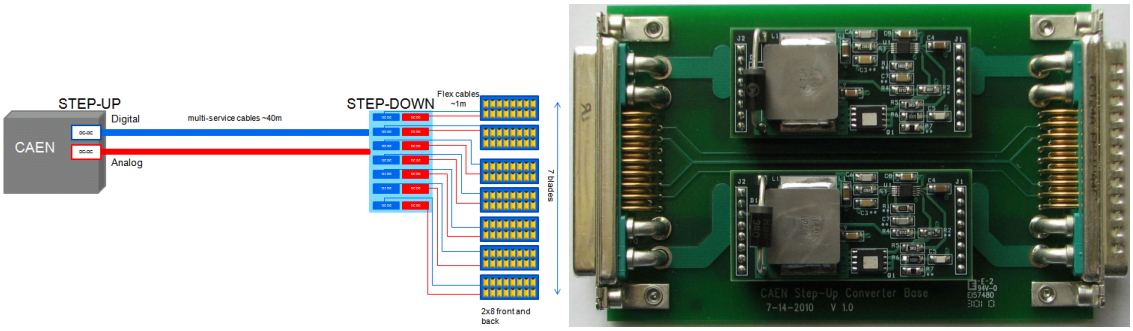

(a) (b)

Figure 2. (a) Step-up/Step-down approach and (b) step-up converters that were designed.

Table 3. Digital power analysis.

	CAEN Output			STEP-UP CONVERTER						STEP-DOWN CONVERTER					ROCS			
	V (CAEN)	I (CAEN)	Pwr (CAEN)	Eff	Ratio	Vout (V)	Iout (A)	Pwr_out (W)	Vcable (V)	Iin (A)	Vin (V)	Pin (W)	Eff	Ratio	Vrocs (V)	Irocs (A)	Pwr_rocs (W)	Ploss=Pstep_up+Pcable +Pstep_down
good	5.50	11.96	65.82	0.80	2.00	11.01	4.78	52.66	2.01	4.78	9.00	43.05	0.60	3.00	3.00	8.61	25.83	39.99W
good	5.36	10.25	54.95	0.80	2.00	10.72	4.10	43.96	1.72	4.10	9.00	36.90	0.70	3.00	3.00	8.61	25.83	29.12W
good	5.25	8.97	47.12	0.80	2.00	10.51	3.59	37.69	1.51	3.59	9.00	32.29	0.80	3.00	3.00	8.61	25.83	21.29W
good	6.75	8.97	60.57	0.80	2.00	13.51	3.59	48.46	1.51	3.59	12.00	43.05	0.60	4.00	3.00	8.61	25.83	34.74W
good	6.65	7.69	51.09	0.80	2.00	13.29	3.08	40.87	1.29	3.08	12.00	36.90	0.70	4.00	3.00	8.61	25.83	25.26W
good	6.57	6.73	44.16	0.80	2.00	13.13	2.69	35.33	1.13	2.69	12.00	32.29	0.80	4.00	3.00	8.61	25.83	18.33W

ratio is 2. The power loss using step-down converters compared to no converter scheme is reduced due to the lower current and voltage drop on the cables. However, the voltage requirement from the CAEN supply unit still surpasses its limit which constraints the implementation of this scheme. In the meantime, this analysis is performed assuming the efficiency of the step-down converter is 80%, where in a real system the efficiency would vary or even degrade due to radiation. One solution is to upgrade the current CAEN supply unit for larger voltage and current limits; however such upgrade could be quite expensive. Another, alternative solution which we propose in this paper is to perform a step-up conversion of voltage by the CAEN supply unit and then a step-down by the detector modules. In figure 2a, we show the FPIX power distribution utilizing both step-up and step-down DC-DC converters. The analog and digital step-up converters are inserted by the CAEN supply unit to increase the voltage and lower the current which ultimately lowers the voltage drop on the cables. At the detector end, a step-down conversion of the voltage is performed to power up the pixels.

In this approach, the step-up converters are cost-effective by utilizing commercial parts. Stepping up the voltage also relaxes the efficiency constraints of the step-down converters by providing a wider range of input voltages. In figure 2b, we show the step-up converters which we designed utilizing commercial parts. The two step-up converters reside on a carrier board which is connected to the back of the CAEN supply unit and multiservice cables. The carrier board allows the high voltage (HV) to pass through, while the sensors are connected to VA and VD voltages.

The sensors purpose is simplified due to the step-up and step-down conversions. In table 3 we show the power analysis performed for the digital power line. The table shows the current and voltages for step-up and step-down converters. The analysis is performed assuming 80% efficiency and conversion ratio of 2 for the step-up converter while the efficiency of the step-down converter can vary from 60% to 80% with conversion ratio 3 and 4. This analysis demonstrates that there

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Table 4. Power comparisons between different schemes for digital line.

Digital	No Conv.	Step-Down Conv. Only	Step-Up/Step-Down Conv.
Pwr_CAEN	57W	44.8W	44.16W
Pwr_ROCs	25.8W	25.8W	25.8W
Pwr_LOSS	31W	18.7W	18.33W
Requires CAEN modifications	Yes	Yes	No

Table 5. Analog power analysis.

	CAEN Output			STEP-UP CONVERTER						STEP-DOWN CONVERTERS					ROCS			
	V (CAEN)	I (CAEN)	Pwr (CAEN)	Eff	Ratio	Vout (V)	Iout (A)	Pout (W)	Vcable (V)	In (A)	Vin (V)	Pin (W)	Eff	Ratio	Vout (V)	Irocs (A)	Pwr_rocs (W)	Ploss=Pstep_up+Pcable +Pstep_down
	3.76	7.78	29.23	0.80	2.00	7.52	3.11	23.39	1.82	3.11	5.70	17.73	0.60	3.00	1.90	5.60	10.64	18.59W
	3.63	6.67	24.19	0.80	2.00	7.26	2.67	19.35	1.56	2.67	5.70	15.20	0.70	3.00	1.90	5.60	10.64	13.55W
good	3.53	5.83	20.60	0.80	2.00	7.06	2.33	16.48	1.36	2.33	5.70	13.30	0.80	3.00	1.90	5.60	10.64	9.96W
good	4.48	5.83	26.14	0.80	2.00	8.96	2.33	20.91	1.36	2.33	7.60	17.73	0.60	4.00	1.90	5.60	10.64	15.50W
good	4.38	5.00	21.92	0.80	2.00	8.77	2.00	17.54	1.17	2.00	7.60	15.20	0.70	4.00	1.90	5.60	10.64	11.28W
good	4.31	4.38	18.86	0.80	2.00	8.62	1.75	15.09	1.02	1.75	7.60	13.30	0.80	4.00	1.90	5.60	10.64	8.22W
good	5.30	4.67	24.71	0.80	2.00	10.59	1.87	19.77	1.09	1.87	9.50	17.73	0.60	5.00	1.90	5.60	10.64	14.07W
good	5.22	4.00	20.87	0.80	2.00	10.43	1.60	16.70	0.93	1.60	9.50	15.20	0.70	5.00	1.90	5.60	10.64	10.23W
good	5.16	3.50	18.06	0.80	2.00	10.32	1.40	14.44	0.82	1.40	9.50	13.30	0.80	5.00	1.90	5.60	10.64	7.42W

Table 6. Analog power comparisons between different powering schemes.

Analog	No Conv.	Step-Down Conv. Only	Step-Up/Step-Down Conv.
Pwr_CAEN	29W	20.4W	18.06W
Pwr_ROCs	10.64W	10.64W	10.64W
Pwr_LOSS	18.3W	9.8W	7.42W
Requires CAEN modifications	Yes	Yes	No

are various voltage ranges for which step-up powering scheme can operate while accommodating different efficiencies of the step-down converters which may degrade over time. We highlight the scenario for which the step-up/step-down approach has the minimum power loss. However, as the efficiency of the step-down converter degrades the power loss of the system increases as well. Similarly, we re-perform this analysis for the analog power line while keeping the same assumptions for the efficiency and conversion ratio of the step-up converter. Table 5 shows the analog line power analysis. Table 4 and 6 show the power comparisons among different schemes. In comparison, step-up/step-down approach has the most reduced power loss and no need for CAEN unit upgrade.

3 Step-up converters

We utilize a boost dc-dc converter for stepping up the voltage. Boost converters are preferred for stepping up voltage due to their low conduction loss and simplicity in the design. Figure 3a shows a simple schematic for boost converters. The principle behind the boost converter is the energy accumulated at the inductor. When the inductor is being charged, it acts like a load and absorbs energy and when being discharged, it is an energy source (like a battery) and it allows higher voltages to be output. There are two operating stages of the boost converter depending on the state of the NFET switch. When the switch is on, the inductor current increases, and when the

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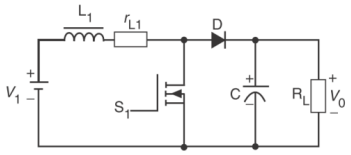

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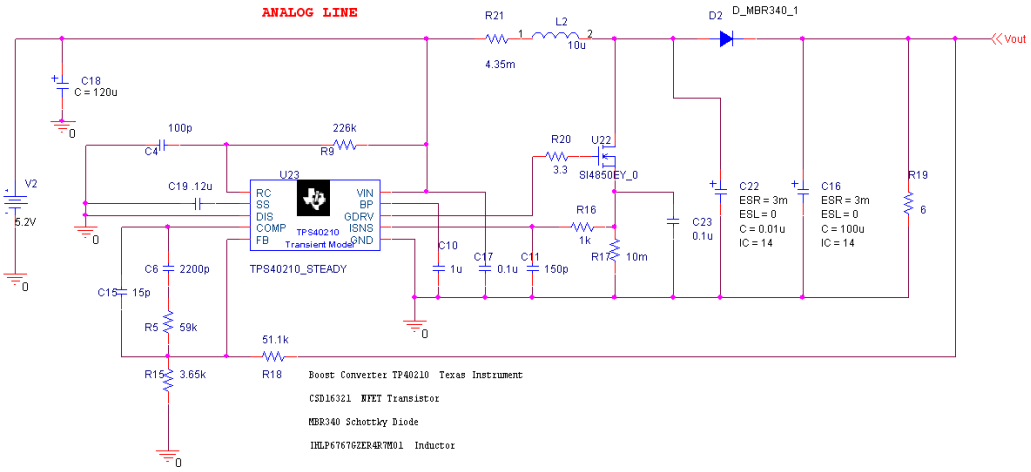

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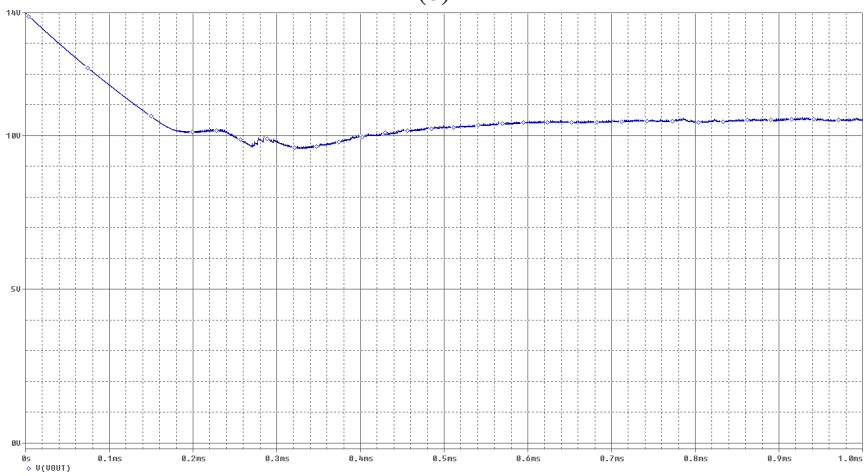

(c)

Figure 3. (a) Boost converter circuit, (b) schematic of our step-converter and (c) SPICE simulation for the step-up converter schematic shown in 3b.

switch is off, the inductor current flows through the diode, the capacitor and load resistance. This results in transfer of energy accumulated at the inductor. In this work, we utilize part TPS40210 [4] of Texas Instrument, which is a wide-input voltage range (4.5V to 52V) boost controller. Given that the analog and digital voltage/current requirements differ, we designed two separate step-up converter using TPS40210 controller. Figures 3b and 3c shows the schematic and output voltage of the converter from simulation for the analog power line. The step-up converter for the digital line is constructed similarly with the exception of a few changes on the resistance and capacitance values to allow different voltage level output for the digital line.

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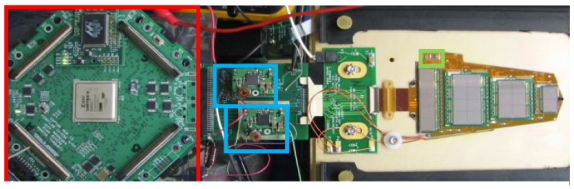

Figure 4. Pixel test stand with CAPTAN system, two step-down AMIS2 DC-DC converters [7], and a forward pixel panel with four plaquettes.

4 Pixel test-stand

We utilize the forward pixel panel to study the pixel performance when powered by the DC-DC converters. Figure 4 shows the pixel test stand. The pixel panel has four pixel plaquettes of different sizes as shown in the right side of the figure 4. The plaquettes are integrated together on high density interconnect (HDI) flex-circuit [5] which are controlled by the token bit manager (TBM) [6]. The DC-DC converters provide power to V_{analog} and $V_{digital}$ of the pixel module. To power up the pixel test stand, we utilize the CAEN power supply unit along with multi-service cables which are the same ones utilized in the CMS detector at LHC. The CAEN power supply unit supplies voltage to the input of the step-up converters for step-up/step-down approach or it is connected directly to the input of step-down converters for the step-down only approach. DC-DC converters power the analog and digital lines of the pixel panel. The panel module has the flexibility to be powered either directly by the CAEN unit (no conversion) or through the DC-DC converters for step-down only and step-up/step-down powering schemes. To cool the pixel panel and the DC-DC converters, we utilize a foam box which is insulated and dry nitrogen air is flushed internally. We run our experiments with low temperatures at the chiller box set to 2°C.

5 Pixel performance analysis

The metrics for pixel performance are based on noise and threshold dispersion of VCAL register, which is equivalent to varying the amount of charge injected to the pixels. We scan the pixels with various VCAL values to obtain their response. Power supply noise can impact pixel performance, and by varying the values of the VCAL register, we aim at finding the impact that power supply noise imposes on the pixels.

There are four test scenarios for which we measure pixel performance: (1) no converter and no cooling, (2) no converter with cooling, (3) converter and no cooling, and (4) converter with cooling. Figure 5a, 5b, and 5c show the pixel test stand. For each of these testing scenarios, we ensure that the voltage and current load remains the same. With cooling, the current drawn by the pixels changes, so we ensure that each ROC's operating bias corresponds to an analog current drawn to *24mA*. To control the amount of current drawn from each ROC, we vary the register value *VANA*. We compute threshold dispersion and noise from the S-curves of pixel response. The S-curve can be represented as a Gaussian distribution by taking its first order derivative. The *threshold dispersion* is the mean, and *noise* is the standard deviation of the Gaussian. In figure 5d we show the measured threshold, pixel noise and VCAL shift for step-down and step-up/step-down powering schemes. We note that the efficiencies on the step-up and step-down converters are lower

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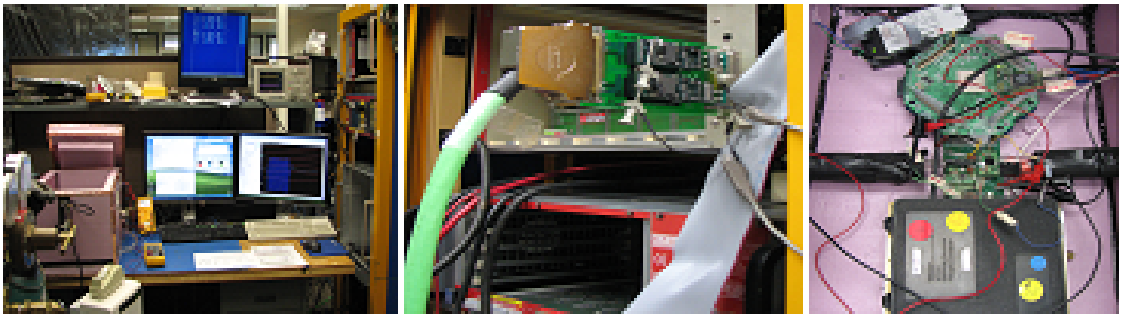

(a) (b) (c)

Comparisons		Step-Down Only	Step-Up/Step-down
Threshold		61.7	57.1
Pixel Noise		258eV	169eV
Peak power supply noise		149mV	268mV
Vcal Shift		1105eV	910eV
Power loss	Analog	0.55W	2.37W
	Digital	1.3W	0.98W
	Total	1.85W	3.35W

(d)

Figure 5. (a) Pixel test stand, (b) step-up converters inserted in the back of CAEN, (c) pixel plaquettes, DAQ system and step-down converters inside the cooling box, and (d) comparison between step-down only and step-up/step-down powering schemes.

than expected. Additionally, the application of the step-up/step-down scheme is not as efficient as expected due to the small current load in the pixel test stand (21 ROCs). Step-up converters are designed to drive 7 blades or 224 ROCs. However, the application of the step-up/step-down approach is promising as it can reliably distribute the voltage and current with less power loss and minimal impact on the pixel performance without requiring expensive upgrade of CAEN supply unit.

6 Conclusions

In this work, we perform pixel performance studies for the CMS Forward Pixel Detector when powered by DC-DC converters for step-down only conversion powering scheme. We propose and describe a novel step-up/step-down powering scheme which facilitates the use of the existing supply unit while further reducing the power loss on the system. We perform power supply noise sensitivities studies, to derive the boundaries that power supply noise start to impact the pixel and readout chip performance. We perform noise and threshold dispersion analysis of the forward pixel panel using both step-down only and step-up/step-down DC-DC powering scheme with and without cooling. We provide comparisons between step-down only and step-up/step-down powering schemes. Future work includes the testing of the step-up converters in a weak magnetic field and after irradiation.

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