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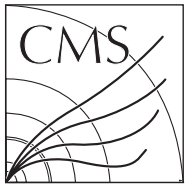

The Compact Muon Solenoid Experiment

Conference Report

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Application of Vertically Integrated Electronics to Intelligent Trackers

Ronald Lipton for the CMS Collaboration

Abstract

At Super-LHC luminosity it is expected that the standard suite of L1 triggers for CMS will saturate. Information from the tracker will be needed to reduce trigger rates to satisfy the L1 bandwidth. Tracking trigger modules which correlate information from closely-spaced sensor layers to form an on-detector momentum filter are being developed by several groups. We report on a trigger module design which utilizes three dimensional IC technology to incorporate chips which are connected both to the top and bottom sensor, providing the ability to filter information locally. A demonstration chip, the VICTR, has been submitted to the Chartered/Tezzaron two-tier 3D run coordinated by Fermilab. We report on the 3D design concept, the status of the VICTR chip and associated sensor integration utilizing oxide bonding.

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3D Technology for Intelligent Trackers

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ABSTRACT: At Super-LHC luminosity it is expected that the standard suite of level 1 triggers for CMS will saturate. Information from the tracker will be needed to reduce trigger rates to satisfy the level 1 bandwidth. Tracking trigger modules which correlate information from closely-spaced sensor layers to form an on-detector momentum filter are being developed by several groups. We report on a trigger module design which utilizes three dimensional integrated circuit technology incorporating chips which are connected both to the top and bottom sensor, providing the ability to filter information locally. A demonstration chip, the VICTR, has been submitted to the Chartered/Tezzaron two-tier 3D run coordinated by Fermilab. We report on the 3D design concept, the status of the VICTR chip and associated sensor integration utilizing oxide bonding.

KEYWORDS: 3D ; Track Trigger ; CMS.

Contents

The term "three dimensional technology" is used by the semiconductor industry to denote a set of technologies and processes which allow for fabrication of devices with vertically stacked interconnection. The primary driver for these developments is the need to increase the level of integration and density of packaging without the costs associated with smaller feature size. At the same time, High Energy Physics has been increasing the sophistication and complexity of it's silicon-based detectors as well as shrinking the size of the pixel. The two seem a natural fit. We will first describe some of the R&D underway at Fermilab and then describe it's application to a possible track trigger for CMS.

1. 3D technology

Three dimensional vertical integration utilizes a combination of wafer thinning, wafer bonding, and via formation technologies [1] [2]. The research is broad, and there are a number of technologies which are being developed in each category. For example wafers can be bonded using adhesives, by metal-metal fusion, or by direct chemical bonding of planarized oxide layers at the wafer surfaces. Vias are normally fabricated using tungsten plugs, either in the bulk silicon wafer itself, or in the insulating layers for silicon-on-insulator technology. In the following we describe our work on qualifying two of the candidate technologies for a track trigger module.

1.1 Direct Oxide Bonding

Metal routing layers on modern CMOS are typically separated by layers of silicon dioxide, which are deposited and then planarized for each process step. When activated by an amine dip and heated to about ≈ 275 deg C, two planar SiO_2 layers will form a strong chemical bond . Ziptronix Inc. has developed an interconnect process, DBI, based on imbedding metal into the oxide [4]. The metal on the two wafers form an electrical contact when the wafers are brought together and the oxide bond is annealed.

We have performed an initial test of this technology utilizing FPIX2 wafers from the BTeV project and sensors from an MIT-Lincoln Labs R&D run. The FPIX was designed for n-on-p sensors and the MIT-LL devices were p-on-n. However the "wrong polarity" performance was adequate for these tests. The FPIX includes an 128×26 array of pixels on 50×400 micron pitch. Individual diced sensors were DBI bonded to the FPIX wafer. The sensors were then thinned from 300 to 100 microns. The sensors included 50 micron deep conductive trenches and the backside could be biased through the trench contact.

The major problem found was due to bond voids, found by scanning acoustic microscopy, in 4 of 21 devices in wafer 1 and 12 of 25 in wafer 2. This is likely due to the unfavorable surface

topography in the two wafers. For die which were well bonded we found the bonding efficiency was 100%. We also found low noise, consistent with minimal additional capacitance due to the DBI bond [6]. We also found no evidence of degradation due to crosstalk between digital activity on the FPIX chip and the sensor, which is only a few microns away. This is presumably due to good shielding of the digital signals on the FPIX chip.

The bonded devices were also tested in the Fermilab test beam, where the resolution was consistent with the pixel pitch. The devices were also irradiated to 10Mrad in the Lowell, Mass. Co^{60} source. The small degradations in gain and noise were consistent with those seen in bare chips irradiated simultaneously.

1.2 Tezzaron multiproject run

A crucial ingredient for our 3D module design is electronics which can communicate directly with sensors above and below. Fermilab has organized a multiproject run which is the first to make these technologies available to high energy physics [7]. Wafers are fabricated at Chartered Semiconductor in their 0.13 micron process with imbedded Through-Silicon-Vias (TSVs) which extend 6 microns into the bulk silicon. The top of the wafers are patterned with a grid of hexagonal copper on 4 micron pitch. This copper serves both as a mechanical and electrical interconnection between pairs of wafers which are bonded face-to-face (Figure 1) by Tezzaron Inc. [8]. After the wafer-to-wafer bonding the top wafer is ground down to expose the TSVs and an aluminum contact layer is patterned.

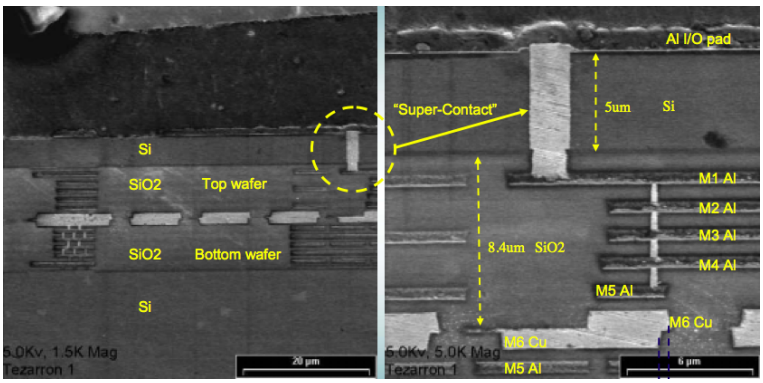


Figure 1. Scanning electron micrograph showing a pair of stacked and bonded wafers using the Tezzaron process.

2. Application to the CMS Track Trigger

The super-LHC upgrade is expected to provide an instantaneous peak luminosity of $5-10\times10^{34}$. At these luminosities the standard suite of triggers in CMS , which do not currently utilize tracking information at level 1, will saturate, and tracking information will be needed to select events. The track trigger is expected to provide information on all tracks with $P_\perp > 2-3$ GeV to the level 2 trigger within 3.2 μs. Transmission of all hits in the tracker to a off-detector processor is prohibitive, both in required power and bandwidth, so an initial $P_\perp$ selection needs to be performed

locally. This can be accomplished in a number of ways. We are exploring the design of a vertically interconnected module with silicon sensors separated by 1-2 mm.

2.1 Trigger Module Design

Figure 2a shows a conceptual drawing of a 3D trigger module. 3D technology, especially the DBI process, provides a technology which allows the readout chip to be bonded to the bottom detector and then thinned to reveal TSVs imbedded in the chip. These TSVs provide a path for direct connection of the sensor on the top to the same readout chip as the sensor on the bottom. The module design is driven by a number of considerations derived from the vertical interconnection:

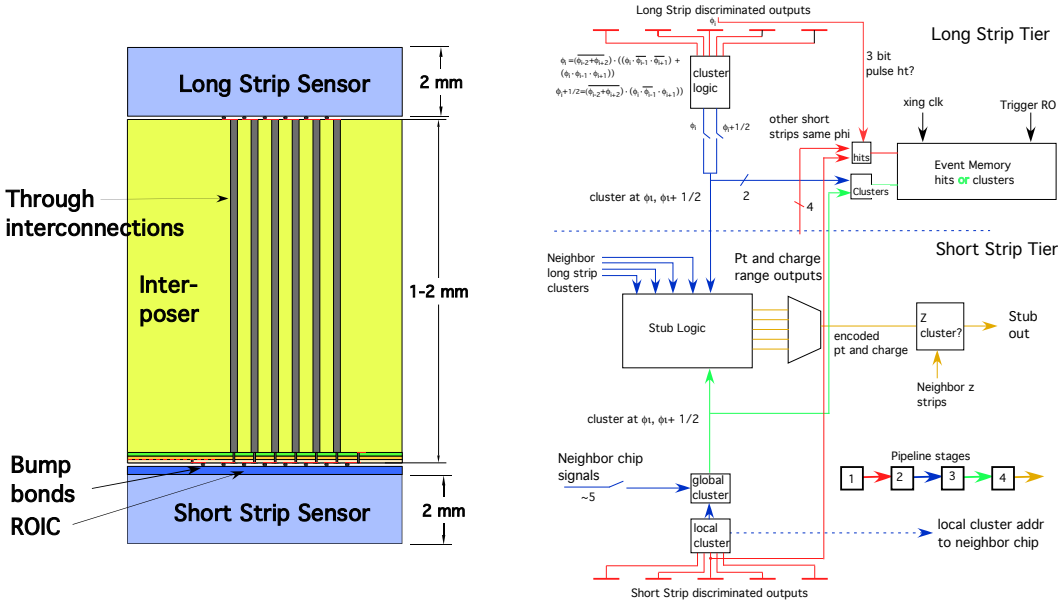
- Local interconnection of top and bottom strips simplifies the coincidence logic and eliminates the need for the encoding, transmission, and decoding of hit addresses.
- Analog transmission of sensor signals across an interposer to a single layer of chips on the bottom tier allows the module to use a single layer of chips, rather than one for each sensor, which would be needed in a 2D design.
- The top tier contains long ($\approx 1cm$) strips and the bottom tier short ($\approx 1-2mm$) strips. The short strips provide Z resolution necessary to accurately define the track vertex within the luminous region. However a single module does not have the lever arm to provide useful z information, so short strips on the top tier are unnecessary. Longer strips on the top tier limit the density of vias on the interposer and the complexity of the interposer design at the cost of additional capacitance.

The interposer is a crucial component of the design. It provides the top-to-bottom interconnection, distributes power, carries the signal bus, and acts as a spacer. The interposer is bump bonded directly to the top sensor and also bumped to the bottom sensor/readout IC sandwich. Candidate materials for the interposer are micromachined silicon or a more standard kapton-based circuit board. In either case material would be removed in the regions away from the interposer vias to reduce the module mass.

2.2 Data flow

Figure 2b shows a schematic of the data flow within a chip. The module must deliver a full event set of track stubs every 25ns. To do this a pipelined architecture is utilized:

1. Discriminated hits are delivered to the local cluster logic for the long and short strips. One to three strip clusters are formed which are associated with the central strip. Larger clusters are rejected.
2. Clusters from neighboring chips are included.
3. P$\perp$ selected stubs are identified by correlating a cluster within a short strip to clusters in the long strips in the local ϕ region.
4. Z clustering can be done.



a. b.

Figure 2. a) Conceptual drawing of a 3D-based stack. Analog signals flow from the top long strip sensor through the interposer to the readout IC (ROIC) bonded to the bottom sensor. b) Schematic of on-chip cluster and stub formation. Event memory is associated with the long strips.

5. Stubs are transmitted off chip.

Stubs are transmitted off the module using an optical link mounted on the support structure. Chips send the stubs to the link using a micropipeline ([9]) architecture. In the initial readout stage stubs are sent off the chips to chips at the edge of the module. The second stage transfers the stubs off-module to the optical drivers. All stubs associated with an event must be transferred within the 25ns crossing interval. Event data, which is larger but 400 times less frequent than the trigger data is interleaved into the trigger stream. Stubs or event data which cannot be transferred in this time are lost. Initial Monte Carlo studies indicate a typical load of 0.06 stubs/cm^2/crossing, but the pipeline must be designed to transfer stubs within one beam crossing including the fluctuations in local occupancy. In our studies we are assuming a factor of 5 for the ratio of peak to average occupancy, but full Monte Carlo studies of this need to be completed and verified with data.

2.3 VICTR Chip

We have designed and submitted a chip, the VICTR, designed to demonstrate the vertical interconnection of sensors through an interposer. The chip is part of the Tezzaron/Chartered multiproject run and consists of two tiers. The top tier will be connected through the interposer to a "long strip" sensor, consisting of 5 mm long strips on 80 micron pitch. The bottom tier will be DBI bonded to a "short strip" sensor consisting of 5×1 mm strips, also on 80 micron pitch. The front end amplifier/discriminator is a modified version of the ATLAS FEI4 front-end also included in the Tezzaron

run. The circuitry provides a prompt coincidence between top and bottom strips and serial readout of latched discriminator patterns to confirm functionality of the stack.

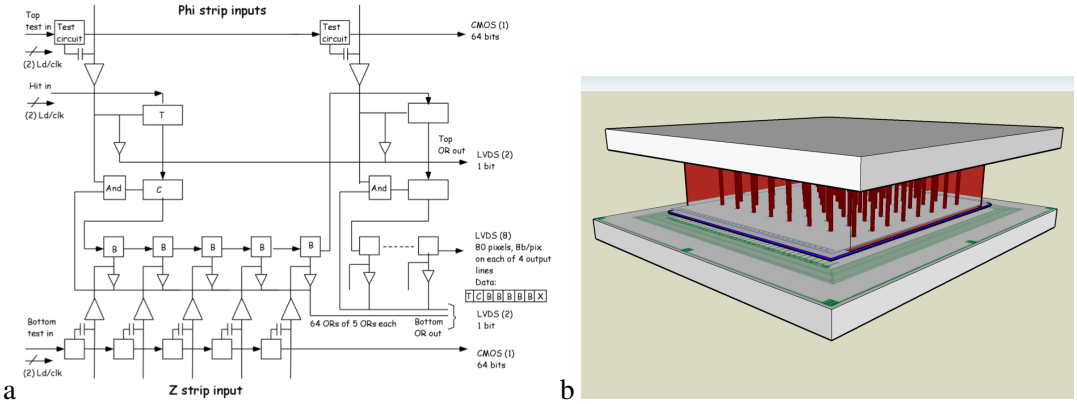


Figure 3. a) Schematic drawing of the VICTR chip. The 5 Z strips on the bottom tier are anded with the long phi strip on the top tier. b) Conceptual drawing of the VICTR-based 3D module stack. The interposer is transparent showing the 8×8 array of vias from the top sensor to the VICTR (which is outlined in blue). The active areas of the sensors are approximately 5×5 mm.

2.4 Stack Assembly

The VICTR will be used to assemble a full stack of the type envisioned for a track trigger module. Sensors which meet the topography requirements for the Ziptronix process are being fabricated at Brookhaven. The fabrication process will be:

1. The top side of completed two-tier Tezzaron wafers are oxide bonded to a handle wafer.
2. The bottom side of the wafers are ground to reveal the bottom TSVs.
3. Sensor and VICTR wafers are processed by Ziptronix to prepare for DBI bonding
4. Diced VICTR chips are DBI bonded to sensor wafers
5. The handle wafer bonded in step 1 is removed by grinding and etching. The remaining VICTR chip extends about 25 microns above the sensor wafer surface.
6. The bottom sensor/VICTR is bump bonded to the interposer
7. The top sensor is bump bonded to the bottom sensor/VICTR/interposer stack.

A sketch of the resulting 3D assembly is shown in Figure 3b.

3. Conclusions

The complexity of forming a silicon-based on-detector track trigger in the super-LHC environment is daunting. In addition to the 3D electronics described in this talk other challenges include interposer development, power delivery, optical data transmission, mechanical design, and downstream

trigger formation. Many of these issues have been discussed at this conference, several specific to the 3D design [10]. In spite of the challenges, technology for implementation of unprecedented intelligence in tracking and triggering systems is becoming available. These developments will undoubtably shape the science emerging from future experiments.

Acknowledgments

We would like to thank the ATLAS FEI-4 group for providing the layouts of the front end amplifier/discriminator sections as well as modifying the circuits for positive polarity and higher input capacitance.

References

[1] *IBM Journal of Research and Development*, Volume 52, No. 6, 2008. Issue devoted to 3D technology.

[2] Philip Garrou, Christopher Bower, Peter Ramm, *Handbook of 3D Integration Technology and Applications of 3D Integrated Circuits*, Wiley-VCH, 2008.

[3] R. Lipton, *3D-vertical integration of sensors and electronics*, *Nucl. Instrum. Meth. A* **579**, 690 (2007).

[4] Q.-Y.Tong, *Room temperature metal direct bonding*,' *Appl. Phys. Lett.* 89, 182101, 2006

[5] Q.-Y.Tong, G.Fountain, P.Enquist, *Room temperature SiO2/SiO2 covalent bonding*, *Appl. Phys. Lett.* 89, 042110, 2006

[6] Z. Ye, *Sensor/ROIC Integration using Oxide Bonding*, *arXiv:0902.2801* [physics.ins-det].

[7] G. Deptuch *et al.*, *Vertically Integrated Circuits at Fermilab*, FERMILAB-CONF-09-596-PPD

[8] R.S.Patti, *Three-Dimensional Integrated Circuits and the Future of System-on-Chip Designs*, *Proceedings of the IEEE*, Vol. 94, Issue 6, June 2006, pp. 1214-1224

[9] I. E. Sutherland, *Micropipelines*, *Commun. ACM*, vol. 32, no. 6, pp. 720–738, June 1989

[10] J. Alexander, W.E. Cooper, U. Heintz, M. Tripati, contributions to WIT2010.