

A 1 Mbit/s Communication Interface for a VMEbus System

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The communication interface presented in this paper is built around the VLSI device WD2511 manufactured by Western Digital Corporation /1/. It handles bit oriented, full duplex data communication which conforms to CCITT X.25 level 2 LAPB (link access protocol balanced). Those protocols include zero bit insertion and deletion, automatic appending and testing of frame check sequences (CRC) and automatic appending of address and control fields for level 2 protocols. The device also contains two direct memory access (DMA) channels, one for transmit and one for receive, to gain access to data buffers. Serial transmission rates of up to 1.1 Mbit/s in full duplex operation can be obtained.

16 on-chip I/O registers are used to control and monitor the operation of the controller. Two control registers provide means to initiate link set up, set the receiver to ready condition and start sending data. Three status registers contain fields for the transmit and receive counters, link status information, and interrupt causing state. Severe changes in link state or failures on the link level are indicated in the error register. Other registers are used to set the timer and retransmission counter, load the address field, and set the pointer to the cyclic buffer management queue.

Transmit data is accessed by the WD2511's DMA channels through cyclic buffer queues, one for transmit (TLOOK) and one for receive (RLOOK). Both queues consist of 8 elements containing buffer addresses and transmission counts.

At a serial transmission speed of 1 Mbit/s (and neglecting zero bit insertion/deletion) the controller would access a new data byte every 8 micro-second for either transmit and receive. This would introduce a heavy load on the computer bus, especially when several DMA devices are present on the same bus. To avoid this problem a dual port memory is provided on the board to separate the computer bus and the serial transmission operation. Communication between CPU and serial transmission line is therefore only possible via this dual port memory by moving messages between the main computing memory and the on-board memory.

The block diagram of the controller board is shown in figure 1. It can be divided into several functional modules. The VMEbus interface provides access to the computer bus signals. Only those signals are used that are necessary for slave data transfer operation [2]. Service requests to the CPU are initiated by the interrupt requester. All 7 interrupt levels may be selected by jumper option. Interrupt acknowledge cycles are answered by the slave device with the assertion of an interrupt vector that is also settable by jumpers.

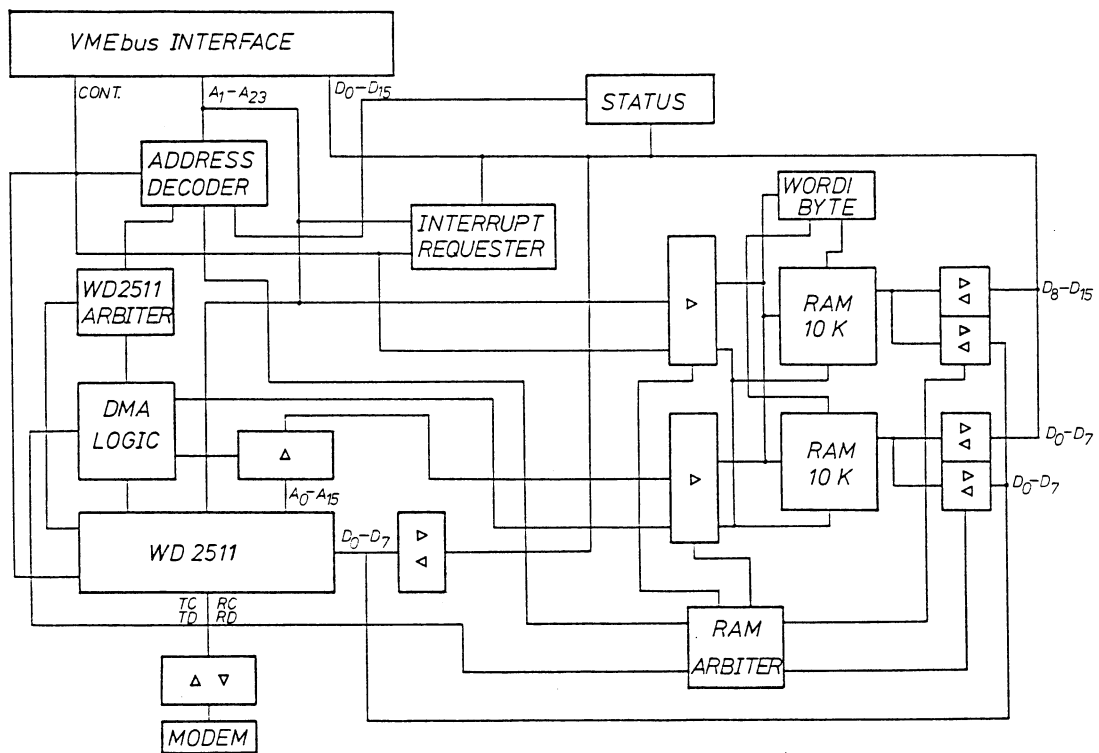


Figure 1: Block diagram of the communication interface

Access to the registers of the WD2511 and the 20 kByte on-board memory is accomplished through two dual port controllers. They arbitrate requests from the VMEbus and the DMA controllers of the WD2511 on a first come first served basis. A total of 32 kBytes address space on the VMEbus (the start address is jumper selectable) is necessary to operate the board. The status register is used for modem control and modem status information /3/.

Programming of the board is simple. After initially setting the registers of the WD2511 and establishing the TLOOK and RLOOK queues the receiver is set ready and link set up is initiated. Data to send is moved to a free transmit buffer and the corresponding entry in TLOOK is made ready. Then the WD2511 is commanded to send the packet. After successful transmission a block acknowledge interrupt is generated and the TLOOK entry is freed again. Received data packets are stored into a free buffer from RLOOK and a received packet interrupt is generated.

An application example of the controller board is shown in Figure 2. In a data acquisition system /4/, where large amounts of data have to be pro-

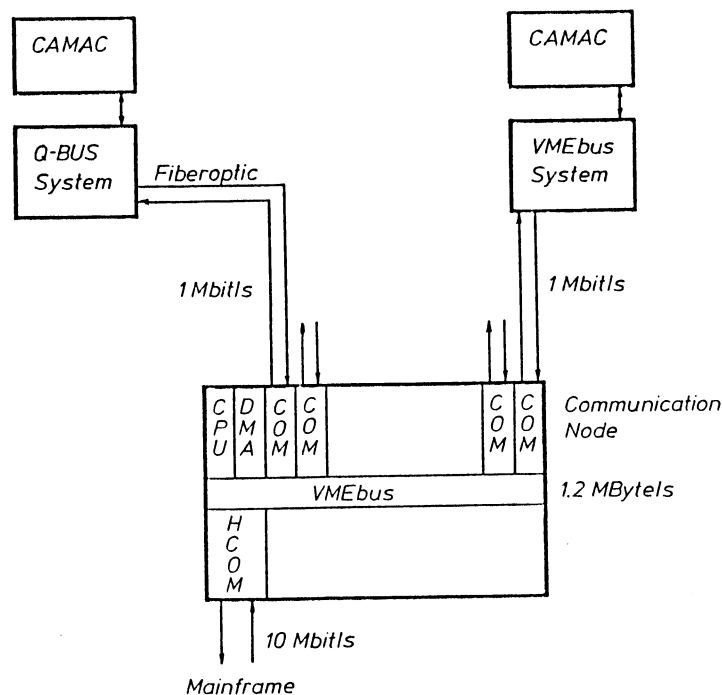


Figure 2: High bandwidth communication node in a data acquisition system

cessed in short time intervals, a mainframe computer is used for data analysis. The communication net connecting the various components of the system has to transfer the measured data as fast as possible to satisfy the user requirement of a sufficiently short response time.

The front end computers, that may be Q-Bus or VMEbus systems (both controller board versions are available), sample data from CAMAC crates. The preprocessed data are then transferred to a communication node via a fiber optics link built with the 1 Mbit/s communication controller. Incoming data packets interrupt the CPU. According to the routing information contained in the packets, data is transferred by the DMA controller (maximum transfer rate 1.2 MByte/s) from the receiver memory to the memory of the destination device. When data is sent to the mainframe computer the destination device is a 10Mbit/s communication board. In this example a throughput of 1 MByte/s may be achieved in the communication node.

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References:

- /1/ WD2511 X.25 Packet Network Interface (LAPB), data sheet, Western Digital Corporation
- /2/ VMEbus specification manual, VMEbus Manufacturers Group, Rev. B, Aug. 1982
- /3/ P. Heimann, A 1 MBit/s communication interface for VME/Q-Bus systems, AMOS development note D105.0, Max-Planck-Institut für Plasmaphysik, Informatik
- /4/ F. Hertweck, AMOS/D the data acquisition system for ASDEX-Upgrade, AMOS development note D100.0, Max-Planck-Institut für Plasmaphysik, Informatik