Design and measurements of 10 bit pipeline ADC for the Luminosity Detector at ILC

Marek Idzik[a], Krzysztof Swientek[a], Szymon Kulis[a]

[a] AGH university of Science and Technology, Faculty of Physics and Applied Computer Science
al. Mickiewicza 30, 30-059 Krakow, Poland

swientek@agh.edu.pl

Abstract

The design and the preliminary measurements of a prototype 10 bit pipeline ADC based on 1.5-bit per stage architecture, developed for the luminosity detector at International Linear Collider (ILC) are presented. The ADC is designed in two versions, with and without a sample-and-hold circuit (S/H) at the input. The prototypes are fabricated in 0.35 μm CMOS technology. A dedicated test setup with a fast FPGA based data acquisition system (DAQ) is developed for the ADC testing. The measurements of static (INL, DNL) and dynamic parameters are performed to understand and quantify the circuit performance. The integral (INL) and differential (DNL) nonlinearity are below 1 LSB and 0.5 LSB respectively. The dynamic measurements show signal to noise (SNHR) ratio of about 58 dB for sampling frequency up to 25 MHz.

I. Introduction

A dedicated multichannel readout electronics is needed for the operation of the luminosity detector (LumiCal) [1] at the future ILC collider [2, 3]. The energy deposited in a silicon sensor, detected and amplified in the front-end electronics, needs to be digitised and registered for further analysis. The precision required on the measurement of deposited energy was studied in simulations and was found to be about 10 bits [4]. Considering the number of detector channels needed (∼200,000) and the limitations on area and power, the optimal choice for the analog to digital conversion seems a dedicated multichannel ADC.

Two schemes of analog to digital conversion are presently under study: one relatively slow ADC per each front-end channel and one faster ADC per group of (about) 8 channels. First option would be the simplest solution from the designer point of view while the second one would allow to save on chip area. The first option requires an ADC with sampling rate of around 3 Msample/s while the second requires the sampling rate of about 24 Msample/s. One of the most efficient architectures assuring a good compromise between the speed, the area and the power consumption is the pipeline ADC [5, 6, 7]. This architecture was chosen for the LumiCal data conversion. Since in the ILC experiment each 1 ms long active beam time will be followed by 200 ms pause [8] the requirements on readout electronics power dissipation may be strongly relaxed if the power is switched off during the pause.

II. Design

The pipeline ADC is built of a number of serially connected converting stages as shown in fig. 1. In this work an architecture with 1.5-bit stages is chosen because of its simplicity and immunity to the offsets in the comparator and amplifier circuits [5]. The 1.5-bit since generates only three different values coded on 2 output bits which are sent to a digital correction block where 18 input bits from 9 stages are combined together resulting in 10 bits of ADC output.

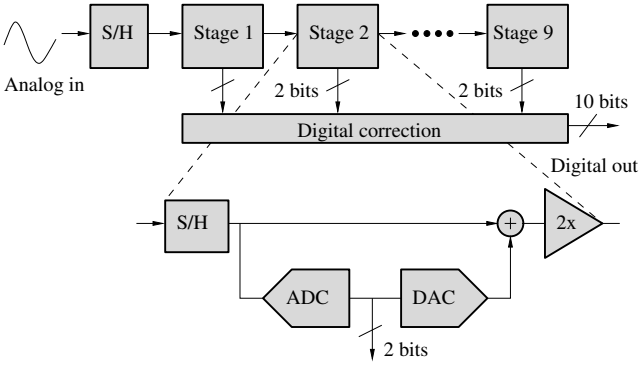

Figure 1: Pipeline ADC architecture

The block diagram of fully differential single stage is shown in fig. 2. Each 1.5-bit stage consist of two comparators, two pairs of capacitors C_s and C_f, an operational transconductance amplifier, several switches and small digital logic circuit. The stage gain of 2 is obtained setting $C_s = C_f$. Since the chosen ADC architecture leaves very relaxed requirements on the comparators thresholds (∼100 mV precision) the comparators are designed as simple dynamic latches.

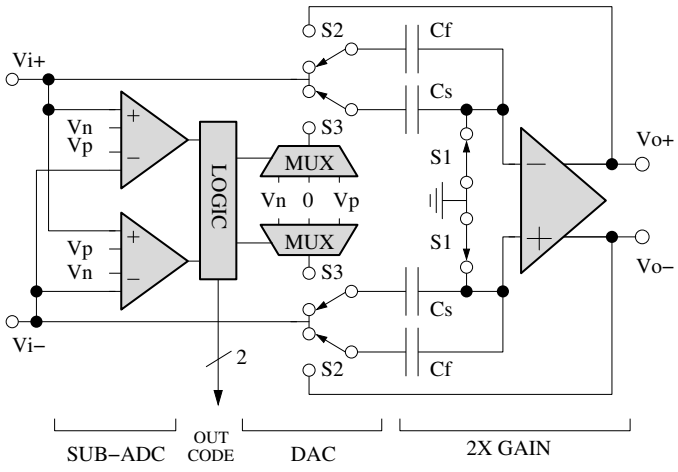

Figure 2: Simplified schematic of a 1.5-bit stage

A critical block of pipeline ADC is the differential amplifier. A telescopic cascode amplifier configuration is used here. This represents the most efficient solution with respect to speed vs power in comparison to commonly used configurations like folded cascode and two stage amplifier. Such solution is possible since the considered technology with relatively high 3.3 V supply voltage leaves enough space for the signal dynamic range, which otherwise would be a weak point of the telescopic configuration. In order to obtain high enough gain in a single stage amplifier a gain-boosting scheme is implemented [9, 10].

To allow the possibility of power saving during the beam pause the prototype features the switches for clock and analog power. One can turn off the biasing currents in the differential amplifier and stop the clock in digital blocks.

Since it is not decided yet whether the S/H circuit will be implemented in the front-end channel or in the ADC itself there are two versions of ADC prototypes with and without S/H circuits.

III. Measurement setup

A number of specific requirements need to be fulfilled for an efficient and complete ADC testing. The most important are:

- availability of differential input signal generator
- input signal and reference voltages precision better than ADC resolution
- wide frequency range of external sampling clock and sine wave input source (for dynamic testing)
- for ADC without sample and hold input stage the input sine waveform should be step like to allow dynamic testing
- acquisition system able to record the digitised ADC data with the rate exceeding the ADC sampling frequency
- possibility to perform automatic scans over input signal amplitude, frequency, sampling rate etc.

The block diagram of a dedicated FPGA based test setup fulfilling above requirements is shown in fig. 3. The setup is controlled from a PC computer through GPIB and USB interfaces. The input signal and clock is generated by Tektronix Arbitrary Waveform Generator AWG2021. Since this 12 bit generator produces single ended signal the conversion to differential is needed. It is done by a dedicated circuit comprised of a fast differential amplifier (THS4505). For measurements with static signals AWG2021 generates a slow voltage ramp in the full ADC range. For dynamic measurements in ADC without S/H input stage the same device generates sine-like step signal.

The reference voltages are generated with the Agilent B1500A Semiconductor Device Analyser. Both the AWG2021 and the B1500A are controlled through the GPIB interface. Such interfacing allows the implementation of automatic scans over all AWG2021 and B1500A parameters (amplitude, frequency, biasing, etc.) and so to determine their effect on the overall circuit performance.

The core of the setup is the FPGA DAQ system built using Altium Nanoboard with Xilinx Spartan-IIE FPGA. Since the data acquisition should be fast the control logic block which reads the data lines from ADC and stores it in the memory (available on the Nanoboard) is written in Verilog HDL language. On the other hand the 8051 microcontroller (IP Core) with dedicated firmware is used to manage the communication between the NanoBoard and PC. Since there is no requirement for very high transmission rate the 8051 works at lower frequency than the logic block. Several simple high level commands are sent from the PC to the microcontroller through its UART port to control the behaviour of the DAQ. UART to USB converter is used in between the Nanoboard and the computer to improve the flexibility of the system. The commands received by the microcontroller configure logic block, start data acquisition and data readout.

It was verified experimentally that the described configuration allows acquisition of the data with a sampling frequency up to 100 MHz.

IV. Preliminary measurements

The ADC prototypes are fabricated in 0.35 μm four metal two poly CMOS technology. The photograph of the ASIC containing ADC channels with and without S/H stage is shown in fig. 4. The size of the chip is 2700×3800 μm which encompass six ADC prototypes, small control logic and pads.

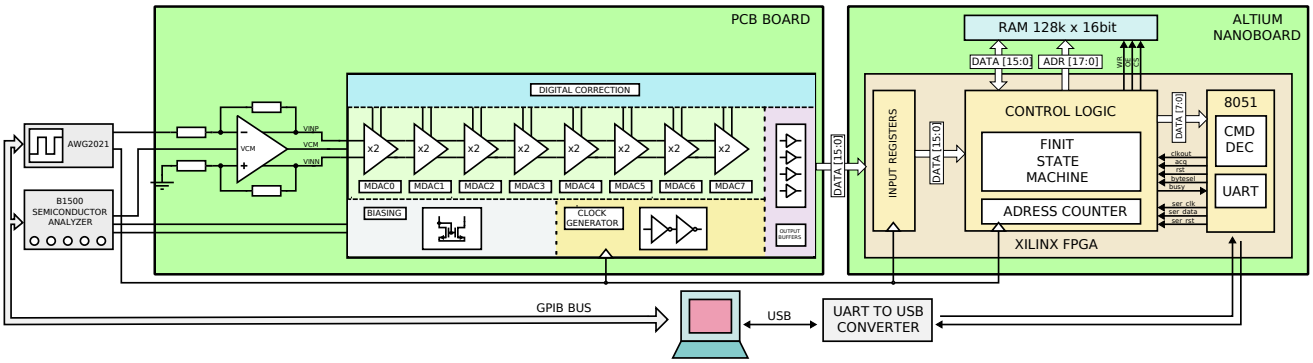

Figure 3: Diagram of a complete test system

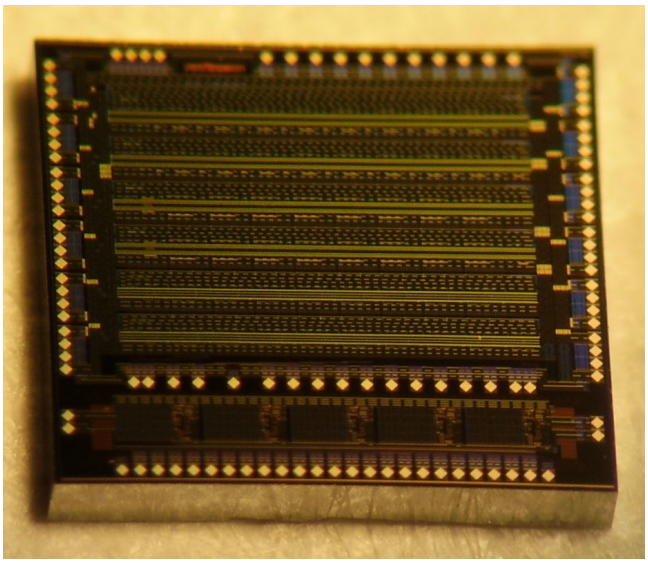

Figure 4: Photograph of ADC ASIC

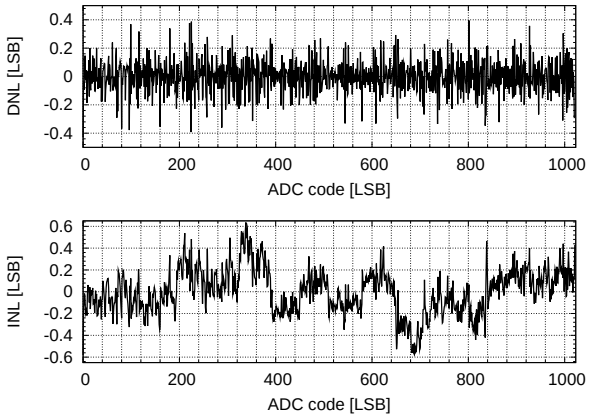

Figure 6: INL and DNL for ADC with sample-and-hold

A. *Static measurements*

Static measurements are performed for the input voltage ramped in the range from -1 V to 1 V. The measured ADC transfer function is shown in figure 5. It is seen that the ASIC is fully functional and linear in first approximation.

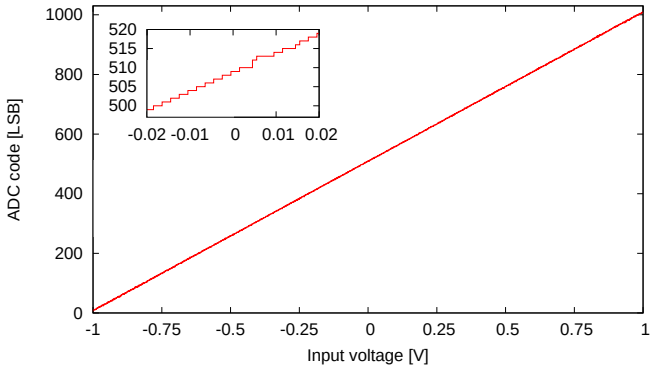

Figure 5: ADC output codes vs input voltage; single measurement typical result

To eliminate noise each data point is measured several hundred times. The magnification in the upper left corner of the figure 5 shows the most probable value (mode) calculated in each point.

The differential (DNL) and integral (INL) nonlinearities are computed using the histogramming method [11]. The results for the ADC with and without sample-and-hold circuits are shown respectively in figure 6 and figure 7.

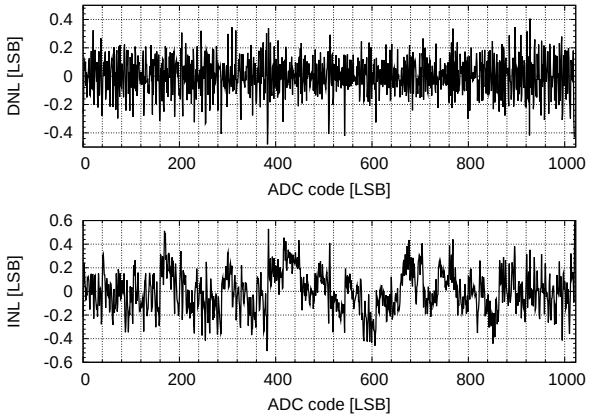

Figure 7: INL and DNL for ADC without sample-and-hold

It is seen that both versions show good linearity i.e. the DNL stays always below 0.5 LSB and INL is significantly below 1 LSB. The ENOB computed from the INL curve is 9.71 in the first case and 9.78 in the second one.

B. *Dynamic measurements*

The dynamic measurements are performed by applying a sine signal to the ADC input and measuring the frequency spectrum distribution at the output. A typical FFT spectrum distribution is shown in figure 8. It is seen that the highest harmonic components are well below 70 dB and the noise level is significantly lower at about 90 dB.

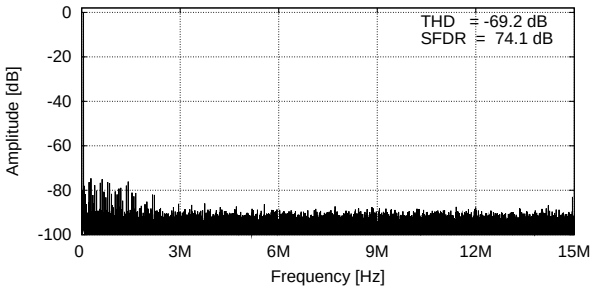

Figure 8: Sample FFT of 40 kHz signal at 30 Msps

From the obtained FFT spectrum important dynamic parameters were calculated. In particular the signal to noise performance was studied. The signal to noise ratio without harmonics (SNHR) as a function of sampling frequency is shown in figure 9. It is seen that SNHR=58 dB up to around 25 MHz and then starts to decrease. The harmonics parameters (THD, SFDR) are not presented here since it was found that the AWG2021 itself generates spurious harmonics on 40 dB level. In order to check the level of harmonics only few measurements were done using the Agilent 33220A arbitrary waveform generator confirming that the harmonics components are below 70 dB.

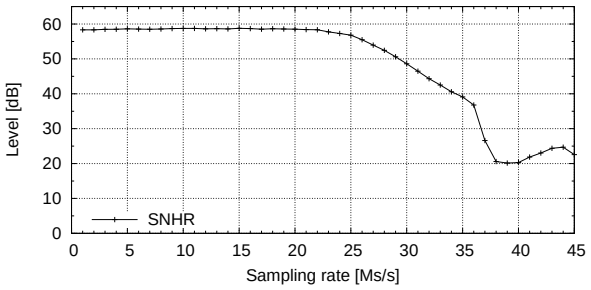

Figure 9: SNHR vs frequency

V. Power consumption

The first power consumption measurements were done at 30 Mhz sampling frequency. For the ADC containing S/H stage the analog and digital currents are 8.6 mA and 6.2 mA respectively. For the version without S/H the same currents are 7.1 mA and 5.5 mA respectively. The power may be reduced when lower sampling frequency is used.

VI. Summary

A 10 bit pipeline ADC was designed, produced and found fully functional. Preliminary static measurements show the maximum DNL and INL of about 0.43 LSB and 0.64 LSB respectively. The dynamic signal to noise ratio measurements give around 58 dB. The performance measurements confirmed the resolution close to 9.5 bits. More detailed dynamic measurements are needed to study better the harmonics. Also the tests of power saving features need to be performed.

VII. Acknowledgements

This work was partially supported by the Commission of the European Communities under the 6^{th} Framework Programme "Structuring the European Research Area", contract number RII3-026126. It was also supported in part by the Polish Ministry of Science and Higher Education under contract nr 372/6.PRUE/2007/7.

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